SPECIFICATION

Device Name	:	IGBT-IPM **(RoHS compliant product)**
Type Name	:	7MBP400VEA060-50
Spec. No.	:	MS6M1440

	DATE	NAME	APPROVED
DRAWN	Feb. 27, 2012	N. Shimizu	
CHECKED	Feb. 27, 2012	M. Watanabe	O.Ikawa
CHECKED	Feb. 27, 2012	K. Oshika	

REVISIONS

Fuji Electric Co.,Ltd.

DWG NO. MS6M1440 1/26

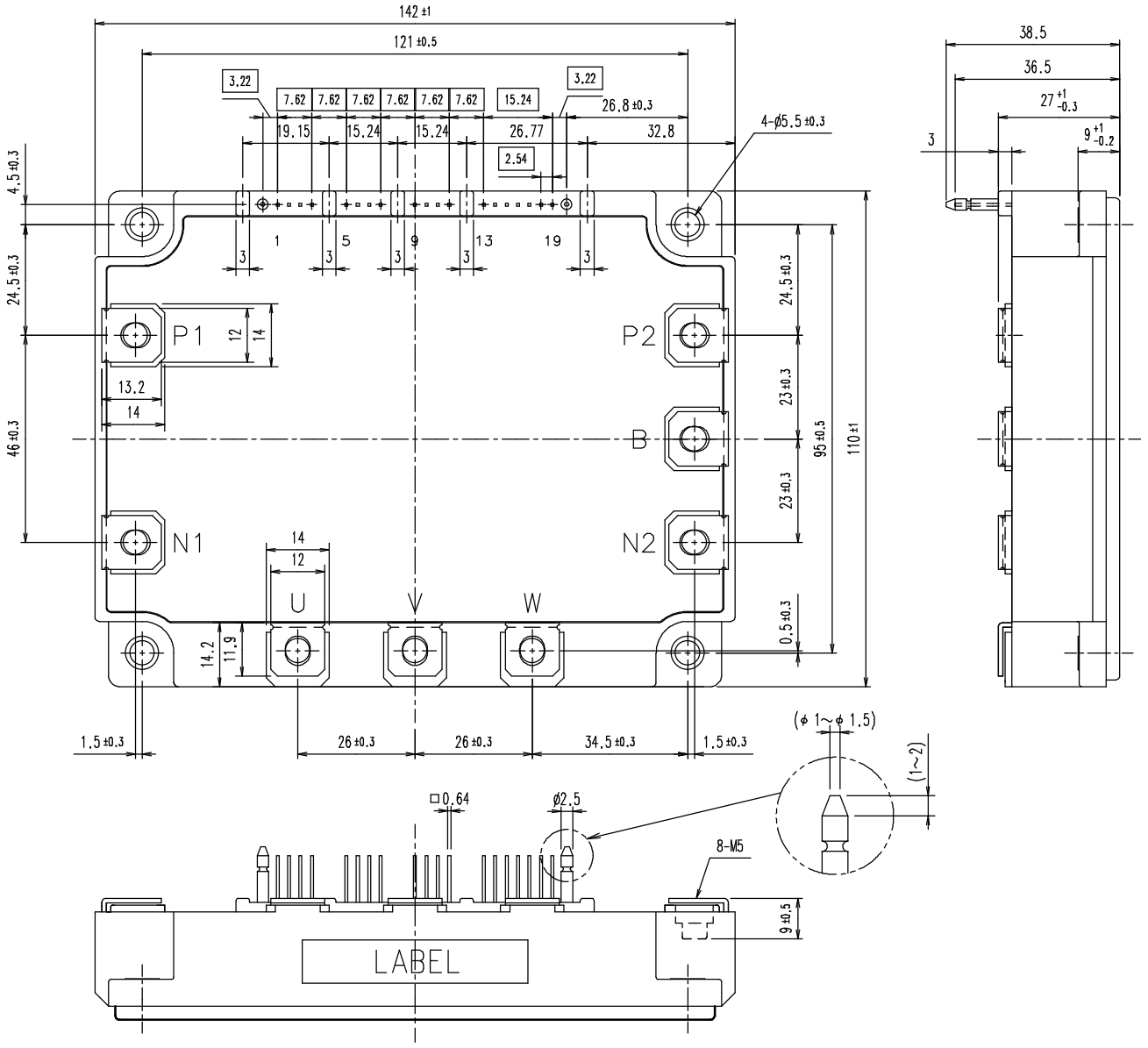
Revised Records

Date	Classi-fication	Ind.	Content	Applied date	Drawn	Checked	Checked	Approved
Feb.27,2012	Enactment	-	-	Issued date	H. Shimizu	M. Watanabe	K. Oshika	O. Ikawa

1. Package Outline Drawings

(Tc=25℃)

Package type: P631



Indication on module(ﾓｼﾞｭｰﾙ表示)

Display on module label

- Logo of production
- Type name: 7MBP400VEA060-50
- IC,VCES rating 400A 600V
- Lot No. (5digits)※
- Place of manufacturing (code)
- Data matrix

※ **Indication of Lot No.**

□□□□□

Odered No. in monthly
Manufactured month
(Jan.～Sep.：1～9, Oct:O, Nov.:N, Dec.:D)
Last digit of manufactured year

注)

Note **1.□は理論寸法を示す。**
"□" shows theoretical dimension.
2.端子ﾋﾟｯﾁは根元寸法とする。
The dimensions of the terminals are defined at the bottom.
3.( )内寸法は、参考値とする。
"( )" shows reference dimension.
4.主端子：Niめっき
Main terminal : Ni plating
制御端子：下地Ni＋表面Auめっき
Control terminal : Au plating on Ni plating

[Dimensions in mm]

2. Pin Descriptions

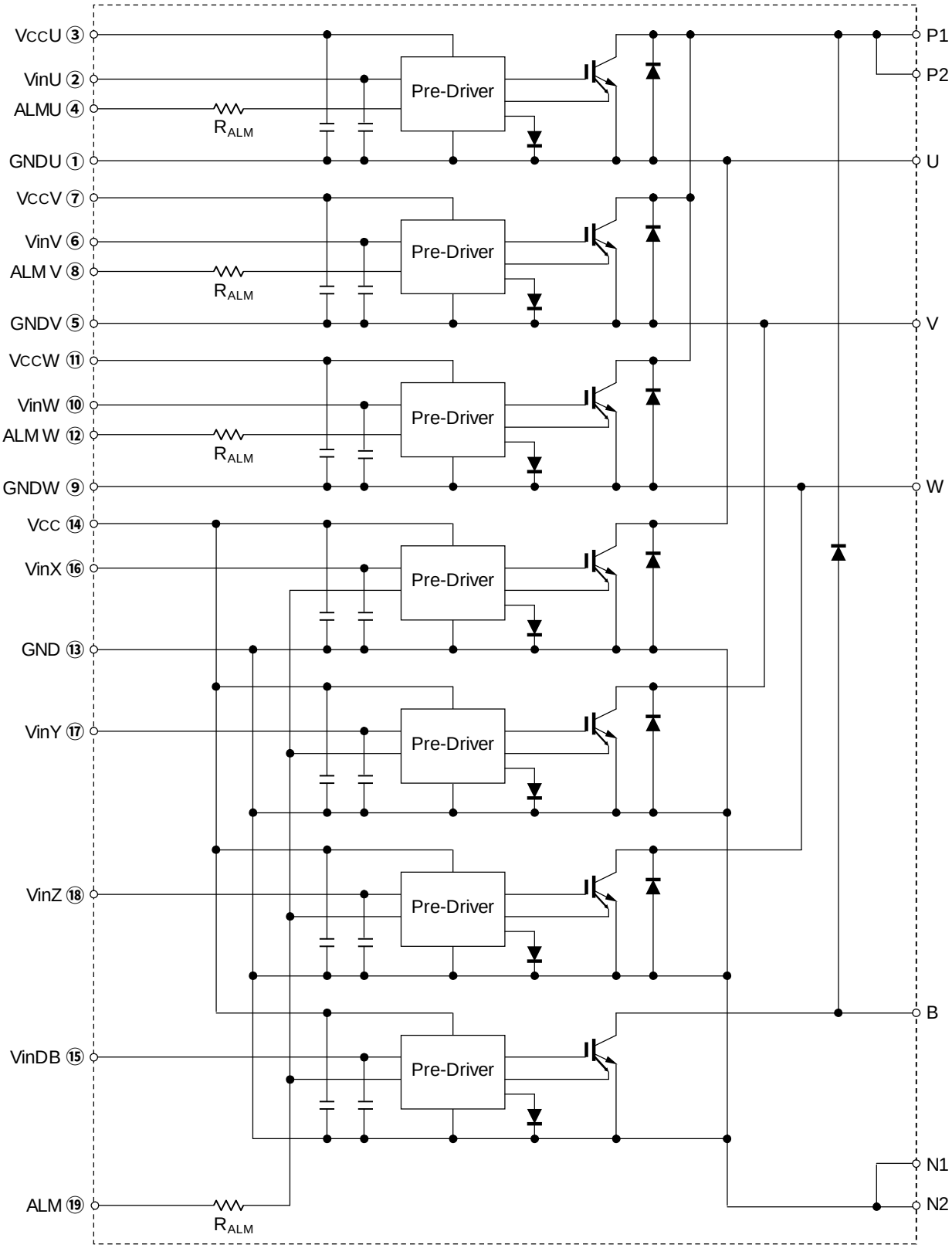
2.1 Main circuit

Symbol	Description
P1,P2	Positive input supply voltage.
U	Output (U).
V	Output (V).
W	Output (W).
N1,N2	Negative input supply voltage.
B	Collector terminal of Brake IGBT.

2.1 Control circuit

No.	Symbol	Description
①	GNDU	High side ground (U).
②	VinU	Logic input for IGBT gate drive (U).
③	VccU	High side supply voltage (U).
④	ALMU	Alarm signal output (U).
⑤	GNDV	High side ground (V).
⑥	VinV	Logic input for IGBT gate drive (V).
⑦	VccV	High side supply voltage (V).
⑧	ALMV	Alarm signal output (V).
⑨	GNDW	High side ground (W).
⑩	VinW	Logic input for IGBT gate drive (W).
⑪	VccW	High side supply voltage (W).
⑫	ALMW	Alarm signal output (W).
⑬	GND	Low side ground.
⑭	Vcc	Low side supply voltage.
⑮	VinDB	Logic input for Brake IGBT gate drive.
⑯	VinX	Logic input for IGBT gate drive (X).
⑰	VinY	Logic input for IGBT gate drive (Y).
⑱	VinZ	Logic input for IGBT gate drive (Z).
⑲	ALM	Low side alarm signal output.

3. Block Diagram



Pre-drivers include following functions
1. Amplifier for driver
2. Short circuit protection
3. Under voltage lockout circuit
4. Over current protection
5. IGBT chip over heating protection

4. Absolute Maximum Ratings

T_C=25℃, V_{CC}=15V unless otherwise specified.

Items				Symbol	Min.	Max.	Units
Collector-Emitter Voltage *1				V_{CES}	0	600	V
Short Circuit Voltage				V_{SC}	200	400	V
Inverter	Collector Current	DC		I_C	-	400	A
		1ms		I_{CP}	-	800	A
		Duty=68.6%	*2	$-I_C$	-	400	A
	Collector Power Dissipation	1 device	*3	P_C	-	1086	W
Brake	Collector Current	DC		I_C	-	200	A
		1ms		I_{CP}	-	400	A
	Forward Current of Diode			I_F	-	200	A
	Collector Power Dissipation	1 device	*3	P_C	-	714	W
Supply Voltage of Pre-Driver *4				V_{CC}	-0.5	20	V
Input Signal Voltage *5				V_{in}	-0.5	V_{CC}+0.5	V
Alarm Signal Voltage *6				V_{ALM}	-0.5	V_{CC}	V
Alarm Signal Current *7				I_{ALM}	-	20	mA
Junction Temperature				T_j	-	150	℃
Operating Case Temperature				T_{opr}	-20	110	℃
Storage Temperature				T_{stg}	-40	125	℃
Solder Temperature *8				T_{sol}	-	260	℃
Isolating Voltage *9				V_{iso}	-	AC2500	Vrms
Screw Torque		Terminal (M5)		-	-	3.5	Nm
		Mounting (M5)					

Notes

*1: V_{CES} shall be applied to the input voltage between all Collector and Emitter.
[P1-(U,V,W,B) , P2-(U,V,W,B) , (U,V,W,B)-N1 , (U,V,W,B)-N2]

*2: Duty=125℃/$R_{th(j-c)D}$/(I_F×V_F Max.)×100

*3: P_C=125℃/$R_{th(j-c)Q}$ (Inverter & Brake)

*4: V_{CC} shall be applied to the input voltage between terminal No.3 and 1, 7 and 5, 11 and 9, 14 and 13.

*5: V_{in} shall be applied to the input voltage between terminal No.2 and 1, 6 and 5, 10 and 9, 15~18 and 13.

*6: V_{ALM} shall be applied to the voltage between terminal No.4 and 1, 8 and 5, 12 and 9, 19 and 13.

*7: I_{ALM} shall be applied to the input current to terminal No.4,8,12 and 19.

*8: Immersion time 10±1sec. 1 time

*9: Terminal to base, 50/60Hz sine wave 1min. All terminals should be connected together during the test.

5. Electrical Characteristics

T_j＝25℃, V_{CC}＝15V unless otherwise specified.

5.1 Main circuit

Item		Symbol	Conditions		Min.	Typ.	Max.	Units
Inverter	Collector Current at off signal input	I_{CES}	V_{CE}=600V		-	-	1.0	mA
	Collector-Emitter saturation voltage *10	$V_{CE(sat)}$	I_C=400A Fig.4	Terminal	-	-	2.05	V
				Chip	-	1.25	-	V
	Forward voltage of FWD *10	V_F	I_F=400A Fig.5	Terminal	-	-	2.60	V
				Chip	-	1.80	-	V
Brake	Collector Current at off signal input	I_{CES}	V_{CE}=600V		-	-	1.0	mA
	Collector-Emitter saturation voltage *10	$V_{CE(sat)}$	I_C=200A Fig.4	Terminal	-	-	1.80	V
				Chip	-	1.25	-	V
	Forward voltage of FWD *10	V_F	I_F=200A Fig.5	Terminal	-	-	2.50	V
				Chip	-	2.00	-	V
Switching time		t_{on}	V_{DC}=300V, Tj=125℃		1.1	-	-	μs
		t_{off}	I_C=400A Fig.1,6		-	-	2.1	μs
		t_{rr}	V_{DC}=300V I_F=400A Fig.1,6		-	-	0.3	μs

*10: The Max value is a case where it measures from P2-(U,V,W,B) , (U,V,W,B)-N2.

5.2 Control circuit

Item	Symbol	Conditions		Min.	Typ.	Max.	Units
Supply current of P-side pre-driver (per one unit)	I_{ccp}	Switching Frequency = 0-15kHz		-	-	45	mA
Supply current of N-side pre-driver	I_{ccn}	Tc=-20~110℃ Fig.7		-	-	155	mA
Input signal threshold voltage	$V_{inth(on)}$	Vin-GND	ON	1.2	1.4	1.6	V
	$V_{inth(off)}$		OFF	1.5	1.7	1.9	V

5.3 Protection Circuit

Item		Symbol	Conditions		Min.	Typ.	Max.	Units
Over Current Protection Level	Inverter	I_{OC}	Tj=125℃ Fig.3		600	-	-	A
	Brake				300	-	-	A
Over Current Protection Delay time		t_{dOC}	Tj=125℃, Fig.3		-	5	-	μs
Short Circuit Protection Delay time		t_{SC}	Tj=125℃, Fig.8		-	2	3	μs
IGBT Chips Over Heating Protection Temperature Level		T_{jOH}	Surface of IGBT Chips		150	-	-	℃
Over Heating Protection Hysteresis		T_{jH}			-	20	-	℃
Under Voltage Protection Level		V_{UV}			11.0	-	12.5	V
Under Voltage Protection Hysteresis		V_H			0.2	0.5	-	V
Alarm Signal Hold Time		$t_{ALM(OC)}$	ALM-GND		1.0	2.0	2.4	ms
		$t_{ALM(UV)}$	Tc=-20～110℃	Vcc≧10V	2.5	4.0	4.9	ms
		$t_{ALM(TjOH)}$	Fig.2		5.0	8.0	11.0	ms
Resistance for current limit		R_{ALM}			960	1265	1570	Ω

6.Thermal Characteristics (Tc = 25℃)

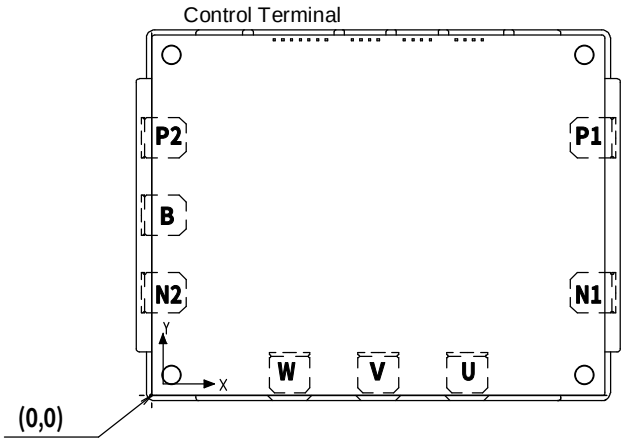
Item			Symbol	Min.	Typ.	Max.	Units
Junction to Case Thermal Resistance*11	Inverter	IGBT	Rth(j-c)Q	-	-	0.115	℃/W
		FWD	Rth(j-c)D	-	-	0.175	℃/W
	Brake	IGBT	Rth(j-c)Q	-	-	0.175	℃/W
		FWD	Rth(j-c)D	-	-	0.405	℃/W
Case to Fin Thermal Resistance with Compound			Rth(c-f)	-	0.05	-	℃/W

*11: For 1device , the measurement point of the case is just under the chip.

Chip layout drawing

Package :**P631**

Type name :**7MBP400VEA060-50**



P631 Bottom view

Location of measurement of Tc (chip center right under)

Element / Axis	U		V		W		X		Y		Z	
	IGBT	FWD	IGBT	FWD	IGBT	FWD	IGBT	FWD	IGBT	FWD	IGBT	FWD
X	105.2	119.9	69.9	84.6	34.6	49.3	117.3	102.6	82.0	67.3	46.7	32.0
Y	76.2	69.7	76.2	69.7	76.2	69.7	33.9	40.4	33.9	40.4	33.9	40.4

Element / Axis	B	
	IGBT	FWD
X	14.1	10.4
Y	32.9	73.6

(**Unit**:**mm**)

7.Noise Immunity (VDC=300V, VCC=15V, Test Circuit Figure 9.)

Item	Conditions	Min.	Typ.	Max.	Units
Common mode rectangular noise	Pulse width 1μs, polarity ±10min. Judge: no over-current, no miss operating	±2.0	-	-	kV

8.Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units
DC Bus Voltage	VDC	-	-	400	V
Power Supply Voltage of Pre-Driver	VCC	13.5	15.0	16.5	V
Switching frequency of IPM	fSW	-	-	20	kHz
Arm shoot through blocking time for IPM's input signal	tdead	1.0	-	-	μs
Screw Torque (M5)	-	2.5	-	3.5	Nm

9.Weight

Item	Symbol	Min.	Typ.	Max.	Units
Weight	Wt	-	980	-	g

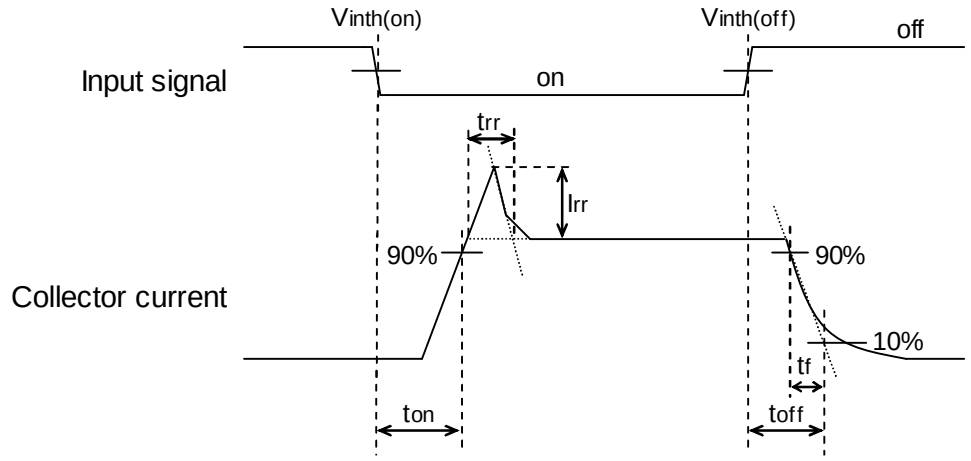


Figure1. Switching Time Waveform Definitions.

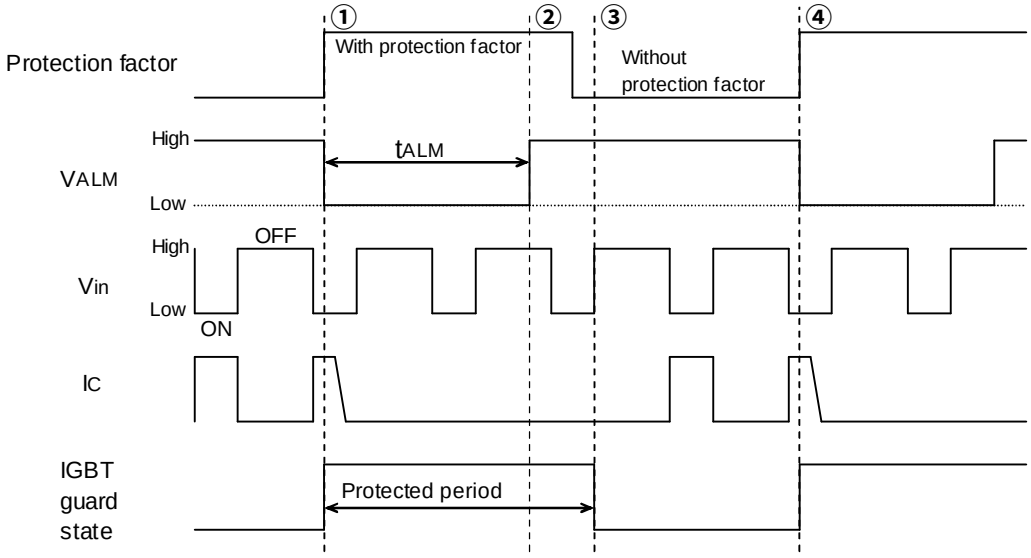


Figure2. Input/output Timing Diagram.

〔Alarm output〕 〔**アラーム出力**〕

Set condition(①): The alarm is output only once(High⇒Low) according to timing when the protection factor occurs.

ｾｯﾄ条件(①): **保護要因の発生したﾀｲﾐﾝｸﾞで、保護動作した相より1回 のみアラーム出力**(High⇒Low)**されます。**

Reset condition②: After it continues at the hold time of each alarm factor(tALM)、it is released regardless of the presence of the alarm factor.

ﾘｾｯﾄ条件(②): **要因毎の保持時間**(tALM)**継続後に 要因の有無に関係なく解除されます。**

〔Protection operation(Switching stop of IGBT)〕 〔**保護動作**(IGBT**のｽｲｯﾁﾝｸﾞ停止**)〕

Set condition(①): The protection function operates when the protection factor occurs.

ｾｯﾄ条件(①): **保護要因の発生とともに動作します。**

Reset condition (③): When the condition of protection factor cancellation、tALM passage、and input signal OFF becomes complete、the protection operation is released.

ﾘｾｯﾄ条件(③): **保護要因解消、**tALM**経過、入力信号**OFF**の条件が揃った時に解除されます。**

〔Condition that alarm is output again〕 〔**アラームが再出力される条件**〕

The protection factor occurs again after the protection operation is reset、the protection function operates at the same time when the alarm is output.(④)

保護動作がﾘｾｯﾄされた後に再度保護要因が発生すれば、アラームが再出力されると同時に保護動作 します(④)**。**

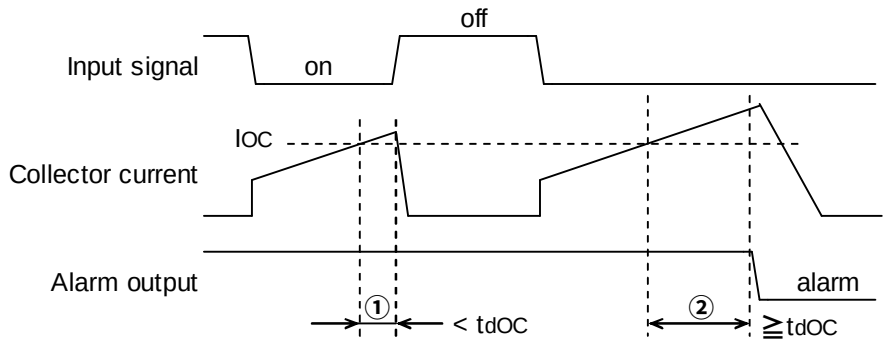


Figure3. Over Current Protection Timing Diagram.

Period ① When a collector current over the OC level flows and the OFF command is input within a p less than the trip delay time tdOC, the current is hard-interrupted and no alarm is output.

期間①: **OCﾚﾍﾞﾙを超えたコレクタ電流が流れ、遮断遅れ時間**tdOC**より短い時間内で、オフ指令が入力された場合は、電流をハード遮断しアラームは出力しません。**

Period ② When a collector current over the OC level flows for a period more than the trip delay time the current is soft-interrupted and the alarm signals are outputted.

期間②: **OCﾚﾍﾞﾙを超えたコレクタ電流が、遮断遅れ時間**tdOC**を超えた時間以上が流れ続けると電流をソフト遮断しアラームを出力します。**

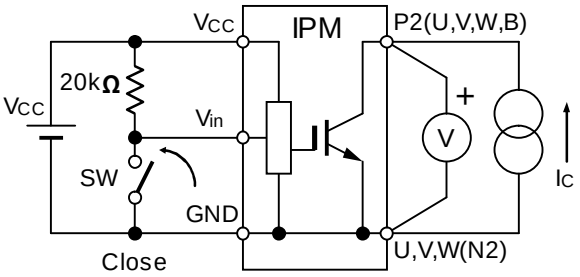


Figure4. $V_{CE(sat)}$ Test Circuit(Terminal)

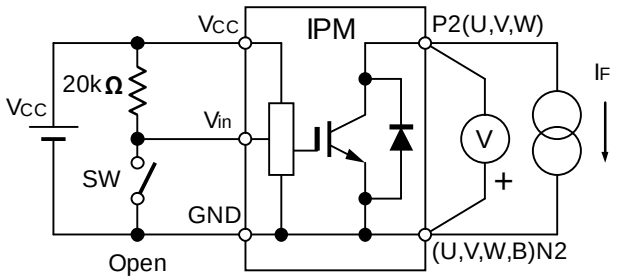


Figure5. V_F Test Circuit(Terminal)

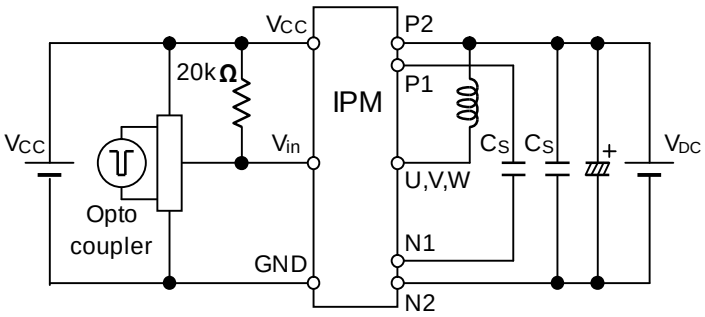


Figure6. Switching Characteristics Test Circuit

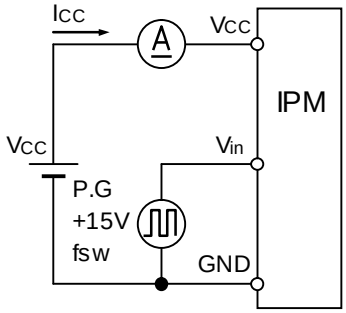


Figure7. I_{CC} Test Circuit

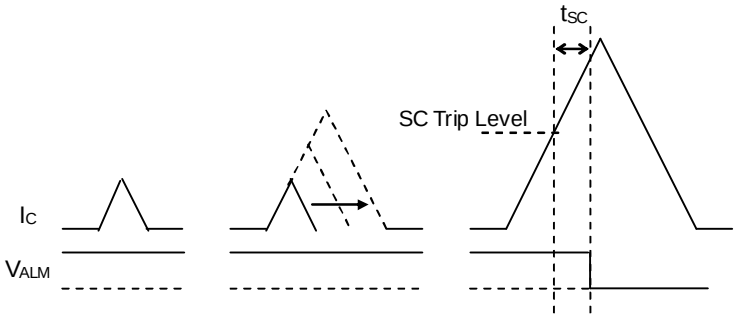
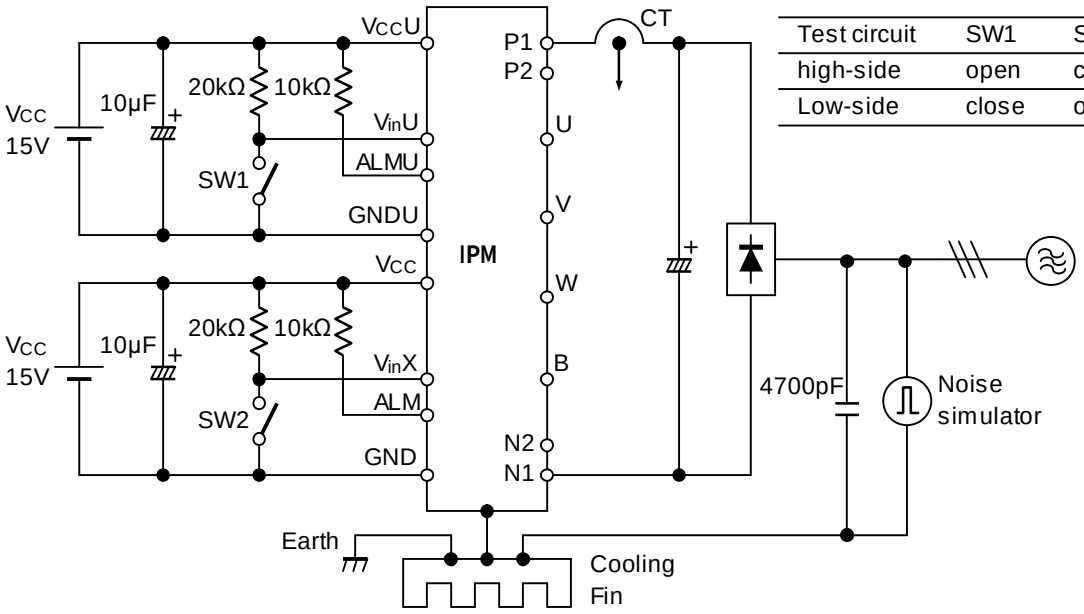


Figure8. Definition of t_{SC}



Test circuit	SW1	SW2
high-side	open	close
Low-side	close	open

Figure9. Noise Test Circuit

10. Truth table

10.1 IGBT Control

The following table shows the IGBT ON/OFF status with respect to the input signal V_{in}.

The IGBT can be turned on when V_{in} is at “Low” level without the operation of IPM’s protection.

入力信号Vin**に対する**IGBT**の**ON/OFF**状態を下表に示します。**

保護要因が無い状態において、Vin**が** ”Low” **レベルで、**IGBT**はON**します。

Input signal	IPM's Protection status	Output (IGBT)
Low	No operation	On
Low	Operation	Off
High	-	Off

10.2 Fault Detection

(1) When a fault is detected at the high side, only the detected arm stops its output.

At that time the detected arm outputs an alarm.

上アームで異常を検出した場合、検出したアームのみ出力を停止します。

この場合、検出したアームはアラームを出力します。

(2) When a fault is detected at the low side, all the lower arms stop their outputs and the alarm signals are outputed from lower arms.

下アーム回路で異常が発生した場合、

下アーム全ての出力を停止し、下アームからアラームを出力します。

(3) An alarm is output only once. The output period is dependent on cause of fault.

アラームは1回のみ出力されます。また、出力期間 (tALM) は異常内容によって異なります。

	Cause of fault	Operation of IGBT				Alarm Output			
		U-phase	V-phase	W-phase	Low side	ALMU	ALMV	ALMW	ALM
High side U-phase	OC	OFF	*	*	*	L	H	H	H
	UV	OFF	*	*	*	L	H	H	H
	T_{jOH}	OFF	*	*	*	L	H	H	H
High side V-phase	OC	*	OFF	*	*	H	L	H	H
	UV	*	OFF	*	*	H	L	H	H
	T_{jOH}	*	OFF	*	*	H	L	H	H
High side W-phase	OC	*	*	OFF	*	H	H	L	H
	UV	*	*	OFF	*	H	H	L	H
	T_{jOH}	*	*	OFF	*	H	H	L	H
Low side	OC	*	*	*	OFF	H	H	H	L
	UV	*	*	*	OFF	H	H	H	L
	T_{jOH}	*	*	*	OFF	H	H	H	L

*：Depend on input logic.

※H:High , L:Low

11. Recommendation for design and application

(1) For the control power supply, secure the enough current capacity.
制御電源は、十分な電流容量を確保してください。

(2) For the control power VCC, use four power supplies isolated each.
Connect the aluminum electrolytic capacitors (about 50V/10μF for upper arm and 50V/47μF for lower arm) as close as possible to the control power terminal VCC. These aluminum electrolytic capacitors are used not for smoothing the control power supply but for reducing the impedance of the external wiring.
Using single power supply such as bootstrap may occur the fluctuation of control power supply, so, it is necessary to design the systems considering these phenomenon in advance.
制御電源Vccは、絶縁された4電源を使用してください。
アルミ電解コンデンサ(上アーム:50V/10uF、下アーム:50V/47uF 程度)を、IPMの制御電源端子Vccに出来るだけ近接して実装してください。尚、本コンデンサは制御電源を平滑化する為のものではなく、IPMまでの配線インピーダンス補正用です。
ブートストラップ等の単電源での使用は、制御電圧変動等が予測される為、十分な検討、検証が必要です。

(3) Don't apply noise current to the IPM's control GND line. It causes the malfunction.
IPMの制御GNDラインにノイズ電流を流さないでください。誤動作の原因となります。

(4) At the external circuit, connections of GNDU to the main terminal U-phase, GNDV to V-phase, GNDW to W-phase, and GND to N1 or N2 -phase are prohibited. It causes the malfunction.
制御端子GNDUと主端子U、制御端子GNDVと主端子V、制御端子GNDWと主端子W、制御端子GNDと主端子N1もしくはN2を外部回路で接続しないでください。誤動作の原因になります。

(5) In case of existence of disuse phase (ex. single phase use or disuse of DB phase), pull up the logic input and alarm signal output terminals of these disuse phase to VCC.
IPMを単相にて使用する場合やブレーキ内蔵タイプにてブレーキを使用しない場合は、使用しない相も制御電源を供給し、入力端子(Vin)、アラーム出力端子(ALM)共にVccへプルアップしてください。入力端子(Vin)オープン状態で制御電源を立ち上げた場合、アラーム出力状態となります。

(6) In designing, make sure that the capacity of primary side current of optocoupler is enough, considering the CTR of optocoupler. In case of the input forward current is not sufficient, input signals of IPM become instability and IPM may occur miss operation.
フォトカプラの一次側電流は、お使いのフォトカプラのCTRを考慮し十分に余裕をもった設計にしてください。
一次電流が不足している場合、IPM入力信号が不安定となり、誤動作の原因となります。

(7) In case of connecting the DC bus line or capacitors to the main terminals, use the paired terminals (P1-N1 or P2-N2). Unpaired connection such as P1-N2 or P2-N1 may cause the malfunction.
To suppress the surge voltage among all the terminals [P1-(U,V,W,B) , P2-(U,V,W,B) , (U,V,W,B)-N1 , (U,V,W,B)-N2] below at maximum rating, reduce the inductance at the DC bus of P1-N1 or P2-N2 circuit and connect some capacitors between the P1 and N1, P2 and N2 terminals.Use capacitors with good high frequency characteristics.
直線母線やコンデンサを主端子に接続する場合は、P1-N1, P2-N2のペア端子を使用してください。
P1-N2, P2-N1のようなペアでの接続は、誤動作の原因となる可能性があります。
P1-N1、もしくはP2-N2間の直流母線は出来るだけ低インダクタンス化し、P1-N1、P2-N2端子間にコンデンサを接続するなどしてサージ電圧を全ての端子間[P1-(U,V,W,B) , P2-(U,V,W,B) , (U,V,W,B)-N1 , (U,V,W,B)-N2]にて、最大定格以下に低減してください。
スナバコンデンサには高周波数特性の良いものを選んでください。

(8) The assurance of solderability in control terminals is within once.Soldering in more than twice is out of quality assurance.
本製品の制御端子部分のハンダ付け性保証回数は1回です。付け直し等による2回以上の回数のハンダ付け性は保証の対象外です。

(9) To estimate the chip temperature accurately, measure the case temperature just under the power chips and sum up the calculated ΔTj-c to the case temperature.
チップ温度推定には、必ずチップ直下のケース温度を測定し、これに計算より求めたΔTj-cを加えて行ってください。

(10) In case of mounting this product on cooling fin, use thermal compound to secure thermal conductivity. If the thermal compound amount was not enough or its applying method was not suitable, its spreading will not be enough, then, thermal conductivity will be worse and thermal run away destruction may occur. The recommended thickness of thermal compound is 100μm. In the applying, confirm the spreading state of thermal compound.
(Spreading state of the thermal compound can be confirmed by removing this product after mounting.)
素子を冷却フィンに取り付ける際には、熱伝導を確保するためのコンパウンド等をご使用ください。又、塗布量が不足したり、塗布方法が不適切な場合、コンパウンドが十分に素子全体に広がらず、放熱悪化による熱破壊に繋がる事があります。コンパウンドの塗布厚は100umを推奨しますが、塗布する際には製品全面にコンパウンドが広がっている事を確認してください。
(実装した後に素子を取りはずすとコンパウンドの広がり具合を確認する事が出来ます。)

(11) This product is designed on the assumption that it applies to an inverter use. Sufficient examination is required at applying to a converter use. Please contact Fuji Electric Co.,Ltd if you would like to apply to converter use.
本製品は、インバータ用途への適用を前提に設計されております。コンバータ用途へ適用される場合は、十分な検討が必要です。もし、コンバータへ適用される場合は御連絡ください。

(12) Design the circuit pattern with shorter wiring from optocoupler to input signal terminals to reduce stray capacity in primary and secondary sides of optocoupler
フォトカプラとIPMの入力端子間の配線は極力短くし、フォトカプラの一次側と二次側の浮遊容量を小さくしたパターンレイアウトにしてください。

(13) A ceramic capacitor(about 0.1μF) should be connected from pin Vcc to GND to stabilize the operation of high speed optocoupler. The total lead length between capacitor and optocoupler is recommended within 1cm.
フォトカプラの安定動作のため、Vcc-GND間に0.1μF程度のセラミックコンデンサを接続してください。
コンデンサとフォトカプラのループ配線長は、出来るだけ1cmを超えないようにしてください。

(14) For the high-speed optocoupler, use high-CMR type with tpHL, tpLH ≦ 0.8μs.
高速フォトカプラは、tpHL,tpLH≦0.8μs、高CMRタイプをご使用ください。

(15) For the alarm output circuit, use low-speed type optocoupler with CTR ≧ 100%.
アラーム出力回路は、低速フォトカプラCTR≧100%のタイプをご使用ください。

(16) Design the control board considering the external noise
制御基板は、外来ノイズの影響を考慮した設計にしてください。

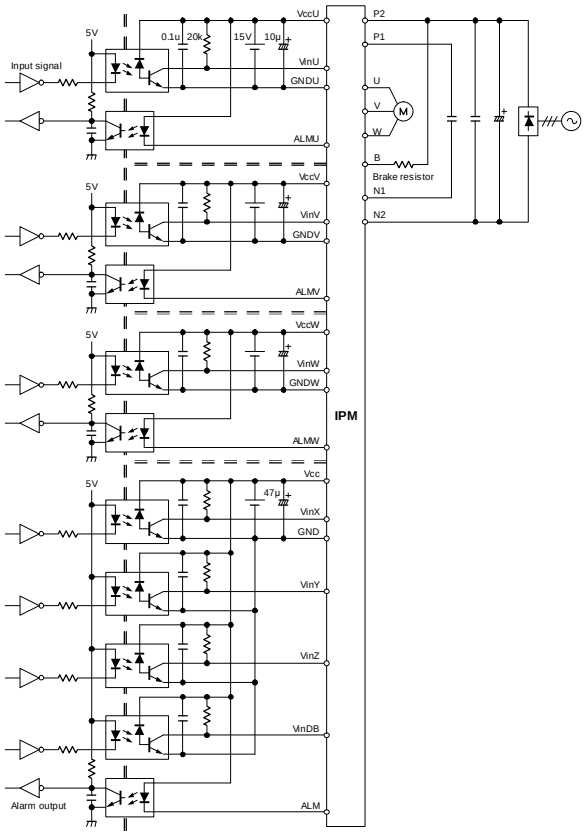
(17) As connecting the capacitor between the input terminal and GND, the response time of secondary side of optocoupler will be delayed compared with the primary side input. So in designing, consider these points.
入力端子-GND間にコンデンサを接続すると、フォトカプラ一次側入力信号に対する応答時間が長くなりますのでご注意ください。

(18) To prevent noise intrusion from the AC lines, connect a capacitor of about 4700pF between the each three-phase lines and the ground.
ACラインからのノイズ侵入を防ぐために、3相各線－アース間に4700pF程度のコンデンサを接続してください。

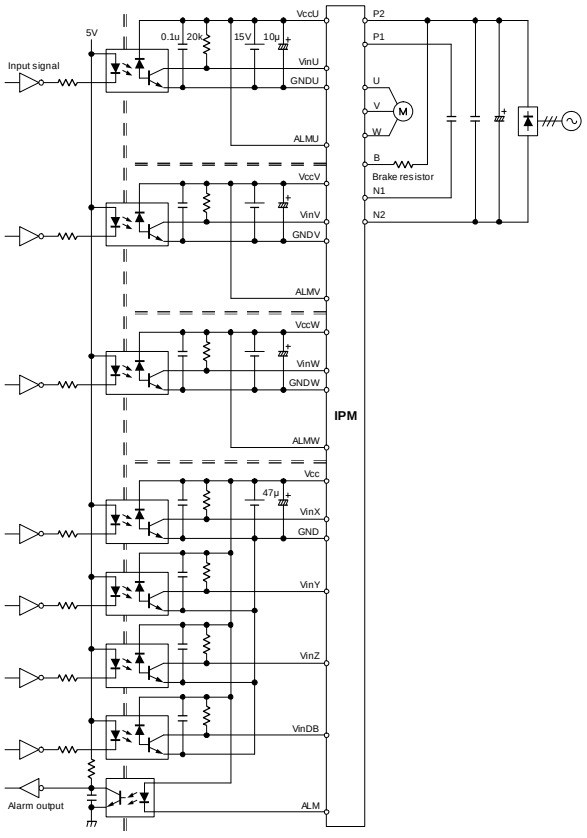
(19) Use this product with keeping the cooling fin's flatness between screw holes within ±50μm per 100mm and the roughness within 10μm. Also keep the tightening torque within the limits of this specification. Too large convex of cooling fin may cause isolation breakdown and this may lead to a critical accident. On the other hand, too large concave of cooling fin makes gap between this product and the fin wider, then, thermal conductivity will be worse and over heat destruction may occur.
冷却フィンはネジ取り付け位置間で平坦度を100mmで±50μm以下、表面の粗さは10μm以下を推奨します。過大な凸反りは本製品の絶縁破壊を起こし、重大事故に発展する場合があります。また、過大な凹反りやゆがみ等は、本製品と冷却フインの間に空隙が生じて放熱が悪くなり、熱破壊に繋がることがあります。

(20) Please see the 『IGBT-IPM APPLICATION MANUAL』 and『IGBT MODULES APPLICATION MANUAL』.
『IGBT-IPM **アプリケーションマニュアル』及び『IGBTモジュール アプリケーションマニュアル』を御参照ください。**

12.Example of applied circuit



(a) In case of use of high-side alarm



(b) In case of no use of high-side alarm

13. Packing and Label

Please see the packing specification of IPM (Technical Rep. No. : MT6M8302).

IPM **梱包仕様書**MT6M8302**を御参照ください。**

14. Cautions for storage and transportation

- Store the IPM at a standard temperature and humidity. (5 to 35**℃**, 45 to 75%)
  Be careful to solderability of the terminals if the IPM has passed over one year from manufacturing date, under the above storage condition.
  常温･常湿保存が望ましい。(5~35**℃**, 45~75%)
  本保存条件下で、製造から1年以上経過した場合は、端子はんだ付け性に十分注意する事。
- Avoid a sudden change in ambient temperature to prevent condensation on the module surfaces.
  モジュールの表面が結露しないよう、急激な温度変化を避けて下さい。
- Avoid places where corrosive gas generates or much dust exists.
  腐食性ガスの発生場所、粉塵の多い場所は避けて下さい。
- Store the module terminals under unprocessed conditions
  モジュールの端子は未加工の状態で保管すること。.
- Avoid physical shock or falls during the transportation.
  運搬時に衝撃を与えたり落下させないで下さい。

15. Scope of application

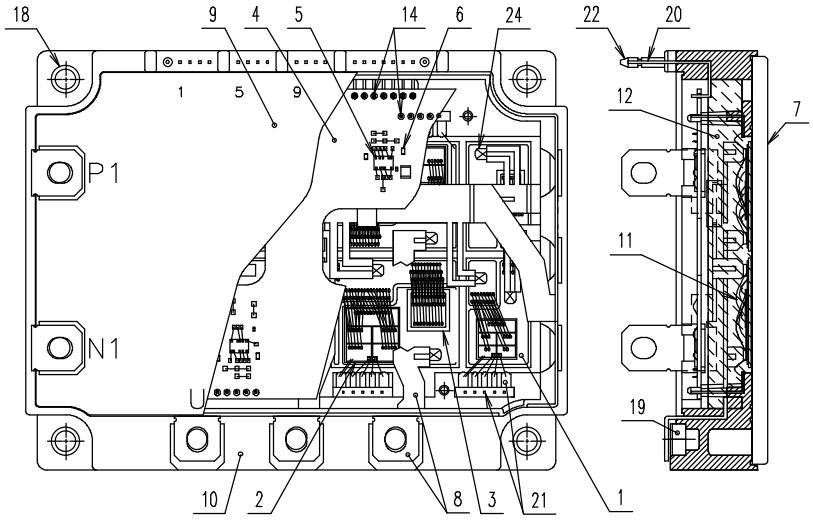
This specification is applied to the IGBT-IPM (type: 7MBP400VEA060-50)

本仕様書は、IGBT-IPM (**型式**:7MBP400VEA060-50)**に適用する。**

16. Based safety standards

UL1557

17. List of materials



※This figure doesn't show the chip size and chip layout exactly. For only explanation of materials.
本図は、材料説明のための図であり、正確なチップサイズやレイアウトを表記したものではありません。

(Total weight of soldering material (typ.) : 18.9g)

No.	Parts	Material (main)	Ref.
1	Isolation substrate	ALN + Cu	
2	IGBT chip	Silicon	
3	FWD chip	Silicon	
4	Printed Circuit Board (PCB)	Glass reinforced Epoxy resin	Halogen Free
5	IC chip	Silicon	
6	Capacitor chip	Ceramics	Ni-Sn plating (External electrode) PbO ※ (Internal electrode)
7	Base plate	Cu	Ni plating (External)
8	Main terminal	Cu	Ni plating (External)
9	Lid	PPS resin	UL 94V-0
10	Case	PPS resin	UL 94V-0
11	Wiring	Aluminum	
12	Silicone gel	Silicone gel	
13	Adhesive (Case)	Silicone resin	(Not drawn in above)
14	Solder (PCB)	Sn/Ag base(Pb Free)	
15	Solder (Under chip)	Sn/Ag base(Pb Free)	(Not drawn in above)
16	Solder (Under Isolation substrate)	Sn/Sb base(Pb Free)	(Not drawn in above)
17	Solder (Under electronic parts)	Sn/Ag base(Pb Free)	(Not drawn in above)
18	Ring	SUS	
19	Nut	Fe	Trivalent chromate treatment
20	Control terminal	Brass	Au plating on Ni plating
21	Inner terminal	Brass	Ni plating (External)
22	Guide pin	Brass	
23	Label	PET	(Not drawn in above)
24	Solder between terminal and Isolation substrate	Sn/Ag base(Pb Free)	

*1：PbO is excluded from RoHS directive.

18. RoHS Directive Compliance List of materials

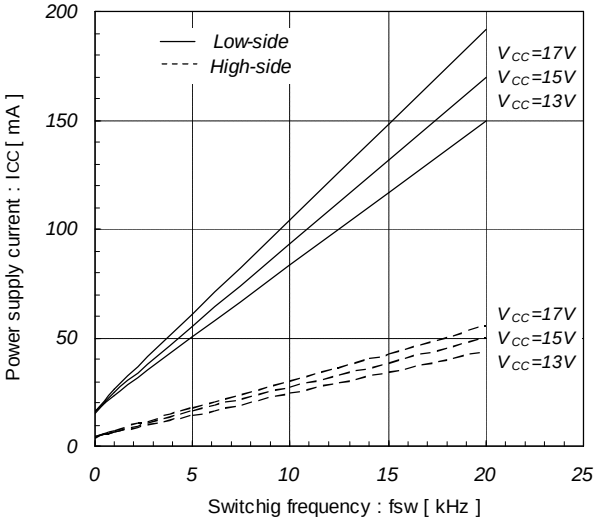
The document (MS5F6209) about RoHS that Fuji Electric issued is applied to this Intelligent Power Module.
The Japanese Edition (MS5F6212) is made into a reference grade.

本IPMは富士電機が発行しているRoHSに関する資料MS5F6209を適用する。
日本語版 (MS5F6212) は参考資料とする。

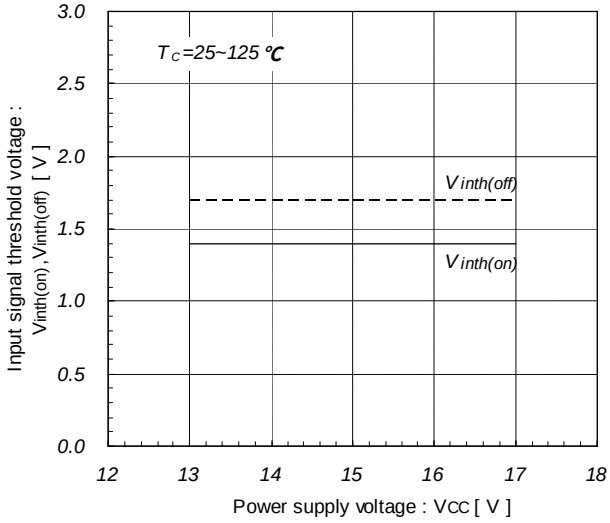
19. Characteristics (Representative)

19-1. Control Circuit

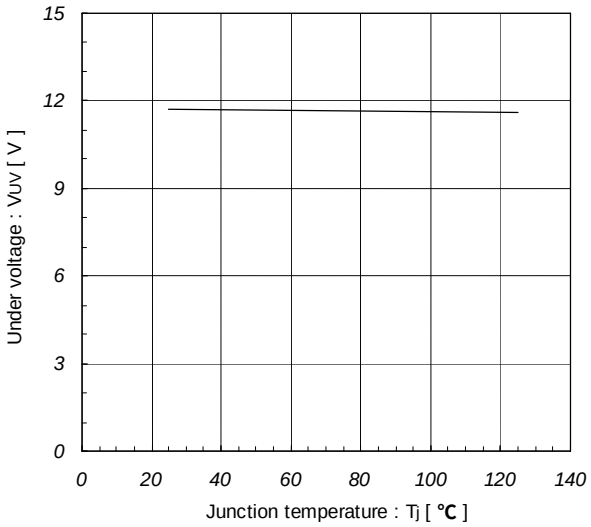
Power supply current vs. Switching frequency
Tj = 25 ℃(typ.)



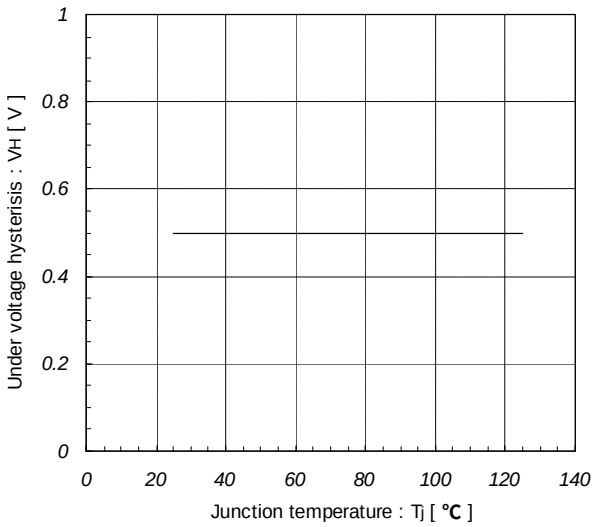
Input signal threshold voltage
vs. Power supply voltage (typ.)



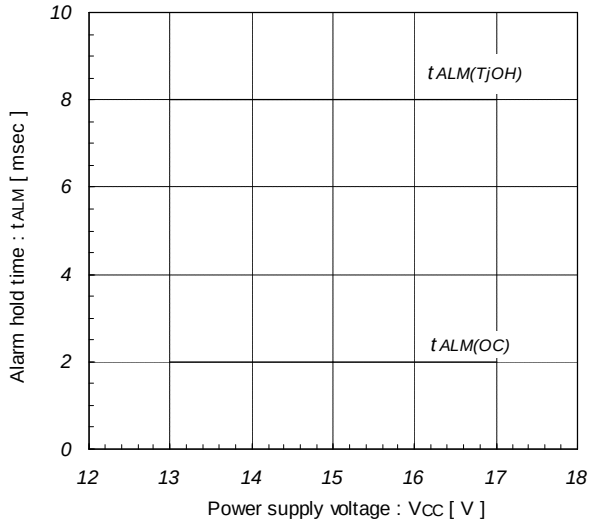
Under voltage vs. Junction temperature (typ.)



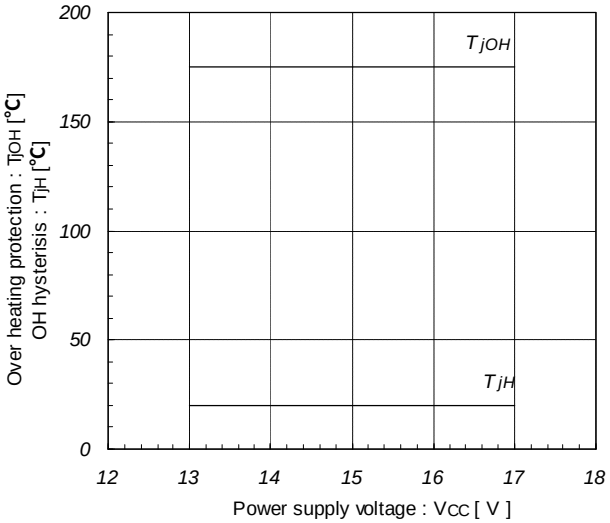
Under voltage hysterisis
vs. Junction temperature (typ.)



Alarm hold time vs. Power supply voltage (typ.)

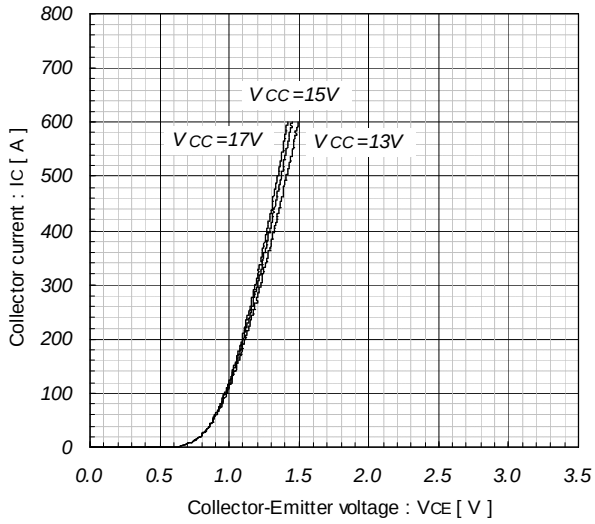


Over heating characteristics
TjOH, TjH vs. VCC (typ.)

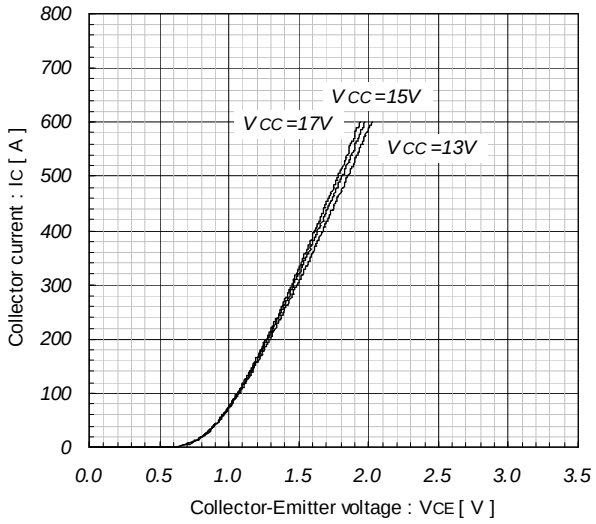


19-2. Inverter

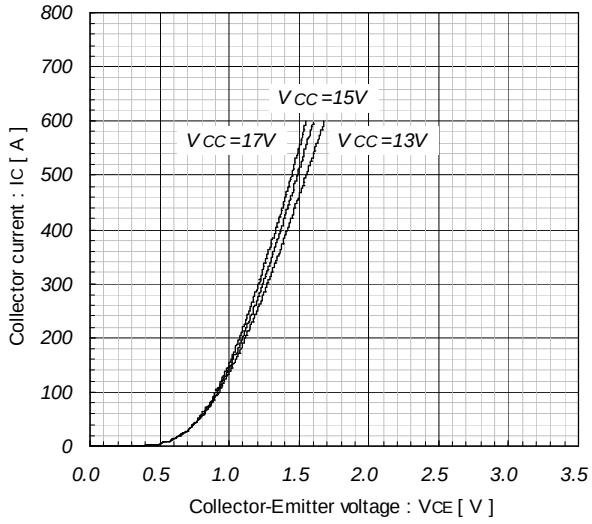
Collector current vs. Collector-Emitter voltage
T_j =25 ℃[Chip] (typ.)



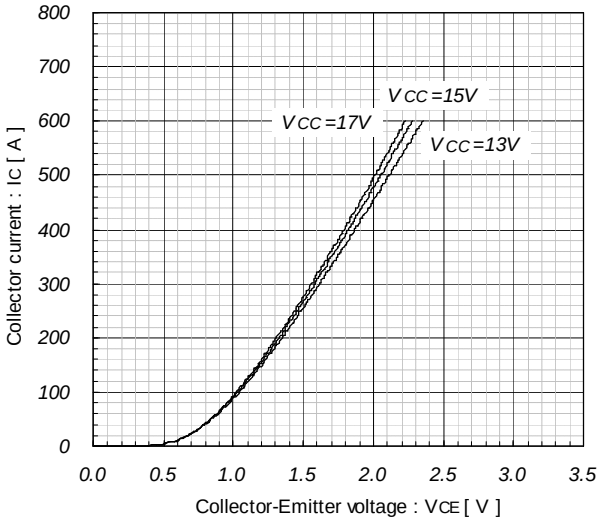
Collector current vs. Collector-Emitter voltage
T_j =25 ℃[Terminal] (typ.)



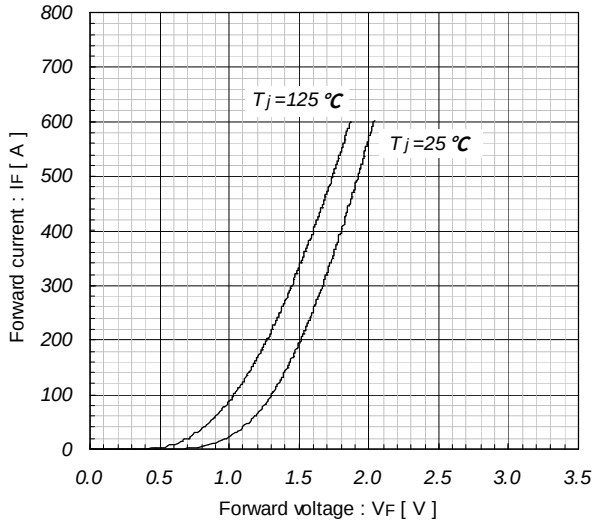
Collector current vs. Collector-Emitter voltage
T_j =125 ℃[Chip] (typ.)



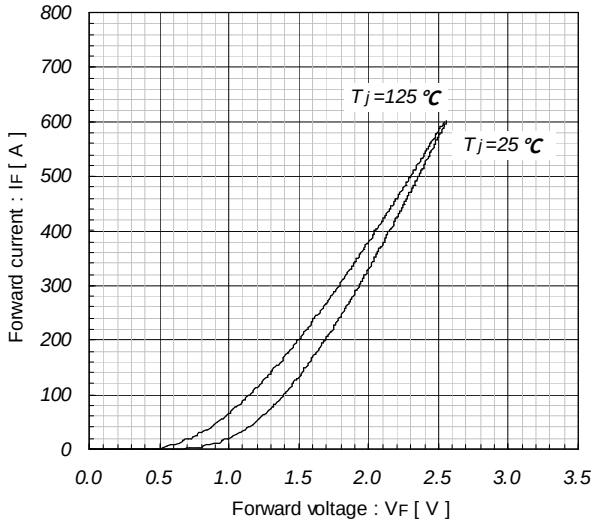
Collector current vs. Collector-Emitter voltage
T_j =125 ℃[Terminal] (typ.)



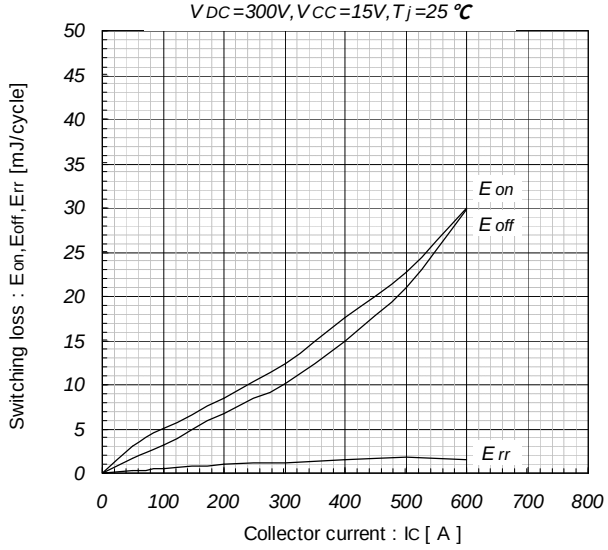
Forward current vs. Forward voltage
[Chip] (typ.)



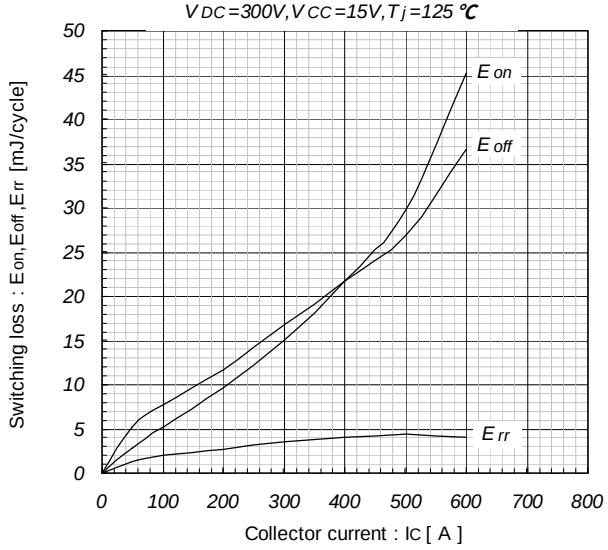
Forward current vs. Forward voltage
[Terminal] (typ.)



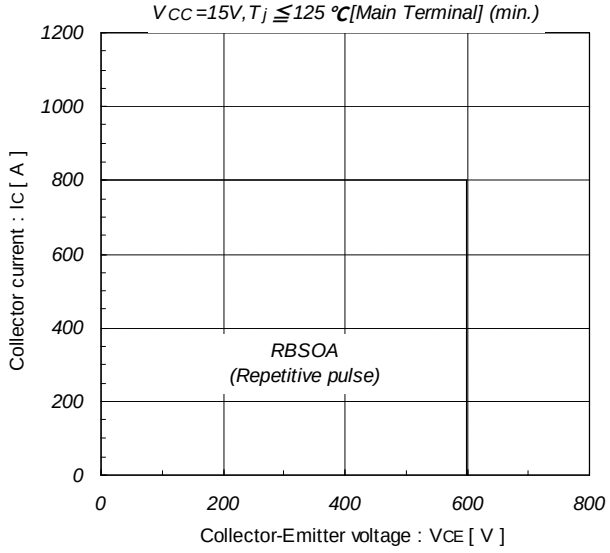
Switching Loss vs. Collector Current (typ.)
V_{DC}=300V, V_{CC}=15V, T_j=25 ℃



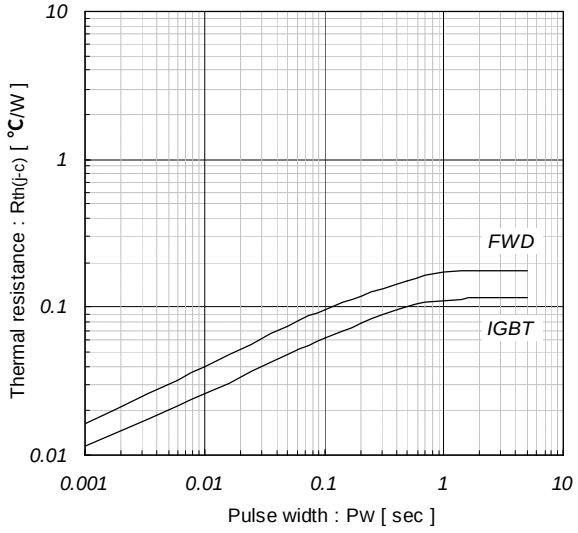
Switching Loss vs. Collector Current (typ.)
V_{DC}=300V, V_{CC}=15V, T_j=125 ℃



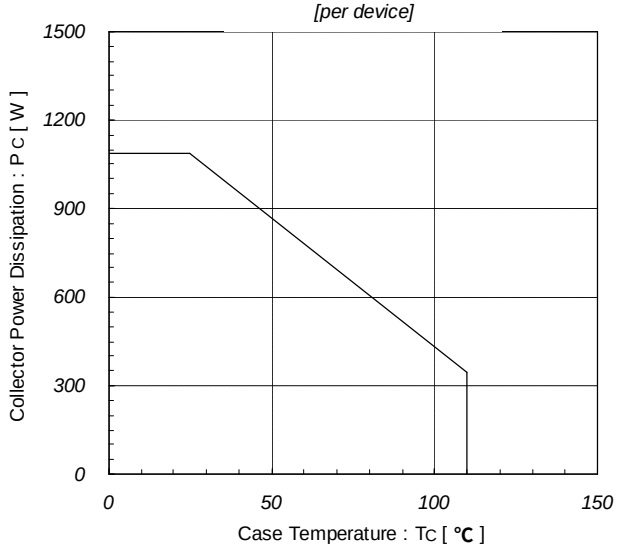
Reversed biased safe operating area
V_{CC}=15V, T_j ≦125 ℃[Main Terminal] (min.)



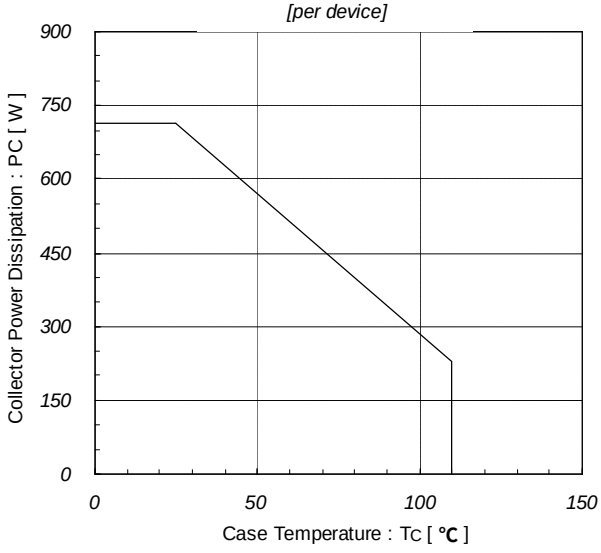
Transient thermal resistance (max.)



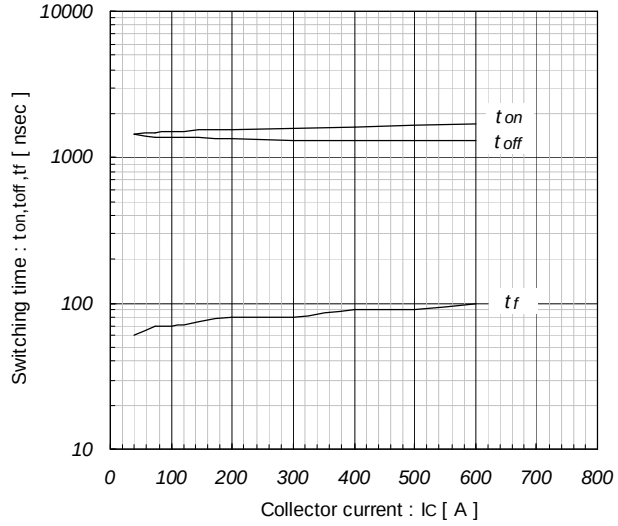
Power derating for IGBT (max.)
[per device]



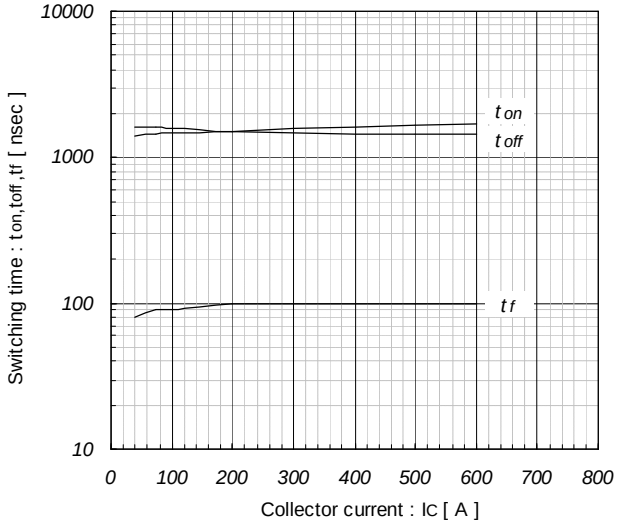
Power derating for FWD (max.)
[per device]



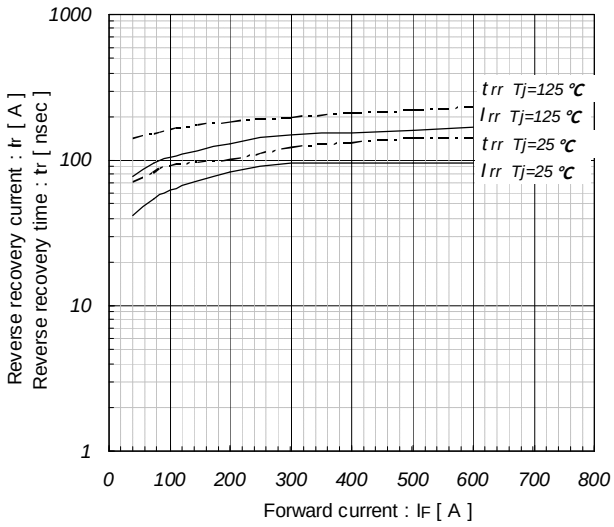
Switching time vs. Collector current (typ.)
V_{DC}=300V, V_{CC}=15V, T_j=25℃



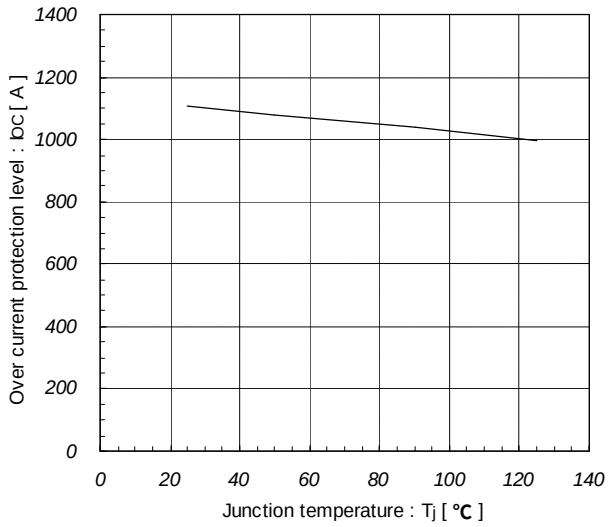
Switching time vs. Collector current (typ.)
V_{DC}=300V, V_{CC}=15V, T_j=125℃



Reverse recovery characteristics (typ.)
trr,Irr vs. If

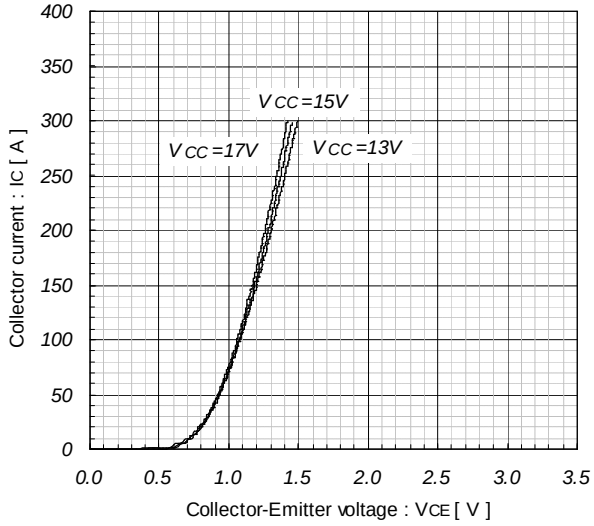


Over current protection vs. Junction temperature (typ.)
V_{CC}=15V

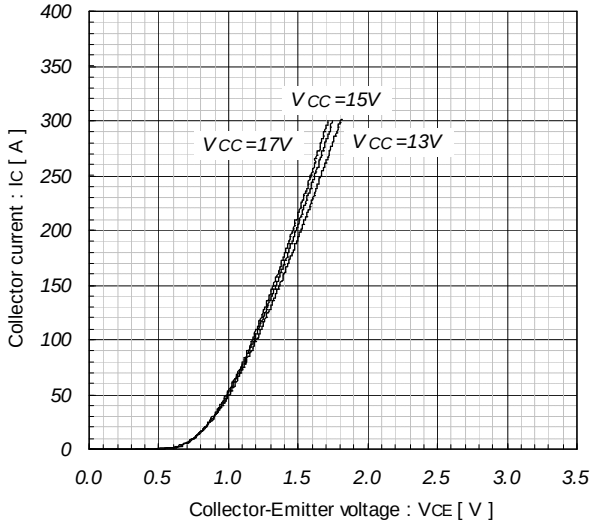


19-3. Brake

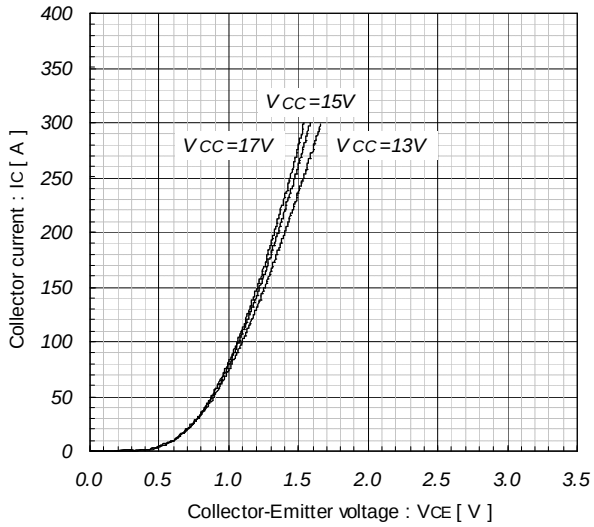
Collector current vs. Collector-Emitter voltage
T_j =25 ℃[Chip] (typ.)



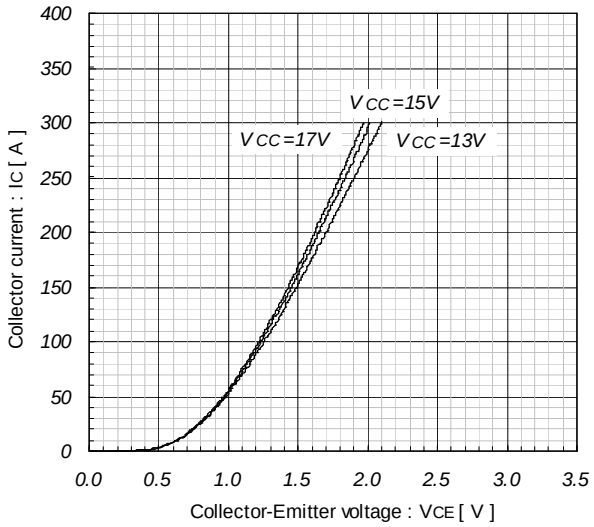
Collector current vs. Collector-Emitter voltage
T_j =25 ℃[Terminal] (typ.)



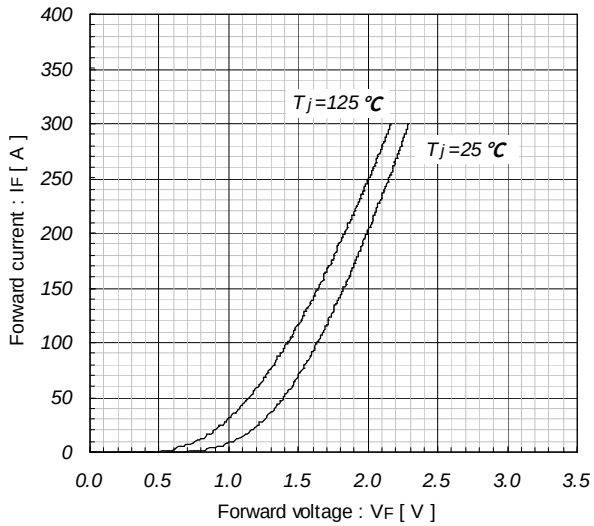
Collector current vs. Collector-Emitter voltage
T_j =125 ℃[Chip] (typ.)



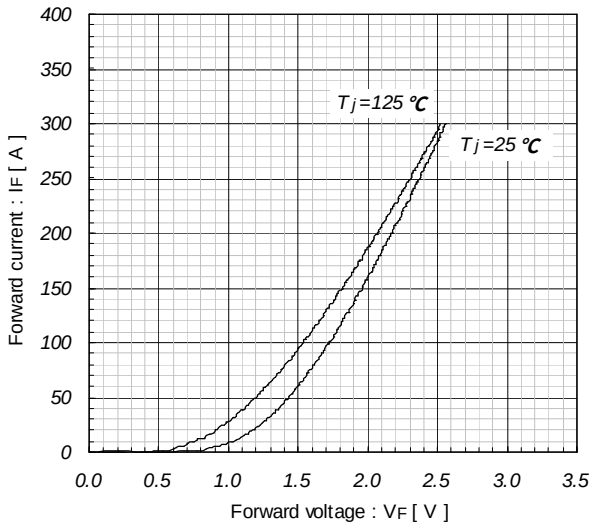
Collector current vs. Collector-Emitter voltage
T_j =125 ℃[Terminal] (typ.)



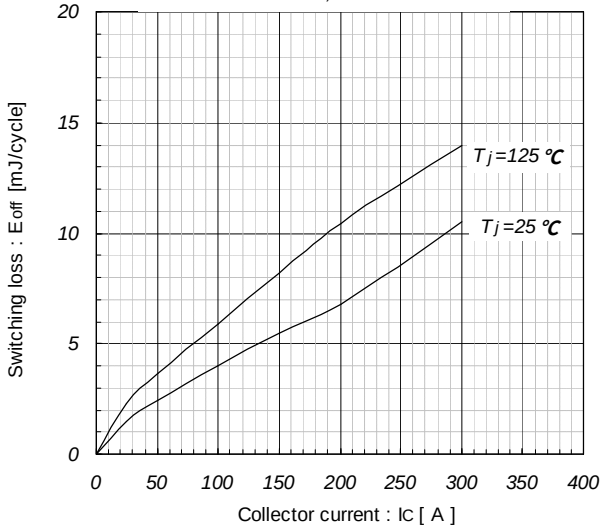
Forward current vs. Forward voltage
[Chip] (typ.)



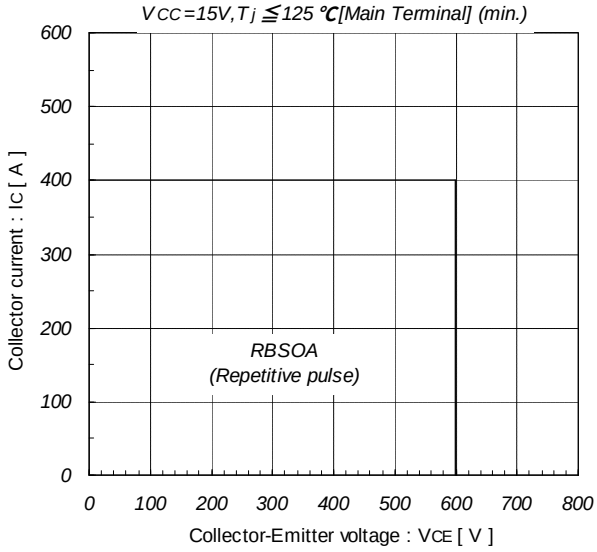
Forward current vs. Forward voltage
[Terminal] (typ.)



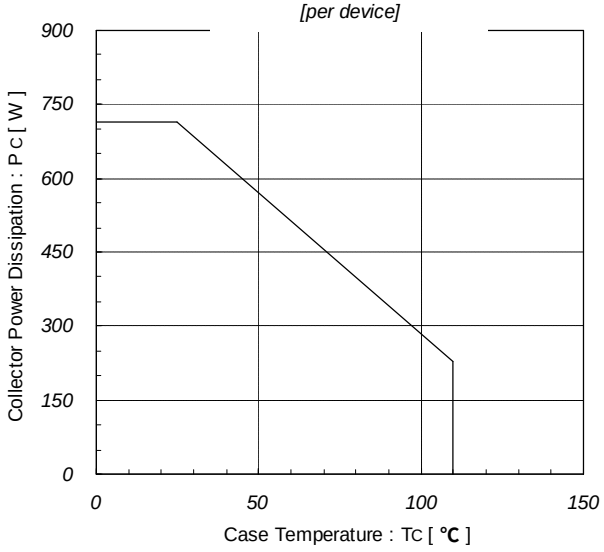
Switching Loss vs. Collector Current (typ.)
V_{DC}=300V, V_{CC}=15V



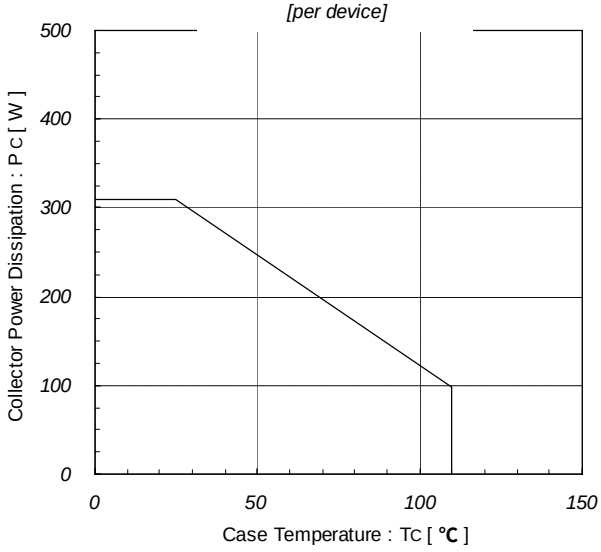
Reversed biased safe operating area
V_{CC}=15V, T_j ≦125 ℃[Main Terminal] (min.)



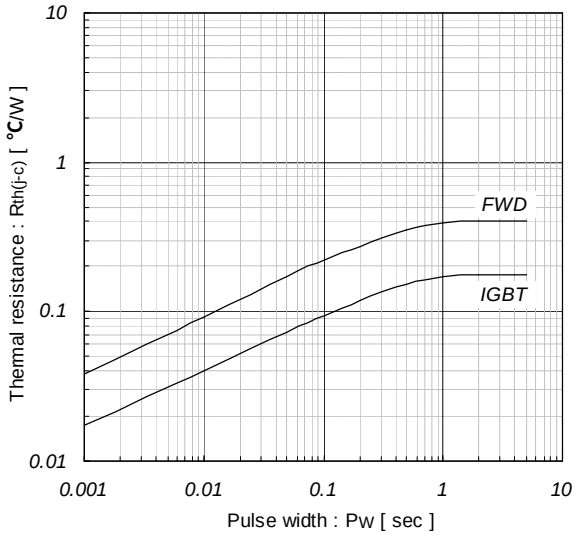
Power derating for IGBT (max.)
[per device]



Power derating for FWD (max.)
[per device]



Transient thermal resistance (max.)



20. Reliability Test

Test conditions and results

Test categories	No.	Test items	Test methods and conditions	Reference norms EIAJ ED-4701	Number of sample	Acceptance number	Number of failure
Mechanical Tests 機械的試験	1	Terminal strength 端子強度 (Pull test)	Pull force : 40 N (main terminal) 10 N (control terminal) Test time : 10 ±1 sec.	Test Method 401 Method Ⅰ	5	(1 : 0)	0
	2	Mounting Strength 締付け強度	Screw torque : 2.5 ~ 3.5 N･m (M5) Test time : 10 ±1 sec.	Test Method 402 Method Ⅱ	5	(1 : 0)	0
	3	Vibration 振動	Range of frequency : 10〜500 Hz Sweeping time : 15 min. Acceleration : 100 m/s^2 Sweeping direction : Each X,Y,Z axis Test time : 6 hr. (2hr./direction)	Test Method 403 Condition code B	5	(1 : 0)	0
	4	Shock 衝撃	Maximum acceleration : 5000 m/s^2 Pulse width 1.0 ms Direction : Each X,Y,Z axis Test time : 3 times/direction	Test Method 404 Condition code B	5	(1 : 0)	0
	5	Solderabitlity はんだ付け性	Solder temp. : 245 ±5 ℃ Immersion duration : 5.0 ±0.5 sec. Test time : 1 time Solder Alloy : Sn-Ag-Cu Each terminal should be Immersed in solder within 1~1.5mm from the body.	Test Method 303	5	(1 : 0)	0
	6	Resistance to soldering heat はんだ耐熱性	Solder temp. : 260 ±5 ℃ Immersion time : 10 ±1sec. Test time : 1 time Each terminal should be Immersed in solder within 1~1.5mm from the body.	Test Method 302 Condition code A	5	(1 : 0)	0
Environment Tests 環境試験	1	High temperature storage 高温保存	Storage temp. : 125 ±5 ℃ Test duration : 1000 hr.	Test Method 201	5	(1 : 0)	0
	2	Low temperature storage 低温保存	Storage temp. : -40 ±5 ℃ Test duration : 1000 hr.	Test Method 202	5	(1 : 0)	0
	3	Temperature humidity storage 高温高湿保存	Storage temp. : 85 ±2 ℃ Relative humidity : 85 ±5% Test duration : 1000hr.	Test Method 103 Test code C	5	(1 : 0)	0
	4	Unsaturated Pressurized Vapor 不飽和蒸気加圧	Test temp. : 120 ±2 ℃ Test humidity : 85 ±5% Test duration : 96 hr.	Test Method 103 Test code E	5	(1 : 0)	0
	5	Temperature cycle 温度サイクル	Test temp. : Minimum storage temp. -40 ±5℃ Maximum storage temp. 125 ±5℃ Normal temp. 5 ~ 35℃ Dwell time : Tmin ~ T_N ~ Tmax ~ T_N 1hr. 0.5hr. 1hr. 0.5hr. Number of cycles : 100 cycles	Test Method 105	5	(1 : 0)	0
	6	Thermal shock 熱衝撃	Test temp. : High temp. side 100^{+0}_{-5} ℃ Low temp. side 0^{+5}_{-0} ℃ Fluid used : Pure water (running water) Dipping time : 5 min. per each temp. Transfer time : 10 sec. Number of cycles : 10 cycles	Test Method 307 Method Ⅰ Condition code A	5	(1 : 0)	0

Test conditions and results

Test categories	No.	Test items	Test methods and conditions	Reference norms EIAJ ED-4701	Number of sample	Acceptance number	Number of failure
Endurance Tests 耐久性試験	1	High temperature reverse bias 高温逆バイアス	Test temp. : Ta = 125 ±5℃ (Tj ≦ 150 ℃) Bias Voltage : VC = 0.8×V_{CES} Bias Method : Applied DC voltage to C-E Vcc = 15V Test duration : 1000 hr.	Test Method 101	5	(1 : 0)	0
	2	Temperature humidity bias 高温高湿バイアス	Test temp. : 85 ±2 ℃ Relative humidity : 85 ±5 % Bias Voltage : VC = 0.8×V_{CES} Vcc = 15V Bias Method : Applied DC voltage to C-E Test duration : 1000 hr.	Test Method 102 Condition code C	5	(1 : 0)	0
	3	Intermitted operating life (Delta-Tj Power cycle) 断続動作	ON time : 2 sec. OFF time : 18 sec. Test temp. : D Tj=100 ±5deg Tj ≦ 150 ℃, Ta=25 ±5℃ Number of cycles : 15000 cycles	Test Method 106	5	(1 : 0)	0

Failure Criteria

Item	Characteristic		Symbol	Failure criteria		Unit
				Lower limit	Upper limit	
Electrical characteristic	Leakage current		I_{CES}	-	USL×2.0	mA
	Saturation voltage		$V_{CE(sat)}$	-	USL×1.2	V
	Forward voltage		V_F	-	USL×1.2	V
	Thermal resistance	IGBT	$R_{th(j-c)Q}$	-	USL×1.2	℃/W
		FWD	$R_{th(j-c)D}$	-	USL×1.2	℃/W
	Over Current Protection		I_{OC}	LSL×0.8	USL×1.2	A
	Alarm signal hold time		t_{ALM}	LSL×0.8	USL×1.2	ms
	Isolation voltage		V_{iso}	Broken insulation		-
Visual inspection	Visual inspection ┌ Peeling Plating └ and the others		-	The visual sample		-

LSL : Lower specified limit.
USL : Upper specified limit.

Note :
Each parameter measurement read-outs shall be made after stabilizing the components at room ambient for 2 hours minimum, 24 hours maximum after removal from the tests.And in case of the wetting tests, for example, moisture resistance tests, each component shall be made wipe or dry completely before the measurement.
信頼性試験後の電気的特性検査及び外観検査は、試験終了後2時間以上、24時間以内室温に放置後行う。又、耐湿性試験や熱衝撃試験のように水分の付着または、内部浸入の可能性のある項目については表面を拭き、エアーブローで表面の水分を除去し、十分に水分が除去された状態で測定する。

Warnings

- This product shall be used within its absolute maximum rating (voltage, current, and temperature). This product may be broken in case of using beyond the ratings.
  製品の絶対最大定格(電圧、電流、温度等)の範囲内で御使用ください。
  絶対最大定格を超えて使用すると、素子が破壊する場合があります。

- Connect adequate fuse or protector of circuit between three-phase line and this product to prevent the equipment from causing secondary destruction.
  万一の不慮の事故で素子が破壊した場合を考慮し、商用電源と本製品の間に適切な容量のヒューズ
  又はブレーカーを必ず付けて2次破壊を防いでください。

- When studying the device at a normal turn-off action, make sure that working paths of the turn-off voltage and current are within the RBSOA specification.
  通常のターンオフ動作における素子責務の検討の際には、ターンオフ電圧・電流の動作軌跡がRBSOA仕様内にあることを確認してください。

- Use this product after realizing enough working on environment and considering of product's reliability life. This product may be broken before target life of the system in case of using beyond the product's reliability life.
  製品の使用環境を十分に把握し、製品の信頼性寿命が満足できるか検討の上、本製品を適用してください。
  製品の信頼性寿命を超えて使用した場合、装置の目標寿命より前に素子が破壊する場合があります。

- If the product had been used in the environment with acid, organic matter, and corrosive gas (For example : hydrogen sulfide, sulfurous acid gas), the product's performance and appearance can not be ensured easily.
  酸・有機物・腐食性ガス(硫化水素, 亜硫酸ガス等)を含む環境下で使用された場合、製品機能・外観などの保証は致しかねます。

- Use this product within the delta-T_j power cycle curve (Technical Rep.No. : MT5Z02525) and the delta-T_C power cycle curve. (Technical Rep.No. : MT5Z02569)
  Power cycle capability is classified to delta-T_j mode which is stated as above and delta-Tc mode. Delta-T_C mode is due to rise and down of case temperature (T_C), and depends on cooling design of equipment which use this product. In application which has such frequent rise and down of T_C, well consideration of product life time is necessary.
  本製品は、ΔT_j**パワーサイクル寿命カーブ(技術資料**No.: MT5Z02525)**と**ΔT_C**パワーサイクル寿命カーブ**
  (技術資料 No.: MT5Z02569)**の範囲内で使ってください。**
  パワーサイクル耐量にはこのΔT_j**による場合の他に、**ΔT_C**による場合があります。これはケース温度(**T_C)**の**
  上昇下降による熱ストレスであり、本製品をご使用する際の放熱設計に依存します。ケース温度の上昇下降が
  頻繁に起こる場合は、製品寿命に十分留意してご使用ください。

- Never add mechanical stress to deform the main or control terminal.
  The deformed terminal may cause poor contact problem.
  主端子及び制御端子に応力を与えて変形させないでください。
  端子の変形により、接触不良などを引き起こす場合があります。

Warnings

- According to the outline drawing, select proper length of screw for main terminal.
  Longer screws may break the case.
  本製品に使用する主端子用のネジの長さは、外形図に従い正しく選定ください。
  ネジが長いとケースが破損する場合があります。

- If excessive static electricity is applied to the control terminals, the devices can be broken.
  Implement some countermeasures against static electricity.
  制御端子に過大な静電気が印加された場合、素子が破壊する場合があります。
  取り扱い時は静電気対策を実施してください。

- Use the latest version Specification and Application Manual every time in case of designing the new equipment.
  新規装置設計の際は、常に最新の仕様書及びアプリケーションマニュアルを適用してください。

Cautions

- Fuji Electric is constantly making every endeavor to improve the product quality and reliability. However, semiconductor products may rarely happen to fail or malfunction. To prevent accidents causing injury or death, damage to property like by fire, and other social damage resulted from a failure or malfunction of the Fuji Electric semiconductor products, take some measures to keep safety such as redundant design, spread-fire-preventive design, and malfunction-protective design.
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- The product described in this specification is not designed nor made for being applied to the equipment or systems used under life-threatening situations. When you consider applying the product of this specification to particular used, such as vehicle-mounted units, shipboard equipment, aerospace equipment, medical devices, atomic control systems and submarine relaying equipment or systems, please apply after confirmation of this product to be satisfied about system construction and required reliability.
  本仕様書に記載された製品は、人命にかかわるような状況下で使用される機器あるいはシステムに用いられることを目的として設計・製造されたものではありません。本仕様書の製品を車両機器、船舶、航空宇宙、医療機器、原子力制御、海底中継機器あるいはシステムなど、特殊用途へのご利用をご検討の際は、システム構成及び要求品質に満足することをご確認の上、ご利用ください。

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