

64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4) 82S25 (O.C.), 3101A (O.C.), 54/74S189 (T.S.)

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature pnp inputs and 1 chip enable line for ease of memory expansion.

During Write, the outputs of each product assume the logic state defined in the truth table.

The family is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N74S189N, N82S25N, and for the military temperature range (-55°C to +125°C) specify S54S189 F or W, S82S25 F or W.

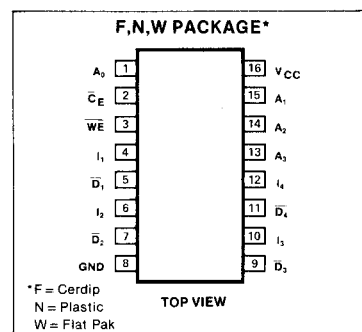
FEATURES

- Output access time:
N82S25: 50ns max
S82S25: 60ns max
N3101A: 35ns max
N74S189: 35ns max
S54S189: 50ns max
- Power dissipation: 6.25mW/bit, typ
- Input loading:
N grade: -100 μ A max
S grade: -150 μ A max
- On-chip address decoding
- Output options:
82S25: Open collector
3101A: Open collector
54/74S189: Tri-state
- Schottky processed
- TTL compatible

APPLICATIONS

- Scratch pad memory
- Buffer memory
- Push down stacks
- Control store

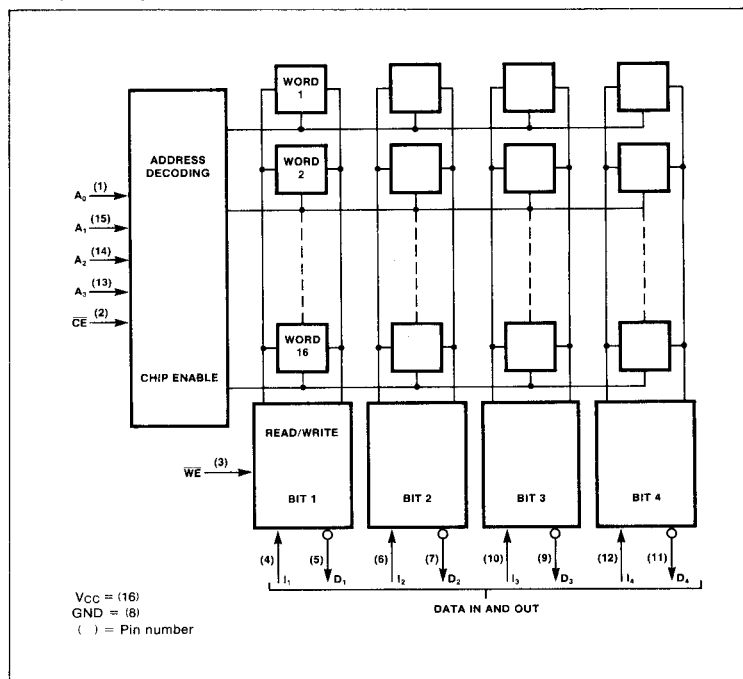
PIN CONFIGURATION



TRUTH TABLE

	$\overline{CE}$	$\overline{WE}$	D_{IN}	82S25	3101A	54/74S189
				DATA OUT		
Read	0	1	X	Stored data	Stored data	Stored data
Write "0"	0	0	0	1	1	Hi-Z
Write "1"	0	0	1	1	1	Hi-Z
Disable	1	X	X	1	1	Hi-Z

BLOCK DIAGRAM

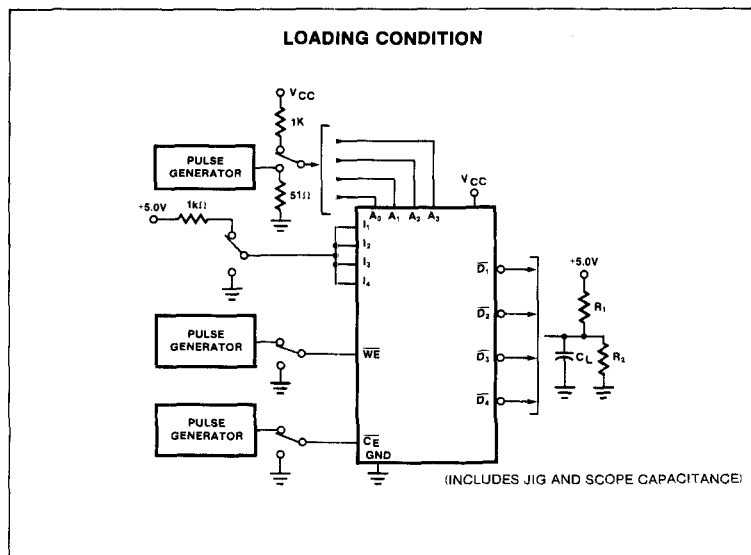
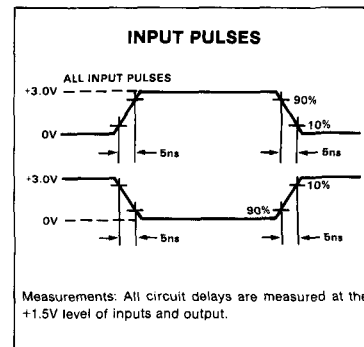


64-BIT BIPOLAR SCRATCH PAD MEMORY (16×4) 82S25 (O.C.), 3101A (O.C.), 54/74S189 (T.S.)**AC ELECTRICAL CHARACTERISTICS** $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, See ac test loadN grade: $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ S grade: $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	N82S25			S82S25			N3101A, N74S189			S54S189			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA Access time					50			60			35			50	ns
TCE Chip enable					35			35			17			25	
TCD Disable time	Output	Chip enable			35			35			17			40	ns
TWD Response time	Output	Write enable			25			30			25			50	ns
TWR Write recovery time					50			60			35			40	ns
TWSA Setup time	Write enable	Address	5			10			0			0			ns
TWHA Hold time			5			10			0			10			
TWSD Setup time		Data in	30			30			25			30			
TWHD Hold time			5			10			0			10			
TWSC Setup time	Write enable	$\overline{\text{CE}}$	0			0			0			0			ns
TWHC Hold time			5			5			0			0			
TWP Pulse width			30			30			25			30			ns
Write enable ⁵															

NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC} .
3. All sense outputs in low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: high = +5.0V, low = GND.
7. Test each input one at a time.

TEST LOAD CIRCUIT**VOLTAGE WAVEFORM**

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PARAMETER ¹		RATING	UNIT
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
V _{OH}	Output voltage High	+5.5	Vdc
T _A	Temperature range Operating		°C
	N grade	0 to +75	
	S grade	-55 to +125	
T _{STG}	Storage	-65 to +150	

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DC ELECTRICAL CHARACTERISTICS
N grade: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S grade: 55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER ⁷		TEST CONDITIONS ⁶	N GRADE			S GRADE			UNIT
			Min	Typ	Max	Min	Typ	Max	
V _{IL}	Input voltage Low ¹	V _{CC} = Min V _{CC} = Max I _{IN} = -12mA, V _{CC} = Min	2.0		.85	2.0		.80	V
V _{IH}	High ¹				-1.5			-1.5	
V _{IC}	Clamp ^{1,7}								
V _{OL}	Output voltage Low ^{2,3,1}	$\overline{CE}$ = Low I _{OUT} = 16mA, V _{CC} = Min I _{OUT} = 2mA	2.4		0.45	2.4		0.5	V
V _{OH}	High (54/74S189) ¹								
I _{IL}	Input current Low	V _{IN} = 0.45V V _{IN} = 5.5V			-100			-150	μA
I _{IH}	High				10			25	
I _{OLK}	Output current Leakage	$\overline{CE}$ = high, V _{OUT} = 5.5V, V _{CC} = Min $\overline{CE}$ = Low V _{OUT} = 0V 2.4 ≥ V _{OUT} ≥ 0.4V			100	-30		100	μA
I _{OS}	Short circuit (54/74S189)				-100			-100	
I _{O(OFF)}	Hi-Z (54/74S189)				±50			±50	
I _{CC}	Supply current ³ 82S25 3101A 54/74S189				105			120	mA
					105			120	
					110			110	
C _{IN}	Capacitance Input	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V, $\overline{CE}$ = high		5			5		pF
C _{OUT}	Output			8			8		

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TIMING DIAGRAMS

