

74LV245AT

Octal bus transceiver; 3-state

Rev. 2 — 4 November 2016

Product data sheet

1. General description

The 74LV245AT is an 8-bit transceiver with 3-state outputs. The device features an output enable (\overline{OE}) and send/receive (DIR) for direction control. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state.

The 74LV245AT is designed to operate over a V_{CC} range from 4.5 V to 5.5 V. The inputs are TTL compatible, which allows the device to be used to translate from 3.3 V to 5 V.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial Power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

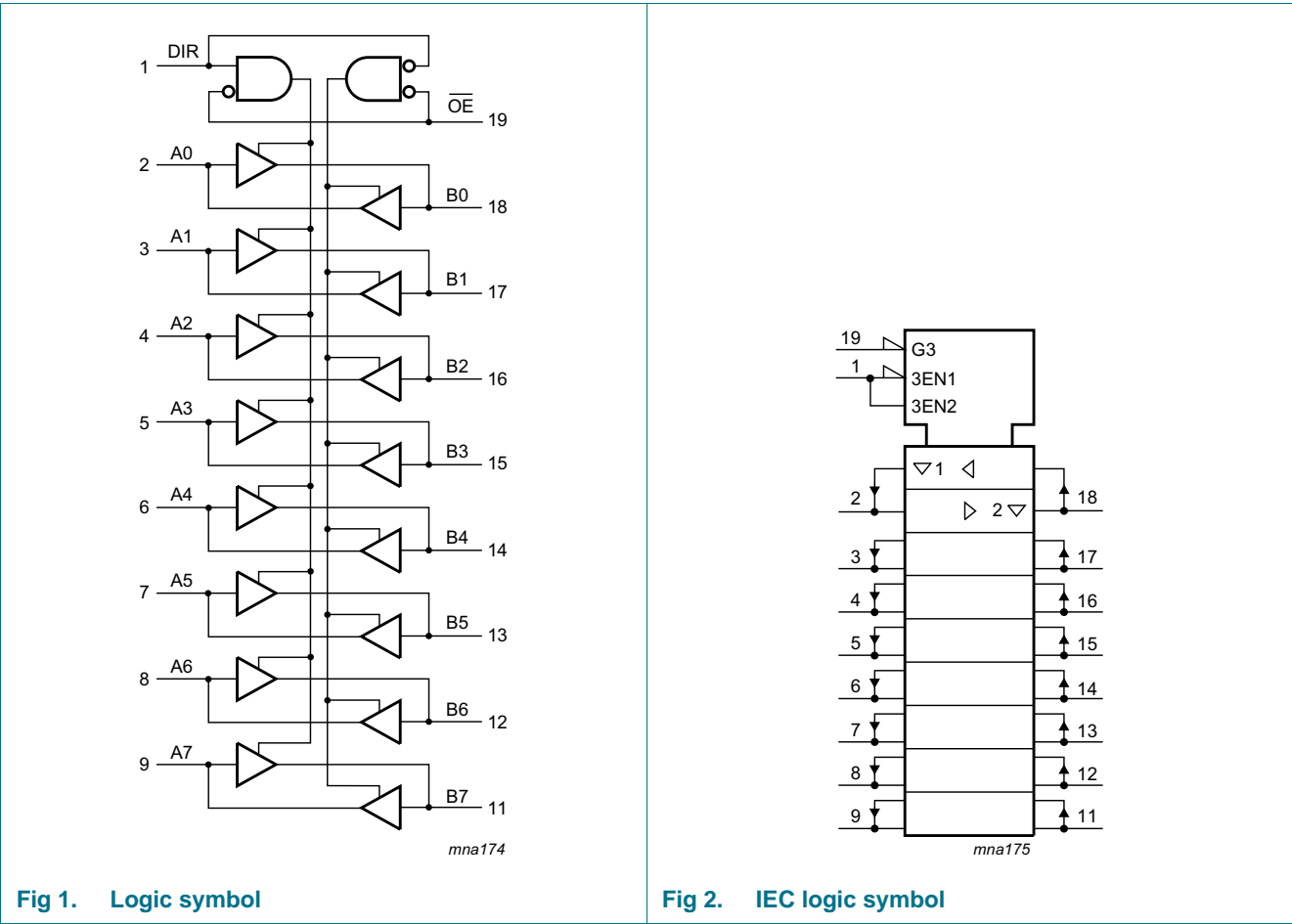
- Direct interface with TTL levels
- Supply voltage range from 4.5 V to 5.5 V
- Typical t_{pd} of 3.1 ns at 5 V
- Typical $V_{OL(p)} < 0.8$ V at $V_{CC} = 5$ V, $T_{amb} = 25$ °C
- Typical $V_{OH(v)} > 2.3$ V at $V_{CC} = 5$ V, $T_{amb} = 25$ °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - ◆ HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3 kV
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 2 kV
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

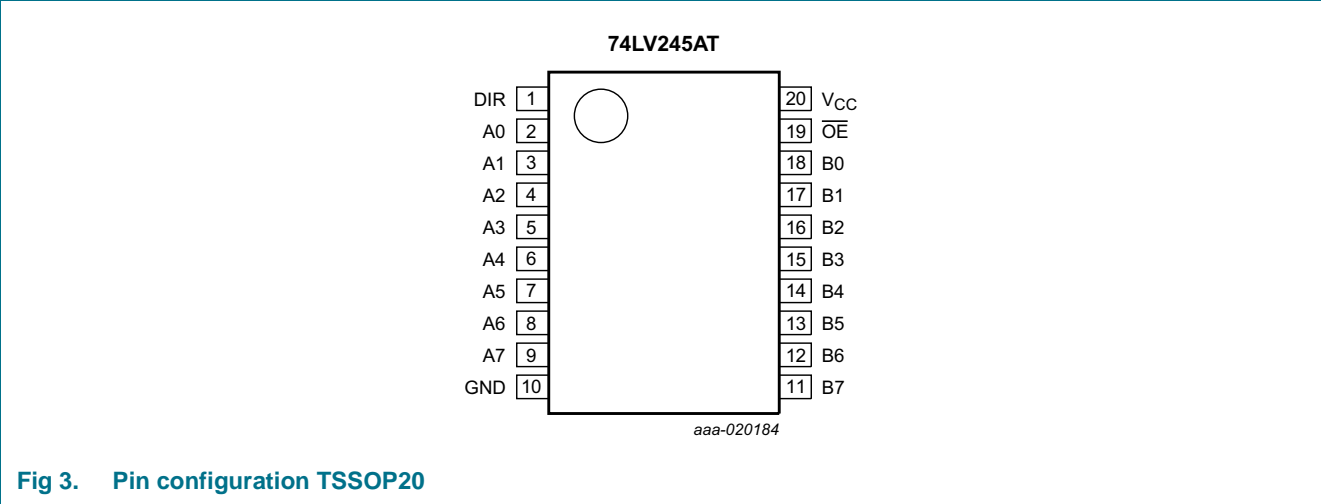
Type number	Package			
	Temperature range	Name	Description	Version
74LV245ATPW	−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0 to B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
$\overline{\text{OE}}$	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table^[1]

Input		Input/output	
OE	DIR	An	Bn
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+7.0	V
V _I	input voltage		−0.5	+7.0	V
V _O	output voltage	active mode	−0.5	V _{CC} + 0.5	V
		power-down or 3-state mode	−0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	−20	-	mA
I _{OK}	output clamping current	V _O < 0 V	−50	-	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		−70	-	mA
T _{stg}	storage temperature		−65	+150	°C
P _{tot}	total power dissipation	T _{amb} = −40 °C to +125 °C	-	500	mW

[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

[3] This value is limited to 7.0 V maximum.

[4] For TSSOP20 package: above 100 °C, the value of P_{tot} derates linearly with 10 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
		power-down or 3-state mode	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2	-	-	2	-	2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5\text{ V}$								
		$I_O = -50\text{ }\mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -16\text{ mA}$	3.94	-	-	3.8	-	3.8	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5\text{ V}$								
		$I_O = 50\text{ }\mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 16\text{ mA}$	-	-	0.44	-	0.55	-	0.55	V
I_{OZ}	OFF-state output current	$V_{CC} = 5.5\text{ V}$; $V_I = V_{IH}$ or V_{IL} ; $V_O = \text{GND to }5.5\text{ V}$	-	-	± 0.25	-	± 2.5	-	± 2.5	μA
I_{OFF}	power-off leakage current	V_I or $V_O = \text{GND to }5.5\text{ V}$; $V_{CC} = 0\text{ V}$	-	-	0.5	-	5	-	5	μA
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 0\text{ V to }5.5\text{ V}$	-	-	± 0.1	-	± 1	-	± 1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 5.5\text{ V}$	-	-	2	-	20	-	20	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = 3.4\text{ V}$; $I_O = 0\text{ A}$; other pins at V_{CC} or GND; $V_{CC} = 5.5\text{ V}$	-	-	1.35	-	1.5	-	1.5	mA

10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V. For test circuit, see Figure 6.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	An to Bn or Bn to An; see Figure 4								
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.1	7.7	1	8.5	1	9.7	ns
		C _L = 50 pF	-	4.4	8.7	1	9.5	1	10.7	ns
t _{en}	enable time	OE to An or OE to Bn; see Figure 5								
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.5	13.8	1	15	1	16.3	ns
		C _L = 50 pF	-	5.8	14.8	1	16	1	17.3	ns
t _{dis}	disable time	OE to An or OE to Bn; see Figure 5								
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.8	7.5	1	8	1	8.6	ns
		C _L = 50 pF	-	6.0	15.4	1	16.5	1	17	ns
t _{sk(o)}	output skew time	V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	-	1	-	1	-	1	ns
C _I	input capacitance	V _I = V _{CC} or GND; V _{CC} = 5 V	-	2	6	-	6	-	6	pF
C _{I/O}	input/output capacitance	V _O = V _{CC} or GND; V _{CC} = 5 V	-	5.5	-	-	-	-	-	pF
C _{PD}	power dissipation capacitance	per buffer; ^[3] C _L = 50 pF; f = 10 MHz; V _I = GND to V _{CC}	-	10.3	-	-	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 5 V.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{pZL} and t_{pZH}.

t_{dis} is the same as t_{pLZ} and t_{pHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

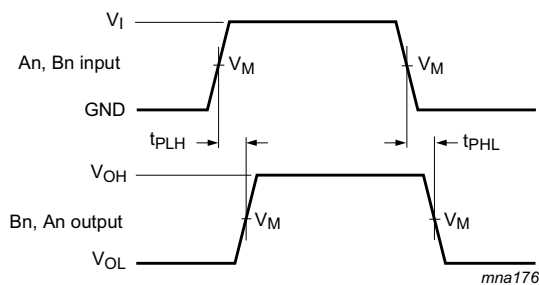
C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts.

Table 8. Noise characteristics
GND = 0 V. For test circuit, see Figure 6.

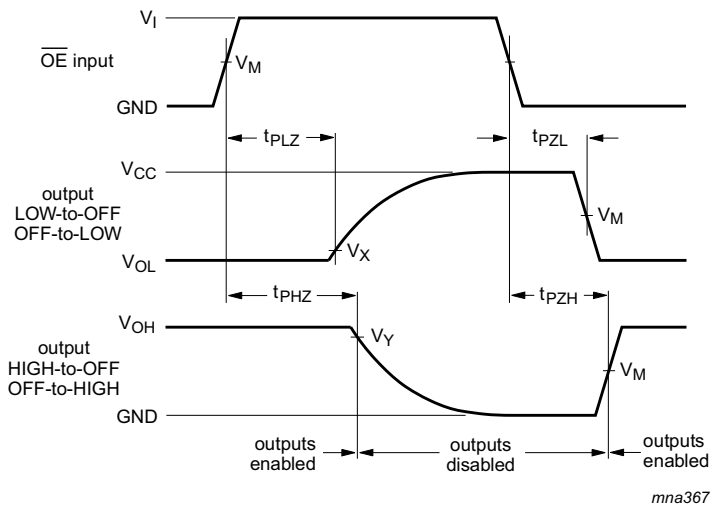
Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
V _{CC} = 5 V; C _L = 50 pF						
V _{OL(p)}	LOW-level output voltage (peak)		-	0.6	1.5	V
V _{OL(v)}	LOW-level output voltage (valley)		−1.5	−0.6	-	V
V _{OH(v)}	HIGH-level output voltage (valley)		-	4.0	-	V
V _{IH(AC)}	AC HIGH-level input voltage	dynamic	2	-	-	V
V _{IL(AC)}	AC LOW-level input voltage	dynamic	-	-	0.8	V

11. Waveforms



Measurement points are given in Table 9.
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 4. Propagation delay input (An, Bn) to output (Bn, An)



Measurement points are given in Table 9.
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Enable and disable times

Table 9. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

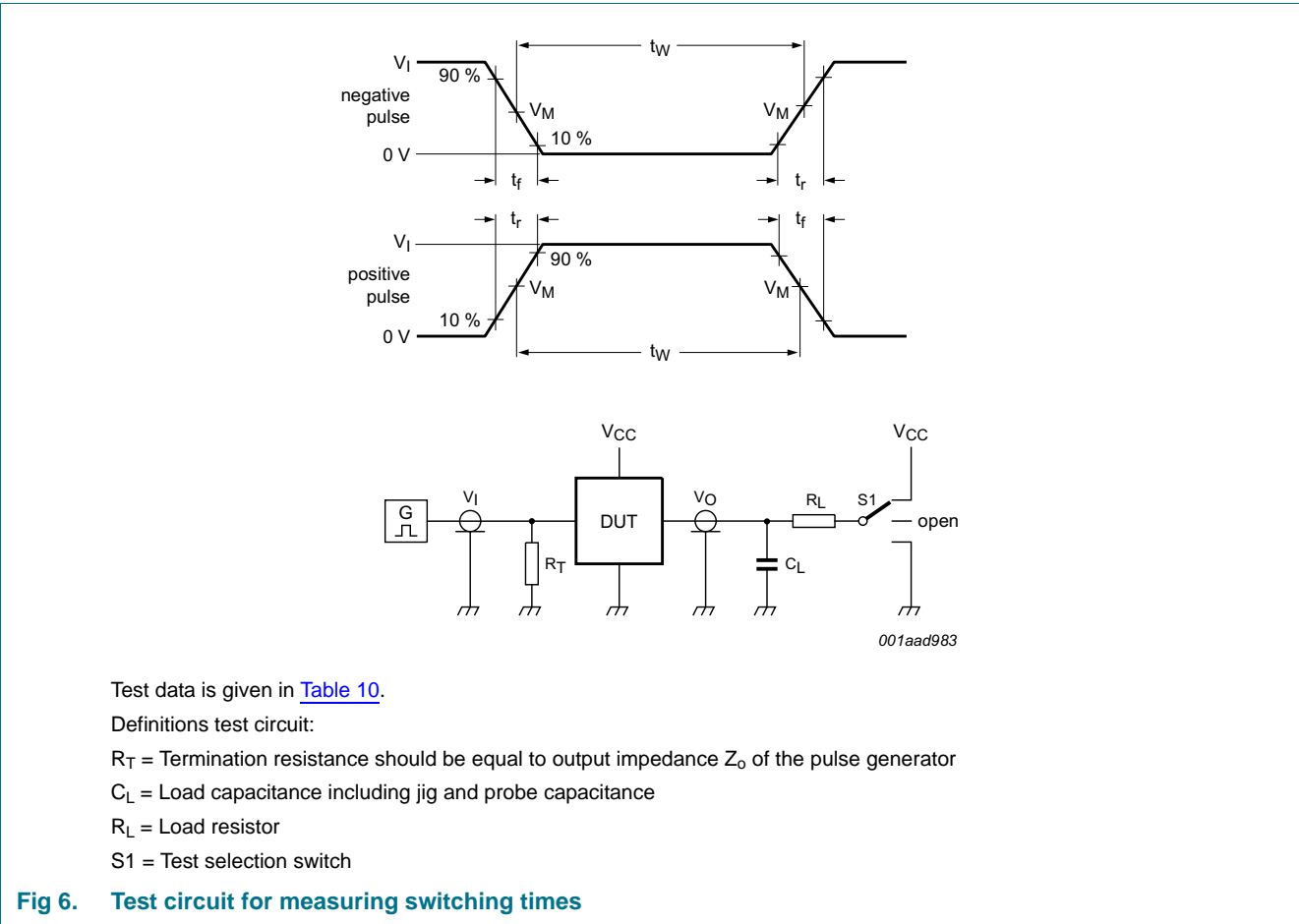


Table 10. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
GND to 3.0 V	3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

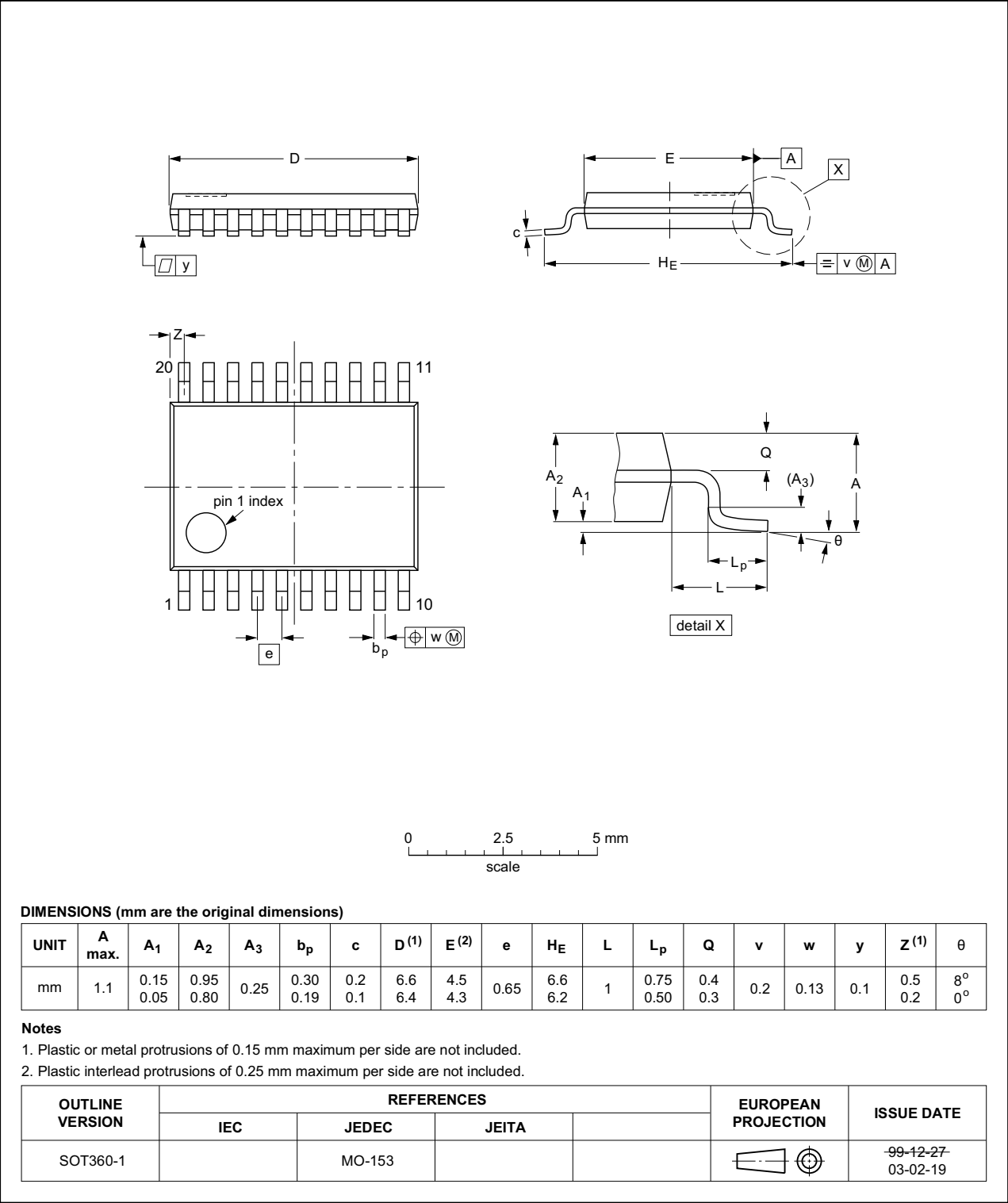


Fig 7. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV245AT v.2	20161104	Product data sheet	-	74LV245AT v.1
Modifications:	• Type number 74LV245ATBQ removed.			
74LV245AT v.1	20160603	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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