Signetics

74LS256
Latch

Dual 4-Bit Addressable Latch
Product Specification

Logic Products

FEATURES

- **Combines dual demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common Clear input**
- **Useful as dual 1-of-4 active HIGH decoder**

DESCRIPTION

The '256 dual addressable latch has four distinct modes of operation and are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{CLR}$ = $\overline{E}$ = LOW), addressed outputs will follow the level of the D inputs, with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS256	19ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS256N
Plastic SO-16	N74LS256D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
$\overline{E}$	Input	2LSul
Other	Inputs	1LSul
All	Outputs	10LSul

NOTE:
A 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

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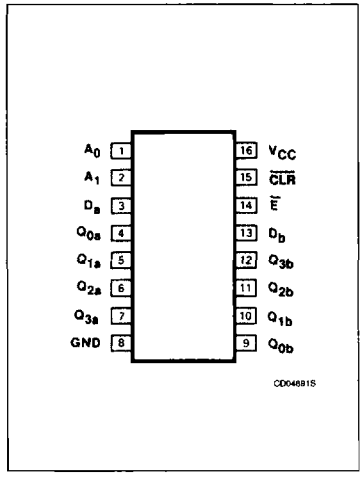
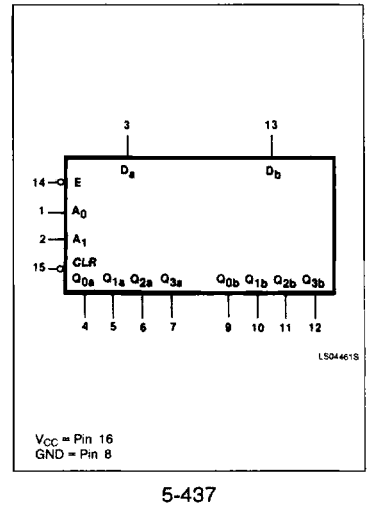
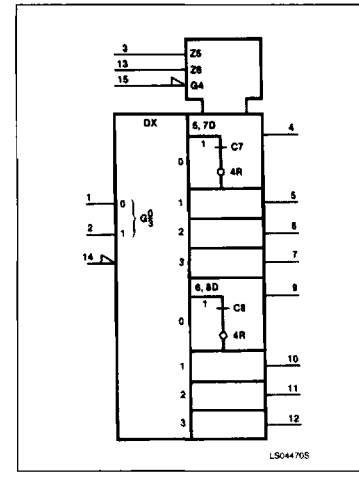
PIN CONFIGURATION



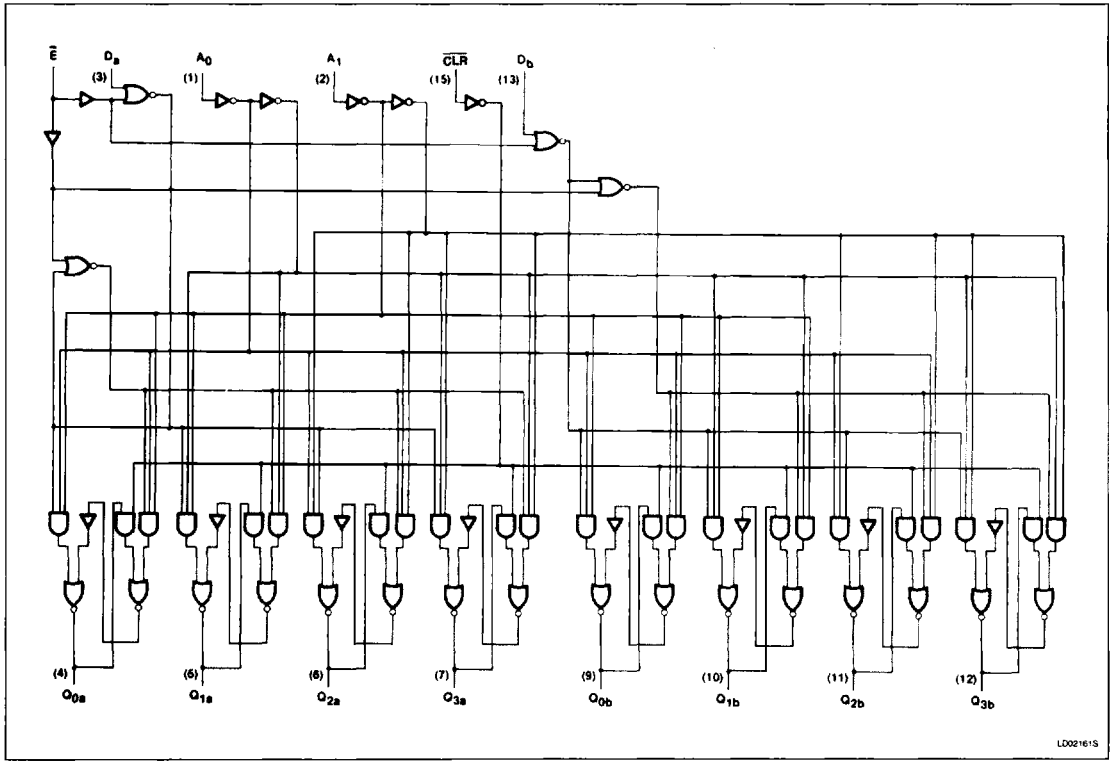
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	$\overline{CLR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3
Clear	L	H	X	X	X	L	L	L	L
Demultiplex (active HIGH) decoder when D = H)	L	L	d	L	L	Q = d	L	L	L
	L	L	d	H	L	L	Q = d	L	L
	L	L	d	L	H	L	L	Q = d	L
	L	L	d	H	H	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	q_0	q_1	q_2	q_3
Addressable latch	H	L	d	L	L	Q = d	q_1	q_2	q_3
	H	L	d	H	L	q_0	Q = d	q_2	q_3
	H	L	d	L	H	q_0	q_1	Q = d	q_3
	H	L	d	H	H	q_0	q_1	q_2	Q = d

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
X = Don't care.
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−400	μA
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74256			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX			0.5	V
			I_{OL} = 4mA			0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	$\overline{E}$ input			40	μA
			Other inputs			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$\overline{E}$ input			−0.8	mA
			Other inputs			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−15		−100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			22	36	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74LS		UNIT
			$C_L = 15pF$, $R_L = 2k\Omega$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1		35 24	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2		32 21	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 3		38 29	ns
t_{PHL}	Propagation delay, Clear to output	Waveform 4		27	ns

AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

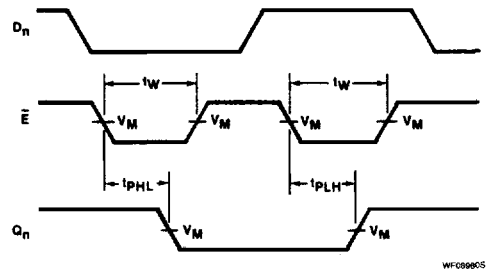
PARAMETER		TEST CONDITIONS	74LS		UNIT
			Min	Max	
t_W	Enable pulse width	Waveform 1	15		ns
t_W	Clear pulse width	Waveform 4	15		ns
$t_S(H)$	Set-up time HIGH, Data to Enable	Waveform 5	15		ns
$t_h(H)$	Hold time HIGH, Data to Enable	Waveform 5	0		ns
$t_S(L)$	Set-up time LOW, Data to Enable	Waveform 5	15		ns
$t_h(L)$	Hold time LOW, Data to Enable	Waveform 5	0		ns
t_S	Set-up time, Address to Enable[a]	Waveform 6	15		ns
t_h	Hold time, Address to Enable[b]	Waveform 6	0		ns

NOTE:

a. The Address to Enable set-up time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

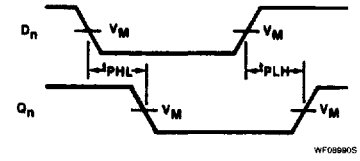
b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC WAVEFORMS



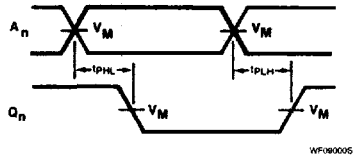
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 1. Propagation Delay Enable To Output And Enable Pulse Width



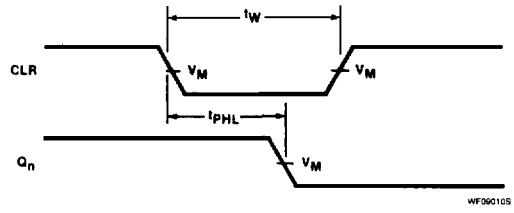
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 2. Propagation Delay Data To Output



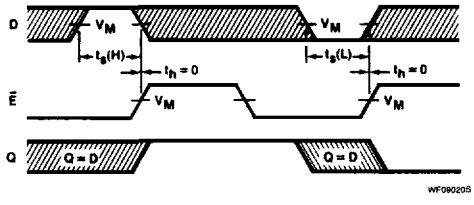
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 3. Propagation Delay Address To Output



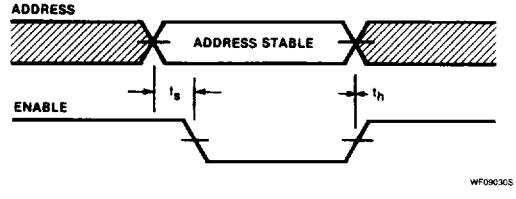
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 4. Clear To Output Delay And Clear Pulse Width



V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5. Data Set-up And Hold Times



V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 6. Address Set-up And Hold Times

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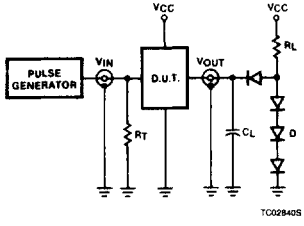
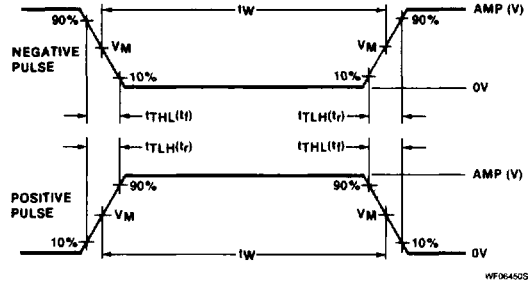
TEST CIRCUITS AND WAVEFORMS





V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns