74HC4075; 74HCT4075

Triple 3-input OR gate Rev. 4 — 4 February 2019

Product data sheet

1. General description

The 74HC4075; 74HCT4075 is a triple 3-input OR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

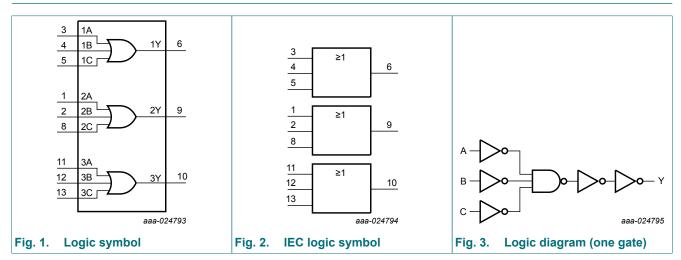
- Complies with JEDEC standard no. 7A
- Input levels:
 - For 74HC4075: CMOS level
 - For 74HCT4075: TTL level
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4075D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1
74HCT4075D			body width 3.9 mm	

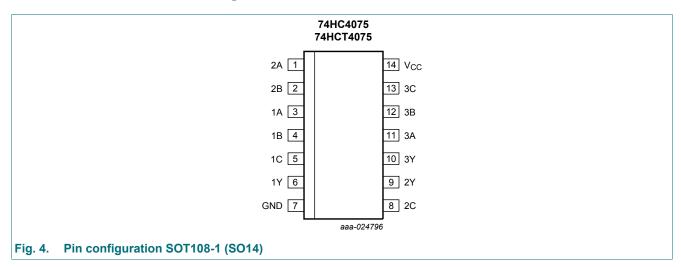
4. Functional diagram





5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A	3, 1, 11	data input
1B, 2B, 3B	4, 2, 12	data input
1C, 2C, 3C	5, 8, 13	data input
1Y, 2Y, 3Y	6, 9, 10	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs	Outputs		
nA	nB	nC	nY
L	L	L	L
X	X	Н	Н
X	Н	X	Н
Н	X	X	Н

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC407	5	7	Unit		
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol Parameter		Conditions	25 °C			-40 ° +85	C to	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC40	75									
V_{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

^[2] For SO14 package: Ptot derates linearly with 8 mW/K above 70 °C.

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		$I_{\rm O}$ = -5.2 mA; $V_{\rm CC}$ = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	2.0	-	20	-	40	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT4	075									
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	8.0	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
lı	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V; $I_O = 0$ A	-	-	2.0	-	20	-	40	μΑ
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V ; $I_O = 0 \text{ A}$								
		nA, nB, nC inputs	-	150	540	-	675	-	735	μΑ
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions			25 °C		-40	0 °C to +	125 °C	Unit
				Min	Тур	Max	Min	Max (85 °C)	Max (125 °C)	
74HC40	75		'				'			
t _{pd}	propagation	nA, nB, nC to nY; see Fig. 5	[1]							
	delay	V _{CC} = 2.0 V		-	28	100	-	125	150	ns
		V _{CC} = 4.5 V		-	10	20	-	25	30	ns
		V _{CC} = 5.0 V; C _L = 15 pF		-	8	-	-	-	-	ns
		V _{CC} = 6.0 V		-	8	17	-	21	26	ns
t _t	transition time	see Fig. 5	[2]							
		V _{CC} = 2.0 V		-	19	75	-	95	110	ns
		V _{CC} = 4.5 V		-	7	15	-	19	22	ns
		V _{CC} = 6.0 V		-	6	13	-	16	19	ns
C _{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC}	[3]	-	28	-	-	-	-	pF
74HCT4	075							'	ı	
t _{pd}	propagation	nA, nB, nC to nY; see Fig. 5	[1]							
	delay	V _{CC} = 4.5 V		-	12	24	-	30	36	ns
		V _{CC} = 5.0 V; C _L = 15 pF		-	10	-	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Fig. 5</u>	[2]	-	7	15	-	19	22	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V	[3]	-	32	-	-	-	-	pF

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

 t_{pd} is the same as t_{PHL} and t_{PLH} . t_{t} is the same as t_{THL} and t_{TLH} . C_{PD} is used to determine the dynamic power dissipation (P_{D} in μ W):

10.1. Waveforms and test circuit

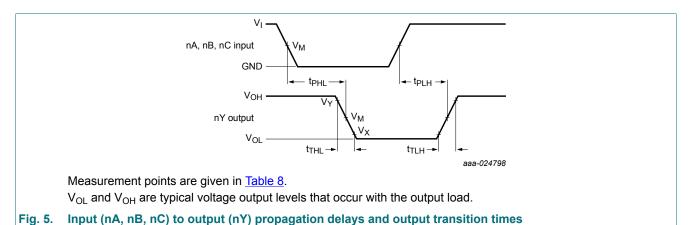
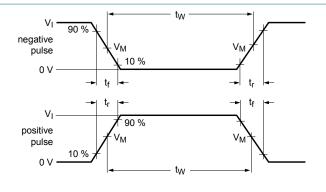
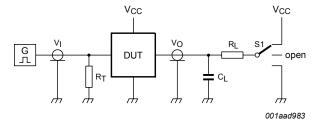


Table 8. Measurement points

Table 0. Measurer	nent points				
Туре	Input	Output			
	V _M	V _M	V _X	V _Y	
74HC4075	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}	
74HCT4075	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}	





Test data is given in Table 9.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 $\ensuremath{\text{C}_{\text{L}}}$ = Load capacitance including jig and probe capacitance.

 R_L = Load resistance.

S1 = Test selection switch

Fig. 6. Test circuit for measuring switching times

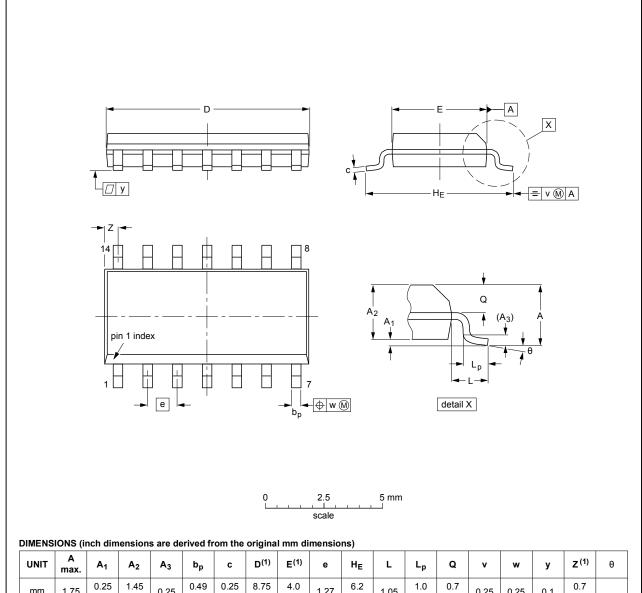
Table 9. Test data

Туре	Input		Load	S1 position	
	V _I	t _r , t _f		R_L	t _{PHL} , t _{PLH}
74HC4075	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT4075	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Fig. 7. Package outline SOT108-1 (SO14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT4075 v.4	20190204	Product data sheet	-	74HC_HCT4075 v.3	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74HCT4075DB (SOT337-1) removed. Type numbers 74HC4075PW and 74HCT4075PW (SOT402-1) removed. 				
74HC_HCT4075 v.3	20161103	Product data sheet	-	74HC_HCT4075 v.2	
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HC4075N and 74HCT4075N removed. 				
74HC_HCT4075 v.2	19901201	Product specification	-	-	

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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