Dual 2-to-4 line decoder/demultiplexer Rev. 4 — 11 December 2015

Product data sheet

#### 1. **General description**

The 74HC139; 74HCT139 decodes two binary weighted address inputs (nA0, nA1) to four mutually exclusive outputs ( $n\overline{Y}0$  to  $n\overline{Y}3$ ). Each decoder features an enable input (nE). When nE is HIGH all outputs are forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V<sub>CC</sub>.

#### **Features and benefits** 2.

- Input levels:
  - For 74HC139: CMOS level
  - For 74HCT139: TTL level
- Demultiplexing capability
- 2 independent 2-to-4 decoders
- Multifunction capability
- Suitable for memory decoding, data routing or code conversion
- Complies with JEDEC standard no. 7A
- Active LOW mutually exclusive outputs
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

#### 3. **Ordering information**

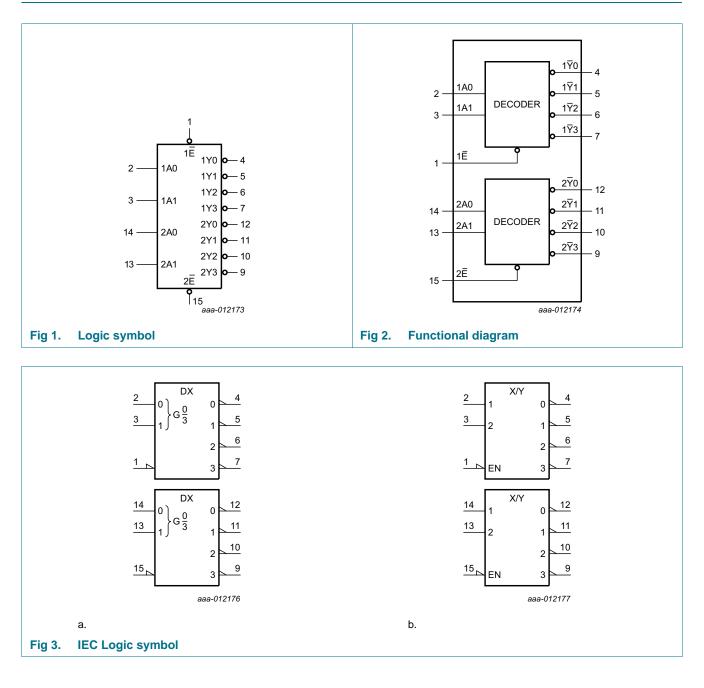
#### Table 1. **Ordering information**

Type number	Package	Package									
	Temperature range	Name	Description	Version							
74HC139D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads;	SOT109-1							
74 HCT139D			body width 3.9 mm								
74HC139DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads;	SOT338-1							
74HCT139DB			body width 5.3 mm								
74HC139PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package;	SOT403-1							
74HCT139PW			16 leads; body width 4.4 mm								

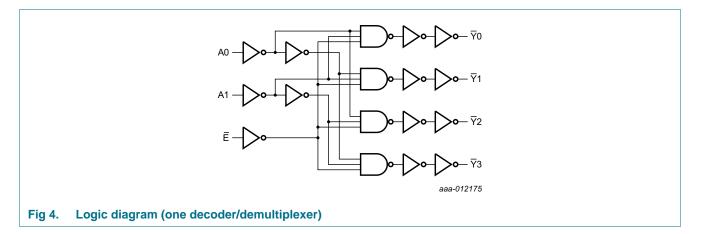


Dual 2-to-4 line decoder/demultiplexer

## 4. Functional diagram

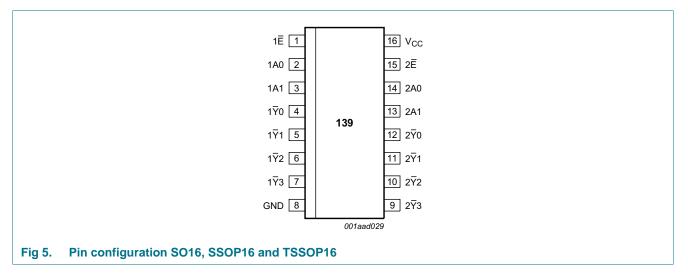


Dual 2-to-4 line decoder/demultiplexer



#### **Pinning information** 5.

### 5.1 Pinning



### 5.2 Pin description

#### Table 2. **Pin description**

Symbol	Pin	Description
1Ē, 2Ē	1, 15	enable input (active LOW)
1A0, 1A1	2, 3	address input
1 <u>7</u> 0, 1 <u>7</u> 1, <u>17</u> 2, <u>17</u> 3	4, 5, 6, 7	output (active LOW)
GND	8	ground (0 V)
2 <u>7</u> 0, <u>2</u> 71, <u>2</u> 72, <u>2</u> 73	12, 11, 10, 9	output (active LOW)
2A0, 2A1	14, 13	address input
V <sub>CC</sub>	16	positive supply voltage

74HC\_HCT139

Dual 2-to-4 line decoder/demultiplexer

## 6. Functional description

#### Table 3.Function table[1]

Control	Input	Input		Output					
nE	nA1	nA0	nY3	nY2	nY1	n¥0			
Н	Х	Х	Н	Н	н	Н			
L	L	L	Н	Н	н	L			
L	L	Н	Н	Н	L	Н			
L	Н	L	н	L	н	Н			
L	Н	Н	L	Н	Н	Н			

[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care.

## 7. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5$ V or $V_{I} > V_{CC} + 0.5$ V		-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O}$ < -0.5 V or $V_{O}$ > $V_{CC}$ + 0.5 V		-	±20	mA
I <sub>O</sub>	output current	$V_{O} = -0.5 \text{ V to} (V_{CC} + 0.5 \text{ V})$		-	±25	mA
I <sub>CC</sub>	quiescent supply current			-	50	mA
I <sub>GND</sub>	ground current			-50	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	SO16 package	<u>[1]</u>	-	500	mW
		SSOP16 package	[2]	-	500	mW
		TSSOP16 package	<u>[2]</u>	-	500	mW

[1] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70  $^\circ C.$ 

[2] For SSOP16 and TSSOP16 packages: Ptot derates linearly with 5.5 mW/K above 60 °C.

Dual 2-to-4 line decoder/demultiplexer

## 8. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC139			74HCT139		
			Min	Тур	Max	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 2.0 V$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5 V$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0 V$	-	-	83	-	-	-	ns/V

## 9. Static characteristics

#### Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>ai</sub>	<sub>nb</sub> = 25	°C	T <sub>amb</sub> = - +85	40 °C to 5 °C		-40 °C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC13	9									
VIH	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	$V_{CC} = 4.5 V$	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}$								
	output voltage	$I_{O} = -20 \ \mu A; \ V_{CC} = 2.0 \ V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_{O} = -20 \ \mu A; \ V_{CC} = 4.5 \ V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -20 \ \mu A; \ V_{CC} = 6.0 \ V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}$								
	output voltage	$I_0 = 20 \ \mu\text{A}; \ V_{CC} = 2.0 \ V$	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 20 \ \mu\text{A}; \ V_{CC} = 4.5 \ V$	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 20 \ \mu A; \ V_{CC} = 6.0 \ V$	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_0 = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
I	input leakage current	$V_I = V_{CC} \text{ or GND};$ $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current		-	-	±0.5	-	±5.0	-	±10.0	μA

Dual 2-to-4 line decoder/demultiplexer

#### Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Tai	<sub>mb</sub> = 25	°C		-40 °C to 5 °C		-40 °C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
I <sub>CC</sub>	supply current		-	-	8.0	-	80	-	160	μA
Cı	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT1:	39									
V <sub>IH</sub>	HIGH-level input voltage	$V_{CC}$ = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	$V_{CC}$ = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
	$I_O = -4 \text{ mA}$		3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
lı	input leakage current	$V_1 = V_{CC}$ or GND; $V_{CC} = 5.5 V$	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OZ</sub>	OFF-state output current		-	-	±0.5	-	±5.0	-	±10	μΑ
I <sub>CC</sub>	supply current		-	-	8.0	-	80	-	160	μA
ΔI <sub>CC</sub>	additional supply current	$\label{eq:VI} \begin{array}{l} V_I = V_{CC} - 2.1 \text{ V};\\ \text{other inputs at } V_{CC} \text{ or GND};\\ V_{CC} = 4.5 \text{ V to 5.5 V};\\ I_O = 0 \text{ A} \end{array}$								
		per input pin; 1An inputs	-	70	252	-	315	-	343	μΑ
		per input pin; 2An inputs	-	70	252	-	315	-	343	μΑ
		per input pin; nE inputs	-	135	486	-	607.5	-	661.5	μΑ
CI	input capacitance		-	3.5	-	-	-	-	-	pF

Dual 2-to-4 line decoder/demultiplexer

## **10.** Dynamic characteristics

#### Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions	Ta	<sub>mb</sub> = 25	°C		= –40 °C ⋅85 °C	T <sub>amb</sub> = to +	= –40 °C 125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC13	9									
t <sub>pd</sub>	propagation	nAn to $n\overline{Y}n$ ; see Figure 6	1]							
	delay	V <sub>CC</sub> = 2.0 V	-	39	145	-	180	-	220	ns
		V <sub>CC</sub> = 4.5 V	-	14	29	-	36	-	44	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	11	-	-	-	-	-	ns
		$V_{CC} = 6.0 V$	-	11	25	-	31	-	38	ns
		$n\overline{E}$ to $n\overline{Y}n$ ; see Figure 7	1]							
		V <sub>CC</sub> = 2.0 V	-	33	135	-	170	-	205	ns
		$V_{CC} = 4.5 V$	-	12	27	-	34	-	41	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	10	-	-	-	-	-	ns
		$V_{CC} = 6.0 V$	-	10	23	-	29	-	35	ns
t <sub>t</sub> transition time		n <del>Y</del> n; see <u>Figure 6</u> and <u>Figure 7</u>	2]							
		V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 V$	-	6	13	-	16	-	19	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	3] _	42	-	-	-	-	-	pF
74HCT1	39									
t <sub>pd</sub>	propagation	nAn to Yn; see Figure 6	1]							
	delay	V <sub>CC</sub> = 4.5 V	-	16	34	-	43	-	51	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	13	-	-	-	-	-	ns
		nE to nYn; see Figure 7	1]							
		V <sub>CC</sub> = 4.5 V	-	16	34	-	43	-	51	ns
		$V_{CC} = 5.0 \text{ V}; \text{ C}_{L} = 15 \text{ pF}$	-	13	-	-	-	-	-	ns
t <sub>t</sub>	transition time	n <del>Y</del> n; see <u>Figure 6</u> and <u>I</u> Figure 7	2]							
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
	1		1	1	1	1	1	1	1	1

Dual 2-to-4 line decoder/demultiplexer

Voltages	Voltages are referenced to GND (ground = 0 V); $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit see <u>Figure 8</u> .										
Symbol	Parameter	Conditions		T <sub>amb</sub> = 25 °C		T <sub>amb</sub> = −40 °C to +85 °C		T <sub>amb</sub> = −40 °C to +125 °C		Unit	
				Min	Тур	Max	Min	Max	Min	Max	
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V	<u>[3]</u>	-	44	-	-	-	-	-	pF

#### Table 7. Dynamic characteristics ...continued

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

 $[3] \quad C_{PD} \text{ is used to determine the dynamic power dissipation (P_D in \mu W).} \\ P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$ 

 $f_i$  = input frequency in MHz;

 $f_o = output$  frequency in MHz;

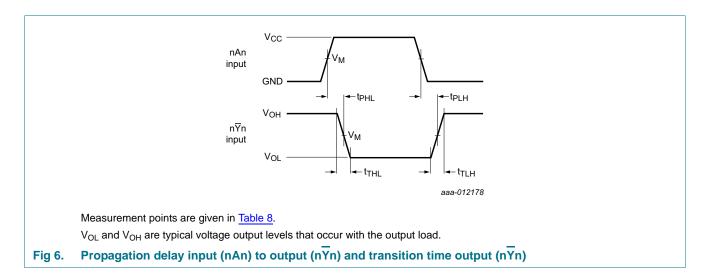
 $C_L$  = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$  = sum of outputs.

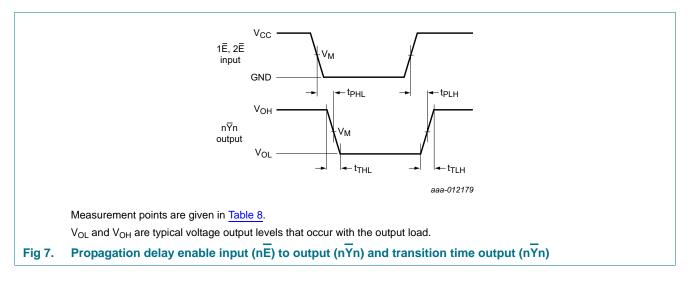
### 11. Waveforms



### **NXP Semiconductors**

## 74HC139; 74HCT139

Dual 2-to-4 line decoder/demultiplexer



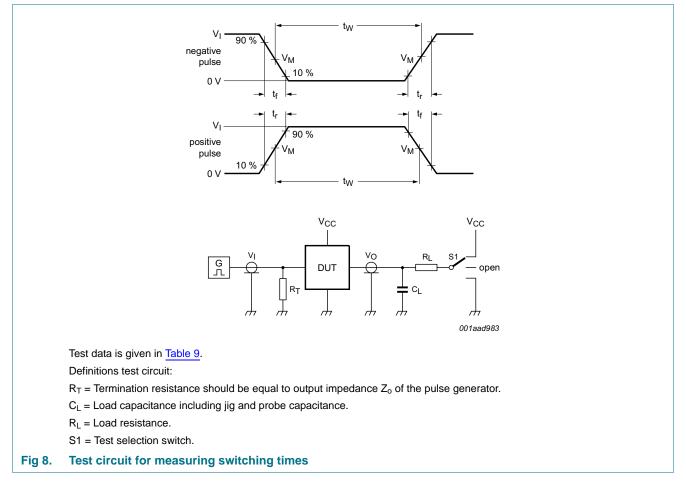
#### Table 8.Measurement points

Туре	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
74HC139	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
74HCT139	1.3 V	1.3 V

### **NXP Semiconductors**

# 74HC139; 74HCT139

### Dual 2-to-4 line decoder/demultiplexer



#### Table 9.Test data

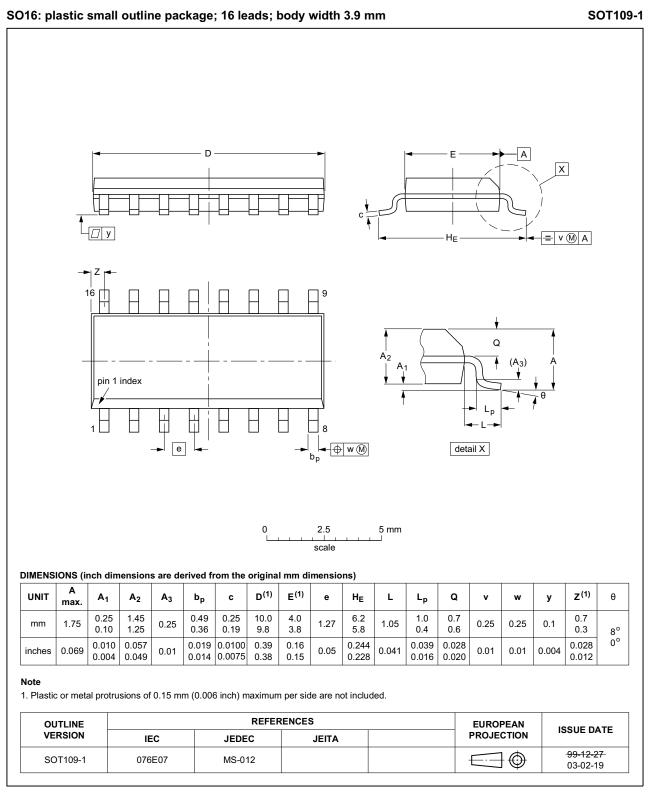
Туре	Input		Load		S1 position			
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	RL	t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>	
74HC139	V <sub>CC</sub>	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>	
74HCT139	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>	

### **NXP Semiconductors**

## 74HC139; 74HCT139

Dual 2-to-4 line decoder/demultiplexer

## 12. Package outline



#### Fig 9. Package outline SOT109-1 (SO16)

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74HC\_HCT139

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Dual 2-to-4 line decoder/demultiplexer

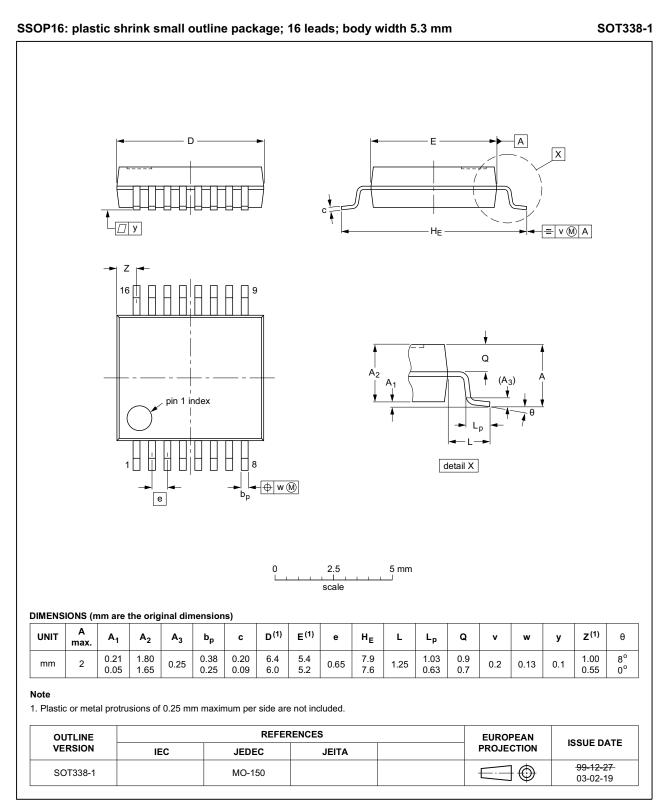


Fig 10. Package outline SOT338-1 (SSOP16)

74HC\_HCT139

Dual 2-to-4 line decoder/demultiplexer

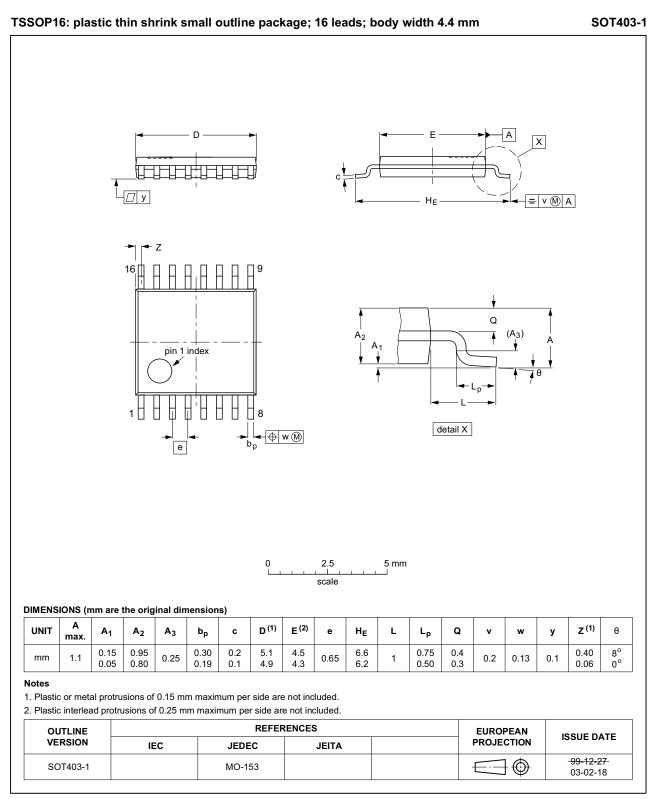


Fig 11. Package outline SOT403-1 (TSSOP16)

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74HC\_HCT139

Dual 2-to-4 line decoder/demultiplexer

## **13. Abbreviations**

Table 10. Abbreviations						
Acronym	Description					
CMOS	Complementary Metal-Oxide Semiconductor					
DUT	Device Under Test					
ESD	ElectroStatic Discharge					
НВМ	Human Body Model					
MM	Machine Model					
TTL	Transistor-Transistor Logic					

## 14. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT139 v.4	20151211	Product data sheet	-	74HC_HCT139 v.3	
Modifications:	<ul> <li>Type numbers 74HC139N and 74HCT139N (SOT38-4) removed.</li> </ul>				
74HC_HCT139 v.3	20140328	Product data sheet	-	74HC_HCT139 v.2	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>				
	<ul> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>				
74HC_HCT139_CNV v.2	19930927	Product specification	-	-	

Dual 2-to-4 line decoder/demultiplexer

## **15. Legal information**

### 15.1 Data sheet status

Document status[1][2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <a href="http://www.nxp.com">http://www.nxp.com</a>.

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#### Dual 2-to-4 line decoder/demultiplexer

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Dual 2-to-4 line decoder/demultiplexer

### **17. Contents**

1	General description 1
2	Features and benefits 1
3	Ordering information 1
4	Functional diagram 2
5	Pinning information 3
5.1	Pinning 3
5.2	Pin description 3
6	Functional description 4
7	Limiting values 4
8	Recommended operating conditions 5
9	Static characteristics 5
10	Dynamic characteristics 7
11	Waveforms 8
12	Package outline 11
13	Abbreviations 14
14	Revision history 14
15	Legal information 15
15.1	Data sheet status 15
15.2	Definitions 15
15.3	Disclaimers 15
15.4	Trademarks 16
16	Contact information 16
17	Contents 17

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Date of release: 11 December 2015 Document identifier: 74HC\_HCT139