



Integrated Device Technology, Inc.

FAST CMOS 8-INPUT MULTIPLEXER

IDT54/74FCT151T/AT/CT

FEATURES:

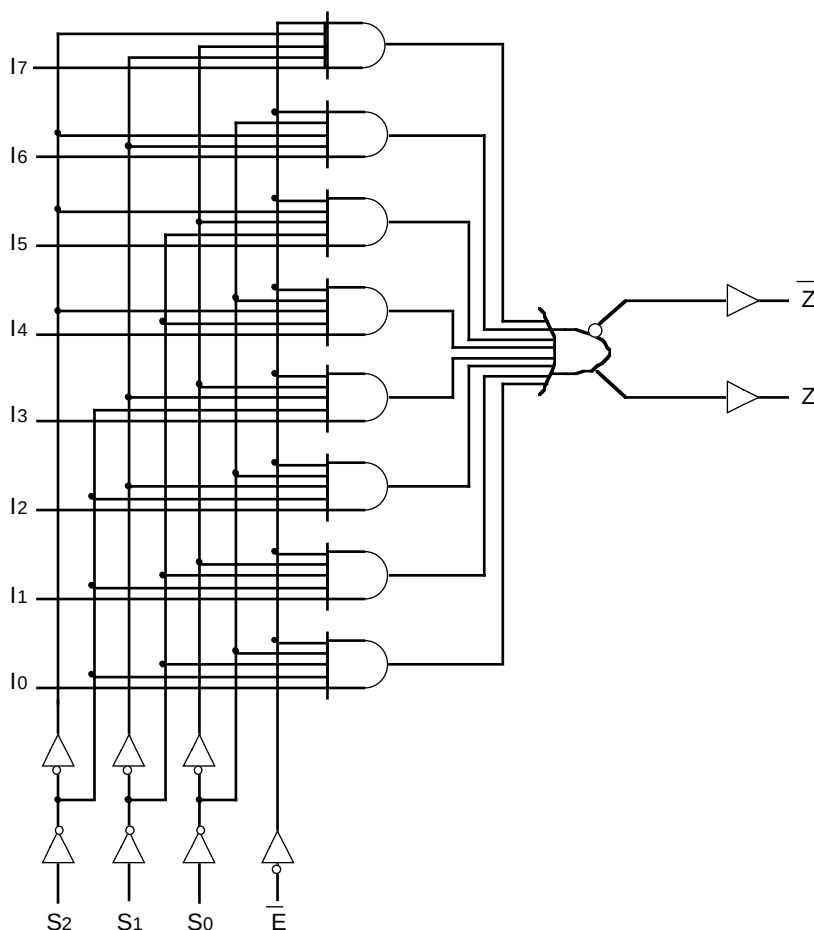
- Std., A, and C speed grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- Extended commercial range of -40°C to $+85^\circ\text{C}$
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- High drive outputs (-15mA I_{OH} , 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

DESCRIPTION:

The IDT54/74FCT151T/AT/CT are high-speed 8-input multiplexers built using an advanced dual metal CMOS technology. They select one bit of data from up to eight sources under the control of three select inputs. Both assertion and negation outputs are provided.

The IDT54/74FCT151T/AT/CT has a common Active-LOW enable ($\bar{E}$) input. When $\bar{E}$ is LOW, data from one of eight inputs is routed to the complementary outputs according to the 3-bit code applied to the Select (S_0 - S_2) inputs. A common application of the 'FCT151 is data routing from one of eight sources.

FUNCTIONAL BLOCK DIAGRAM



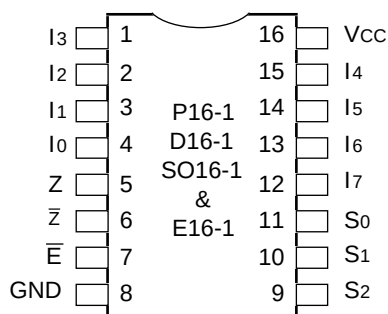
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

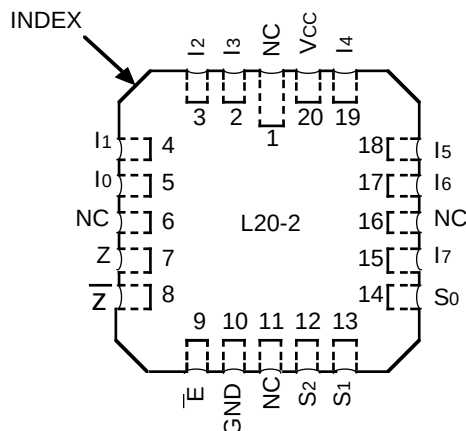
SEPTEMBER 1996

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

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LCC
TOP VIEW

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

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- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
I ₀ - I ₇	Data Inputs
S ₀ - S ₂	Selects Inputs
E-bar	Enable Input (Active LOW)
Z	Data Output
Z-bar	Inverted Data Output

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FUNCTION TABLE⁽¹⁾

Inputs				Outputs	
S ₂	S ₁	S ₀	E-bar	Z	Z-bar
X	X	X	H	L	H
L	L	L	L	I ₀	I ₀ -bar
L	L	H	L	I ₁	I ₁ -bar
L	H	L	L	I ₂	I ₂ -bar
L	H	H	L	I ₃	I ₃ -bar
H	L	L	L	I ₄	I ₄ -bar
H	L	H	L	I ₅	I ₅ -bar
H	H	L	L	I ₆	I ₆ -bar
H	H	H	L	I ₇	I ₇ -bar

NOTE:

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- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't care, Z = High Impedance.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	± 1	μA
I_{OZH}	High Impedance Output Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	μA
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, $V_I = V_{CC} (\text{Max.})$		—	—	20	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$ ⁽³⁾ , $V_O = \text{GND}$		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -6\text{mA MIL.}$ $I_{OH} = -8\text{mA COM'L.}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 32\text{mA MIL.}$ $I_{OL} = 48\text{mA COM'L.}$	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\bar{E}$ or $\overline{OE} = \text{GND}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁵⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\bar{E}$ or $\overline{OE} = \text{GND}$ One Input Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.2	6.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	3.5	7.5	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_o)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_o = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FCT151T				IDT54/74FCT151AT				IDT54/74FCT151CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay SN to Z̄	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.6	1.5	7.4	1.5	5.6	1.5	6.2	ns
tPLH tPHL	Propagation Delay SN to Z		1.5	10.5	1.5	11.5	1.5	6.8	1.5	7.6	1.5	5.8	1.5	6.5	ns
tPLH tPHL	Propagation Delay Ē to Z̄		1.5	7.0	1.5	7.5	1.5	5.6	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPLH tPHL	Propagation Delay Ē to Z		1.5	9.5	1.5	11.0	1.5	5.8	1.5	6.6	1.5	5.0	1.5	5.7	ns
tPLH tPHL	Propagation Delay IN to Z̄		1.5	6.5	1.5	7.5	1.5	5.2	1.5	5.8	1.5	4.4	1.5	4.9	ns
tPLH tPHL	Propagation Delay IN to Z		1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.1	1.5	4.7	1.5	5.2	ns

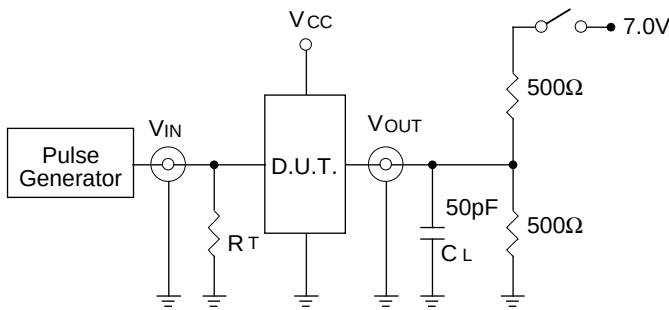
NOTES:

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- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

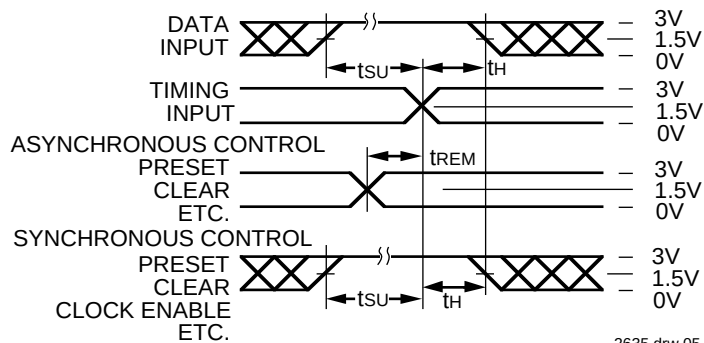
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

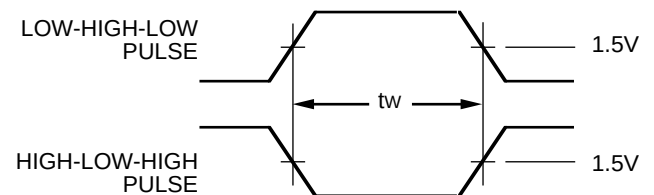
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SET-UP, HOLD AND RELEASE TIMES



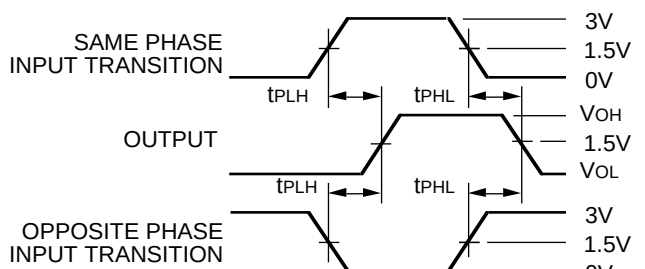
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PULSE WIDTH



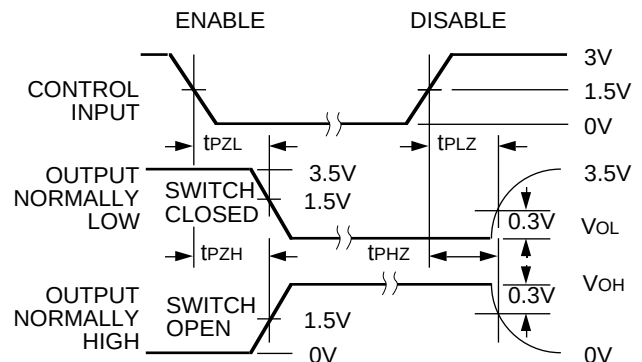
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PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

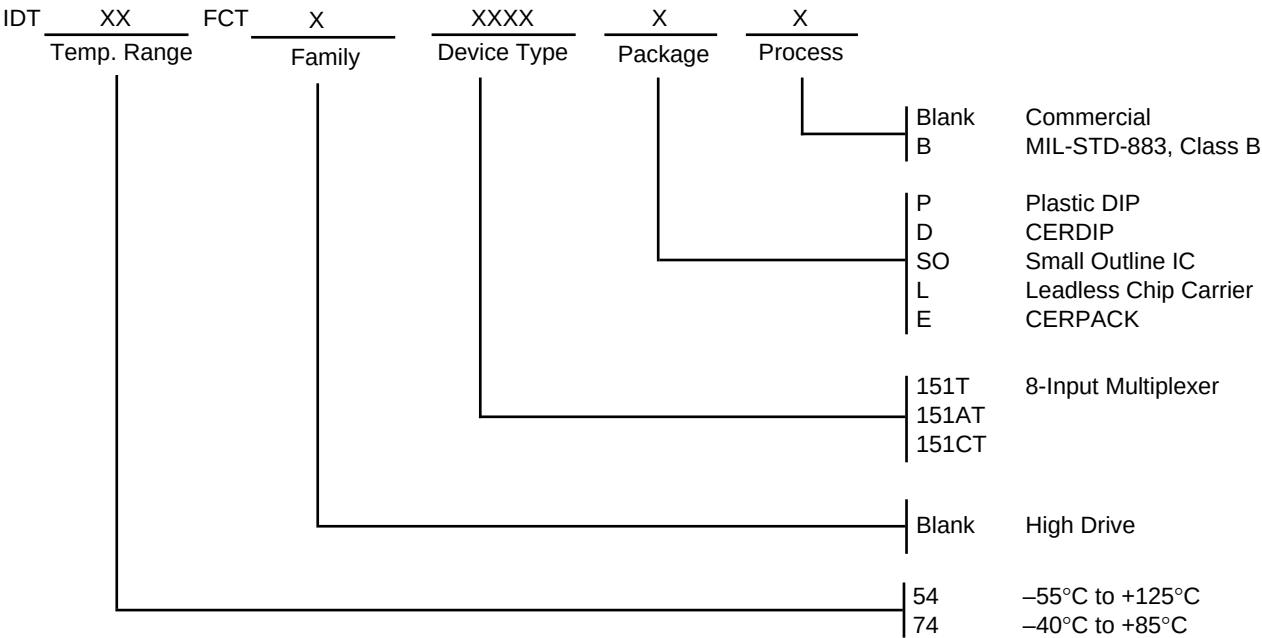


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NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$

ORDERING INFORMATION



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