

## 74F827 • 74F828 10-Bit Buffers/Line Drivers

### General Description

The 74F827 and 74F828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

The 74F828 is an inverting version of the 74F827.

### Features

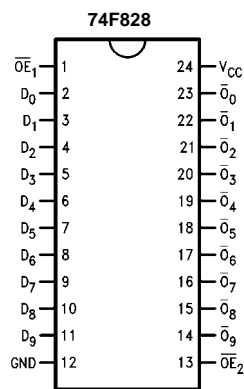
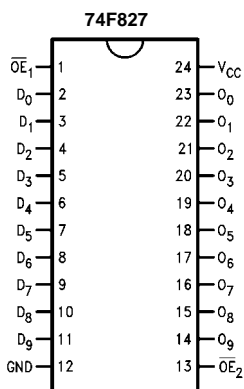
- 3-STATE output
- 74F828 is inverting

### Ordering Code:

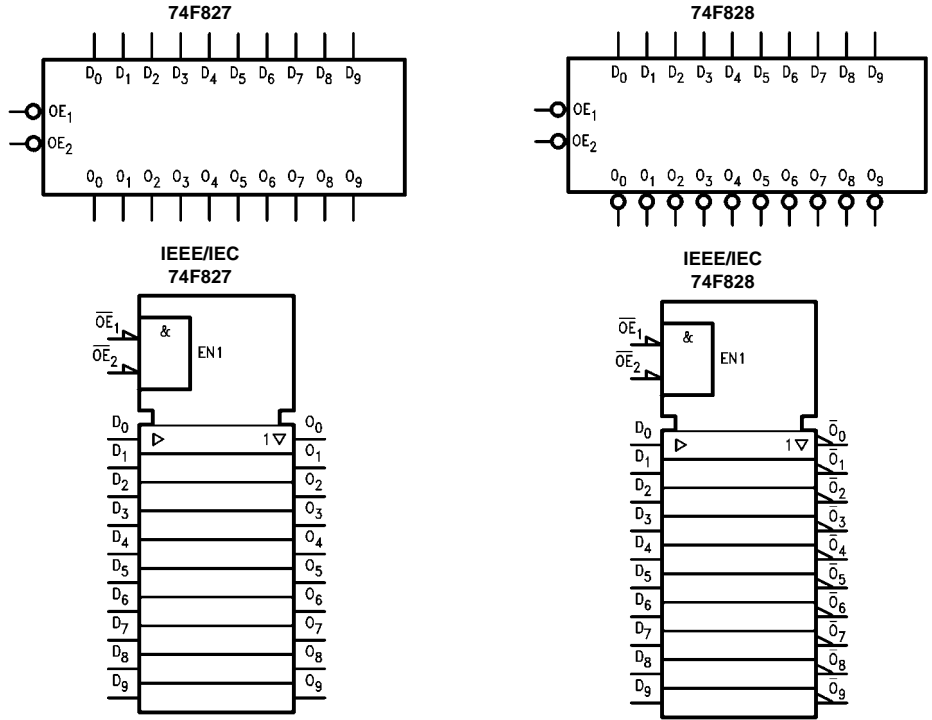
Order Number	Package Number	Package Description
74F827SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F827SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
74F828SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F828SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagrams



# Logic Symbols



# Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
OE <sub>1</sub> , OE <sub>2</sub>	Output Enable Input	1.0/1.0	20 μA/-0.6 mA
D <sub>0</sub> -D <sub>7</sub>	Data Inputs	1.0/1.0	20 μA/-0.6 mA
O <sub>0</sub> -O <sub>7</sub>	Data Outputs, 3-STATE	600/106.6 (80)	-12 mA/64 mA (48 mA)

# Functional Description

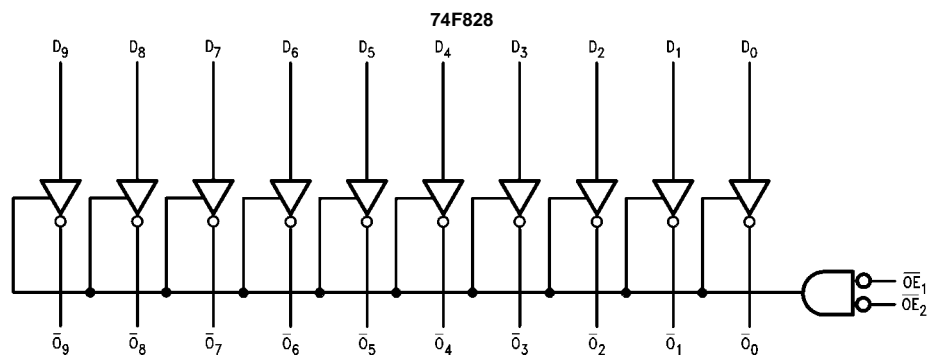
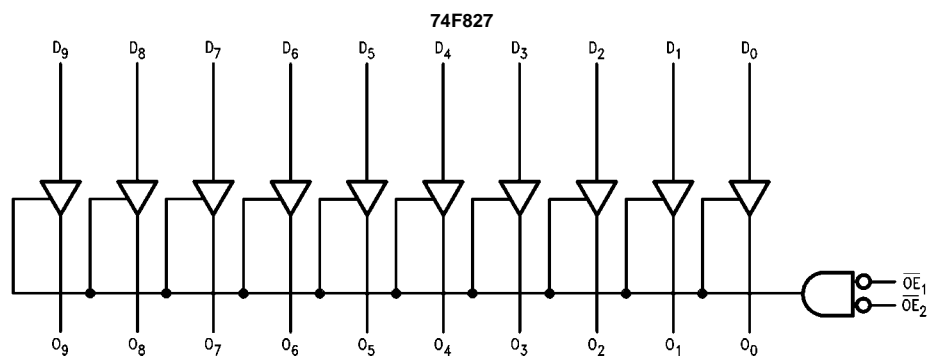
The 74F827 and 74F828 are line drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density. The devices have 3-STATE outputs controlled by the Output Enable (OE) pins. The outputs can sink 64 mA and source 15 mA. Input clamp diodes limit high-speed termination effects.

# Function Table

Inputs		Outputs		Function
$\overline{\text{OE}}$	$D_n$	$O_n$		
		74F827	74F828	
L	H	H	L	Transparent
L	L	L	H	Transparent
H	X	Z	Z	High Z

H = HIGH Voltage level  
L = LOW Voltage Level  
Z = High Impedance  
X = Immaterial

## Logic Diagrams



**Absolute Maximum Ratings** (Note 1)

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	–0.5V to V <sub>CC</sub>
3-STATE Output	–0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

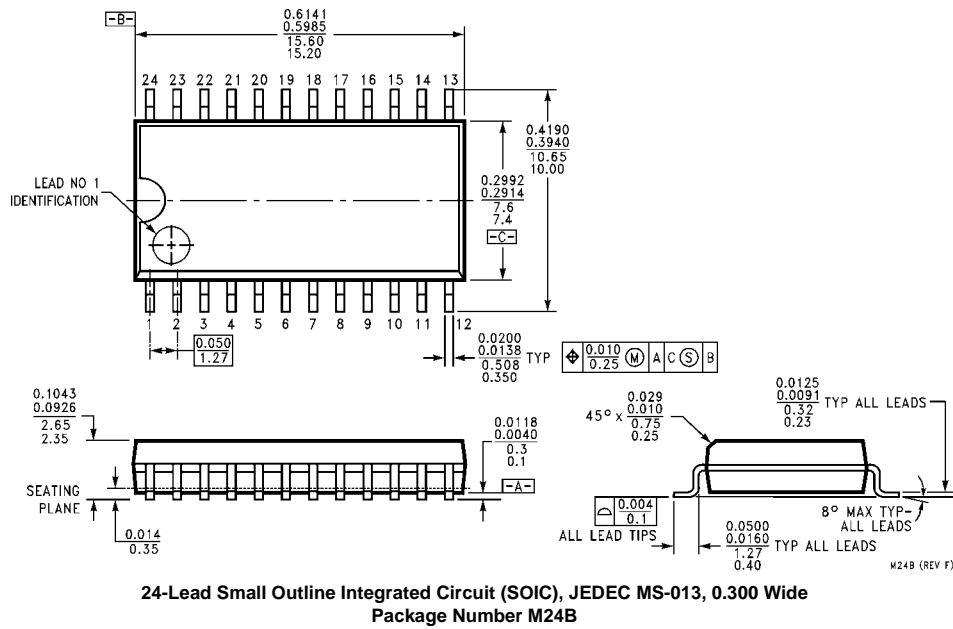
**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			–1.2	V	Min	I <sub>IN</sub> = –18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.4 2.0 2.7		V	Min	I <sub>OH</sub> = –3 mA I <sub>OH</sub> = –15 mA I <sub>OH</sub> = –3 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			–0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			–50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	–100		–225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current (74F827)		30	45	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (74F827)		60	90	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current (74F827)		40	60	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current (74F828)		14	20	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (74F828)		56	85	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current (74F828)		35	50	mA	Max	V <sub>O</sub> = HIGH Z

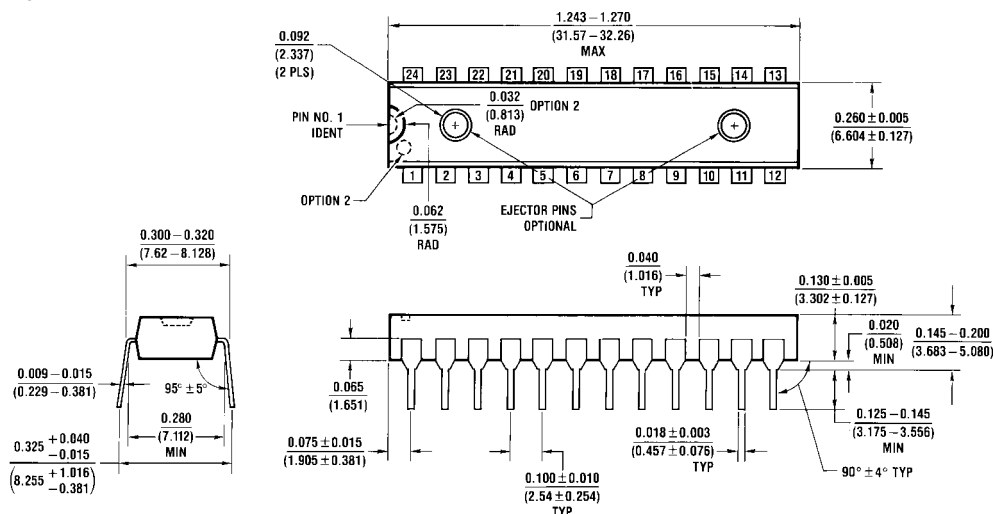
## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	1.0	3.0	5.5	1.0	7.5	1.0	6.5	ns
t <sub>PHL</sub>	Data to Output (74F827)	1.5	3.3	5.5	1.5	7.0	1.5	6.0	
t <sub>PLH</sub>	Propagation Delay	1.0	3.0	5.0			1.0	5.5	ns
t <sub>PHL</sub>	Data to Output (74F828)	1.0	2.0	4.0			1.0	4.0	
t <sub>PZH</sub>	Output Enable Time	3.0	5.7	9.0	2.5	10.0	2.5	9.5	ns
t <sub>PZL</sub>	$\overline{\text{OE}}$ to O <sub>n</sub>	3.5	6.8	11.5	3.0	12.5	3.0	12.0	
t <sub>PHZ</sub>	Output Disable Time	1.5	3.3	8.0	1.5	9.0	1.5	8.5	ns
t <sub>PLZ</sub>	$\overline{\text{OE}}$ to O <sub>n</sub>	1.0	3.5	8.0	1.0	9.0	1.0	8.5	

# Physical Dimensions inches (millimeters) unless otherwise noted



# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N24C (REV F)

24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide Package Number N24C

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