

March 1988 Revised August 1999

74F651 • 74F652 Transceivers/Registers

General Description

These devices consist of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

Features

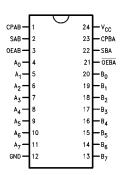
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths 74F651 inverting 74F652 non-inverting

Ordering Code:

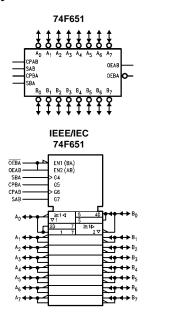
Order Number	Package Number	Package Description
74F651SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F651SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
74F652SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
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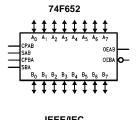
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

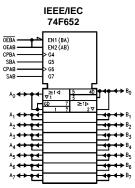
Connection Diagram



Logic Symbols







Unit Loading/Fan Out

Pin Names	Decerinties	U.L.	Input I _{IH} /I _{IL}	
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}	
A ₀ -A ₇ , B ₀ -B ₇	A and B Inputs/	1.0/1.0	20 μA/–0.6 mA	
	3-STATE Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)	
CPAB, CPBA	Clock Inputs	1.0/1.0	20 μA/-0.6 mA	
SAB, SBA	Select Inputs	1.0/1.0	20 μA/-0.6 mA	
OEAB, OEBA	Output Enable Inputs	1.0/1.0	20 μA/-0.6 mA	

Function Table

	Inputs					Inputs/Outp	uts (Note 1)	Outside a Maria
OEAB	OEBA	СРАВ	СРВА	SAB	SBA	A ₀ thru A ₇	B ₀ thru B ₇	Operating Mode
L	Н	H or L	H or L	Χ	Х	Input	Input	Isolation
L	Н	\	\	Χ	Χ			Store A and B Data
Х	Н	\	H or L	Χ	Χ	Input	Not Specified	Store A, Hold B
Н	Н	\	\	Χ	Χ	Input	Output	Store A in Both Registers
L	Χ	H or L	\	Χ	Χ	Not Specified	Input	Hold A, Store B
L	L	\	\	Χ	Χ	Output	Input	Store B in Both Registers
L	L	Χ	Χ	Χ	L	Output	Input	Real-Time B Data to A Bus
L	L	Χ	H or L	Χ	Н			Store B Data to A Bus
Н	Н	Χ	Χ	L	Χ	Input	Output	Real-Time A Data to B Bus
Н	Н	H or L	Χ	Н	Χ			Stored A Data to B Bus
Н	L	H or L	H or L	Н	Н	Output	Output	Stored A Data to B Bus and
								Stored B Data to A Bus

H = HIGH Voltage Level X = Immaterial

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

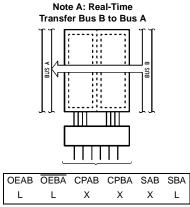
The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

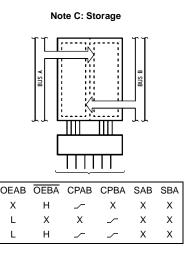
Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW-to-HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Note B: Real-Time

Transfer Bus A to Bus B



OEAB OEBA CPAB CPBA SAB SBA Н Н Χ Χ



Х

L

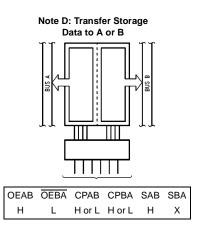
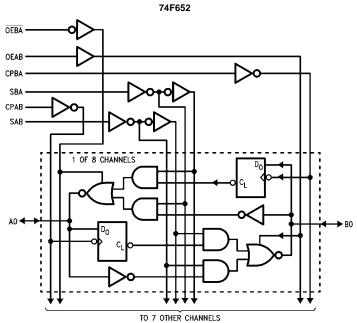


FIGURE 1.

Χ

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

OEBA OEAB CPBA SBA CPAB SAB TO 7 OTHER CHANNELS

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

 $\begin{array}{lll} \mbox{Storage Temperature} & -65^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{Ambient Temperature under Bias} & -55^{\circ}\mbox{C to } +125^{\circ}\mbox{C} \\ \mbox{Junction Temperature under Bias} & -55^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \end{array}$

 V_{CC} Pin Potential to Ground Pin -0.5V to +7.0VInput Voltage (Note 3) -0.5V to +7.0VInput Current (Note 3) -30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC} 3-STATE Output -0.5V to +5.5V

Current Applied to Output

Recommended Operating Conditions

Free Air Ambient Temperature 0°C to +70°C Supply Voltage +4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

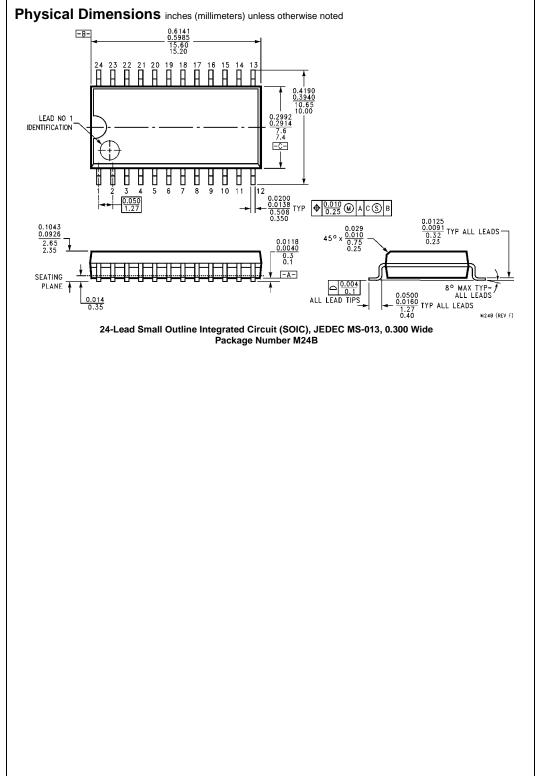
Symbol	Parameter		Min	Тур	Max	Units	v _{cc}	Conditions
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				8.0	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage	10% V _{CC}	2.0			V	Min	$I_{OH} = -15 \text{ mA } (A_n, B_n)$
V _{OL}	Output LOW Voltage	10% V _{CC}			0.55	V	Min	I _{OL} = 64 mA (A _n , B _n)
I _{IH}	Input HIGH Current				5.0	μА	Max	V _{IN} = 2.7V (Non I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test				7.0	μА	Max	V _{IN} = 7.0V
I _{BVIT}	Input HIGH Current Breakdown (I/O)				0.5	mA	Max	$V_{IN} = 5.5V$ (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current				50	μА	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test		4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current				3.75	μА	0.0	VI _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V (Non I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current				70	μΑ	Max	$V_{OUT} = 2.7V (A_n, B_n)$
I _{IL} + I _{OZL}	Output Leakage Current				-650	μΑ	Max	$V_{OUT} = 0.5V (A_n, B_n)$
los	Output Short-Circuit Current		-100		-225	mA	Max	$V_{OUT} = 0V$
I _{ZZ}	Bus Drainage Test				500	μΑ	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current			105	135	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			118	150	mA	Max	$V_0 = LOW$
I _{CCZ}	Power Supply Current			115	150	mA	Max	V _O = HIGH Z

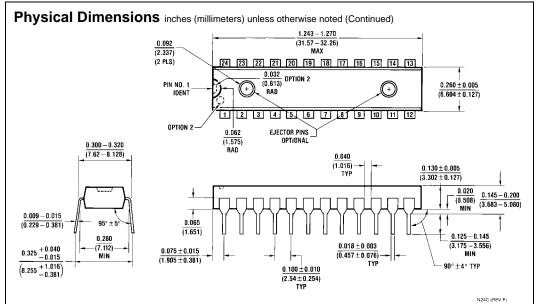
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25$ °C $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Max	Min	Max	Min	Max	
f _{MAX}	Max. Clock Frequency	90		75		90		MHz
t _{PLH}	Propagation Delay	2.0	7.0	2.0	8.5	2.0	8.0	ns
t _{PHL}	Clock to Bus	2.0	8.0	2.0	9.5	2.0	9.0	
t _{PLH}	Propagation Delay	2.0	8.5	1.0	9.0	2.0	9.0	no
t _{PHL}	Bus to Bus (74F651)	1.0	7.5	1.0	8.0	1.0	8.0	ns
t _{PLH}	Propagation Delay	1.0	7.0	1.0	8.0	1.0	7.5	ns
t _{PHL}	Bus to Bus (74F652)	1.0	6.5	1.0	8.0	1.0	7.0	115
t _{PLH}	Propagation Delay	2.0	8.5	2.0	11.0	2.0	9.5	no
t _{PHL}	SBA or SAB to A or B	2.0	8.0	2.0	10.0	2.0	9.0	ns

AC Operating Requirements

	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$		$T_A = -55^{\circ}C$	C to +125°C	$T_A = 0^{\circ}C \text{ to } +70^{\circ}C$		
Symbol				$V_{CC} = +5.0V$		$V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
t _{PZH}	Enable Time	2.0	9.5	2.0	10.0	2.0	10.0	ns
t_{PZL}	*OEBA to A	2.0	12.0	2.0	10.0	2.0	12.5	
t _{PHZ}	Disable Time	1.0	7.5	1.0	9.0	1.0	8.0	
t_{PLZ}	*OEBA to A	2.0	8.5	1.0	9.0	2.0	9.0	
t _{PZH}	Enable Time	2.0	9.5	2.0	10.0	2.0	10.0	
t_{PZL}	OEAB to B	3.0	13.0	2.0	12.0	3.0	14.0	
t _{PHZ}	Disable Time	2.0	9.0	1.0	9.0	2.0	10.0	ns
t_{PLZ}	OEAB to B	2.0	10.5	1.0	12.0	2.0	11.0	115
t _S (H)	Setup Time, HIGH or	5.0		5.0		5.0		ns
$t_S(L)$	LOW, Bus to Clock	5.0		5.0		5.0		113
t _H (H)	Hold Time, HIGH or	2.0		2.5		2.0		ns
$t_H(L)$	LOW, Bus to Clock	2.0		2.5		2.0		115
t _W (H)	Clock Pulse Width	5.0		5.0		5.0		ns
$t_{W}(L)$	HIGH or LOW	5.0		5.0		5.0		115





24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide Package Number N24C

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