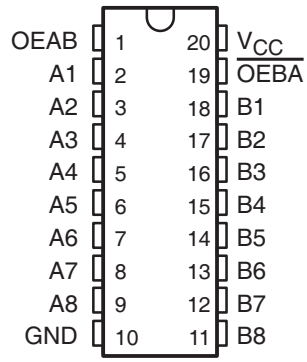
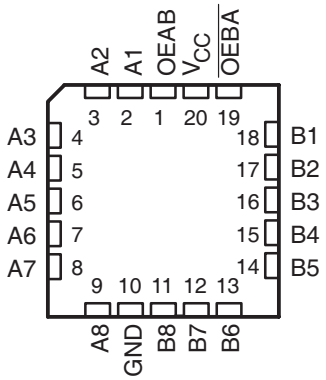
- **Local Bus-Latch Capability**
- **Noninverting Logic**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54F623 . . . J PACKAGE
SN74F623 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F623 . . . FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the output enable (OEAB and $\overline{\text{OEBA}}$) inputs.

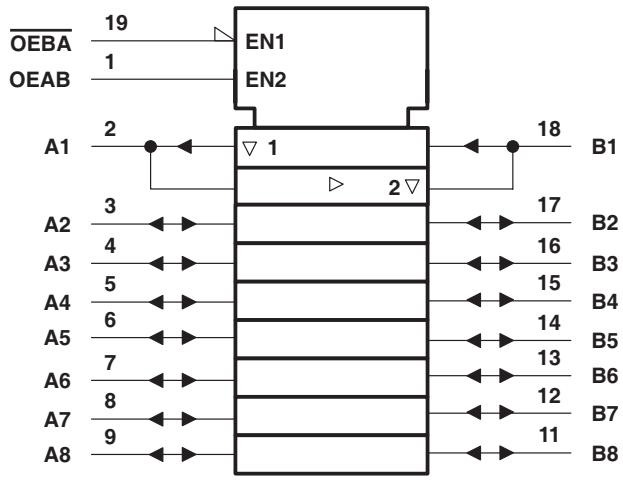
The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this configuration. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

The SN54F623 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F623 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

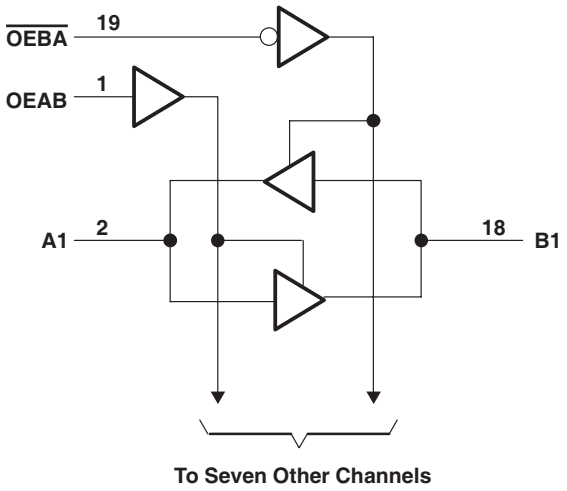
INPUTS		OPERATION
$\overline{\text{OEBA}}$	OEAB	
L	L	B data to A bus
L	H	B data to A bus, A data to B bus
H	L	Isolation
H	H	A data to B bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (excluding I/O ports) (see Note 1) . . . . . –1.2 V to 7 V
Input current range, I_{IK} . . . . . –30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . –0.5 V to V_{CC}
Current into any output in the low state: SN54F623 (A1–A8) . . . . . 40 mA
SN54F623 (B1–B8) . . . . . 96 mA
SN74F623 (A1–A8) . . . . . 48 mA
SN74F623 (B1–B8) . . . . . 128 mA
Operating free-air temperature range: SN54F623 . . . . . –55°C to 125°C
SN74F623 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

			SN54F623			SN74F623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				– 18			– 18	mA
I_{OH}	High-level output current	A1–A8			– 3			– 3	mA
		B1–B8			– 12			– 15	
I_{OL}	Low-level output current	A1–A8			20			24	mA
		B1–B8			48			64	
T_A	Operating free-air temperature		– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F623			SN74F623			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2			– 1.2	V
V_{OH}	A1–A8	V_{CC} = 4.5 V	I_{OH} = – 1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = – 3 mA	2.4	3.3		2.4	3.3		
	B1–B8		I_{OH} = – 3 mA	2.4	3.3		2.4	3.3		
			I_{OH} = – 12 mA	2	3.2					
			I_{OH} = – 15 mA				2	3.1		
	Any output	V_{CC} = 4.75 V,	I_{OH} = – 1 mA to – 3 mA				2.7			
V_{OL}	A1–A8	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	B1–B8		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	A and B ports	V_{CC} = 5.5 V	V_I = 5.5 V			1			1	mA
	OEAB or $\overline{OEBA}$		V_I = 7 V			0.1			0.1	
I_{IH}‡	A and B ports	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	µA
	OEAB or $\overline{OEBA}$					20			20	
I_{IL}‡	A and B ports	V_{CC} = 5.5 V,	V_I = 0.5 V			– 0.65			– 0.65	mA
	OEAB or $\overline{OEBA}$					– 0.6			– 0.6	
I_{OS}§	A1–A8	V_{CC} = 5.5 V,	V_O = 0	– 60		– 150	– 60		– 150	mA
	B1–B8			– 100		– 225	– 100		– 225	
I_{CCH}		V_{CC} = 5.5 V,	Any output = 4.5 V		110	140		110	140	mA
I_{CCL}		V_{CC} = 5.5 V	OEAB or $\overline{OEBA}$ = 4.5 V, A1–A8 = GND		110	140		110	140	mA
I_{CCZ}		V_{CC} = 5.5 V	$\overline{OEBA}$ or A1–A8 = 4.5 V, OEAB = GND		99	130		99	130	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			′F623			SN54F623		SN74F623		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.2	3.6	5.5	1.1	6.8	1.2	6.5	ns
t_{PHL}			2.2	4.6	7	1.6	8	1.7	7.5	
t_{PLH}	B	A	1.2	3.6	5.5	1.1	6.8	1.2	6.5	ns
t_{PHL}			1.7	4.1	6.5	1.6	8	1.7	7.5	
t_{PZH}	$\overline{OEBA}$	A	3.1	8.1	10.5	2.7	12.4	3.1	12	ns
t_{PZL}			2.8	7.1	9.5	2.5	10.3	2.8	10	
t_{PHZ}	$\overline{OEBA}$	A	1.7	4.1	6.5	1.6	8.3	1.7	7.5	ns
t_{PLZ}			1.7	4.1	6.5	1.5	7.4	1.7	7	
t_{PZH}	OEAB	B	2.8	7.6	10	2.7	12	2.8	11.5	ns
t_{PZL}			2.8	6.6	9	2.8	10	2.9	9.5	
t_{PHZ}	OEAB	B	2.2	5.6	8.5	1.9	10	2.2	10	ns
t_{PLZ}			3.2	6.6	9	3.1	10.7	3.2	10	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN54F623J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		
SN74F623DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74F623DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74F623N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SNJ54F623FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54F623J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF SN54F623, SN74F623 :

- Catalog: SN74F623
- Military: SN54F623

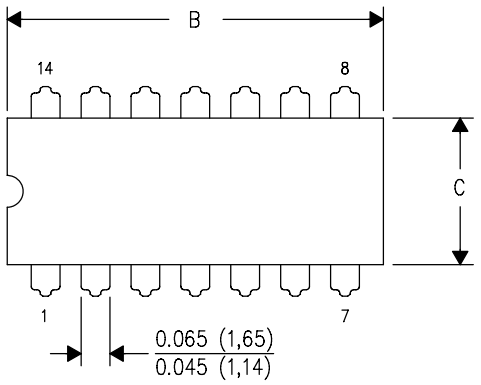
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

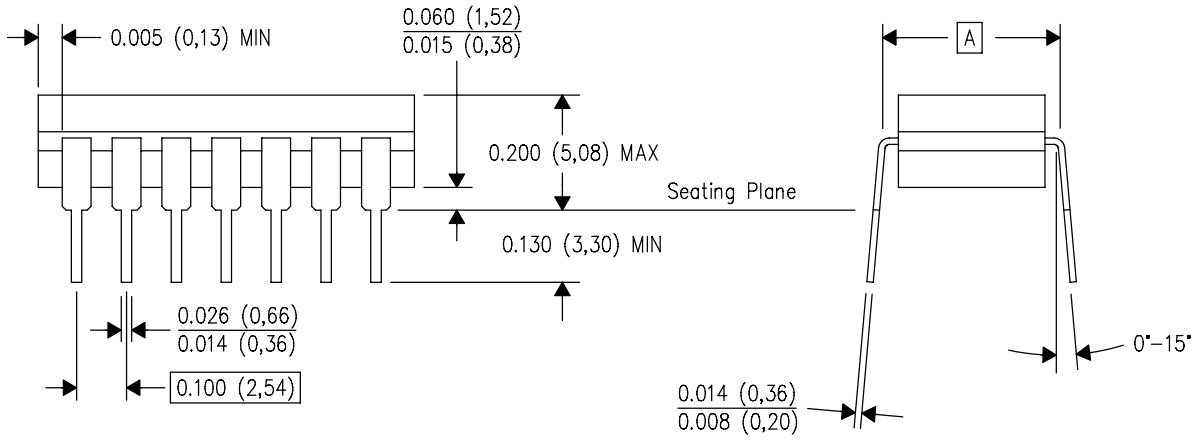
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

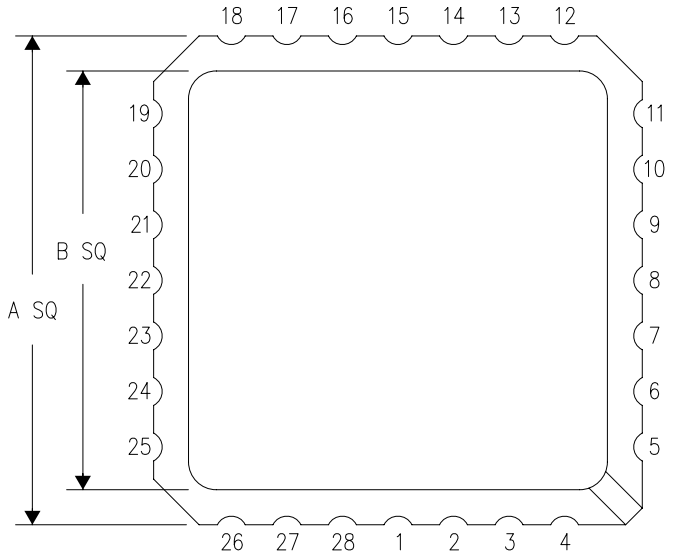


4040083/F 03/03

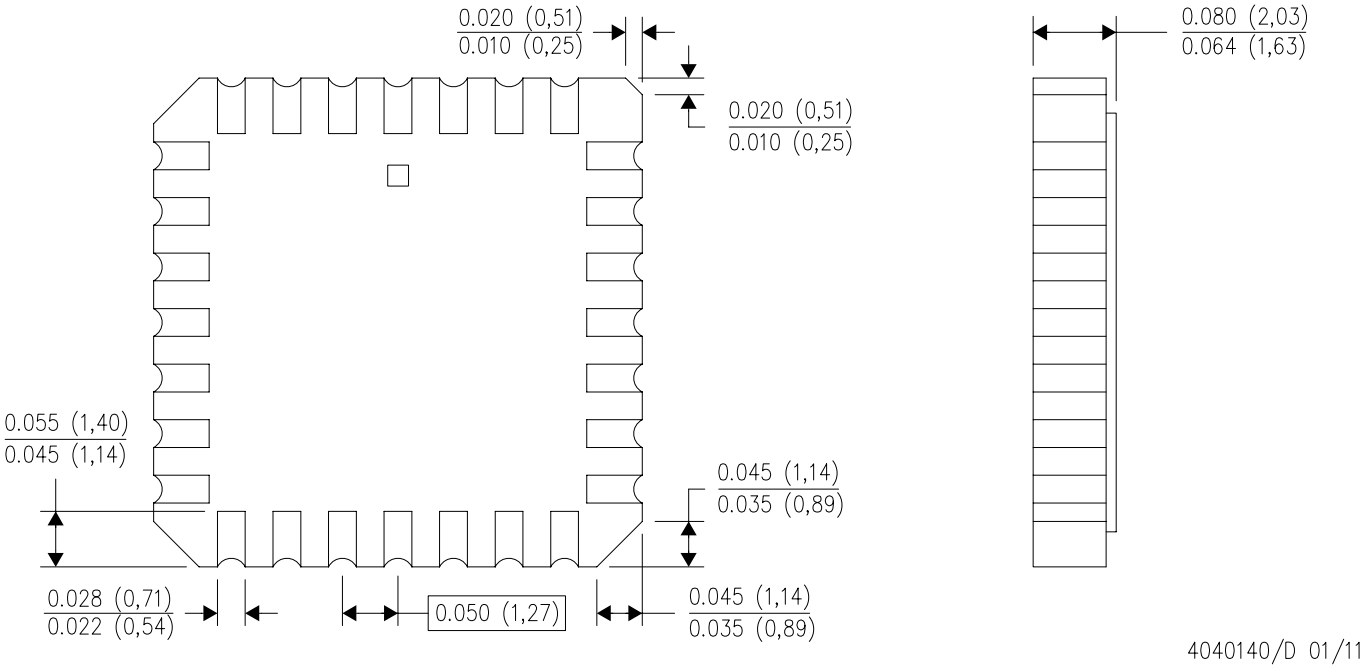
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



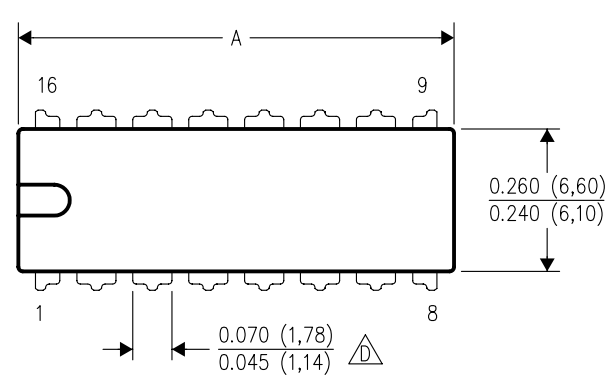
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

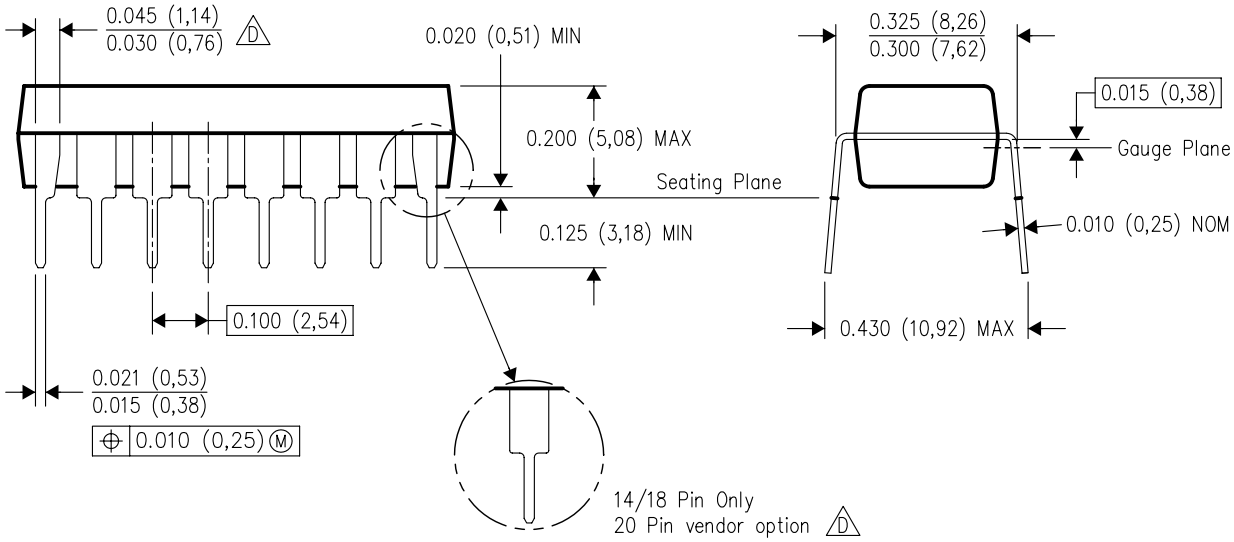
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

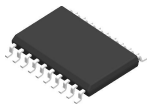


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

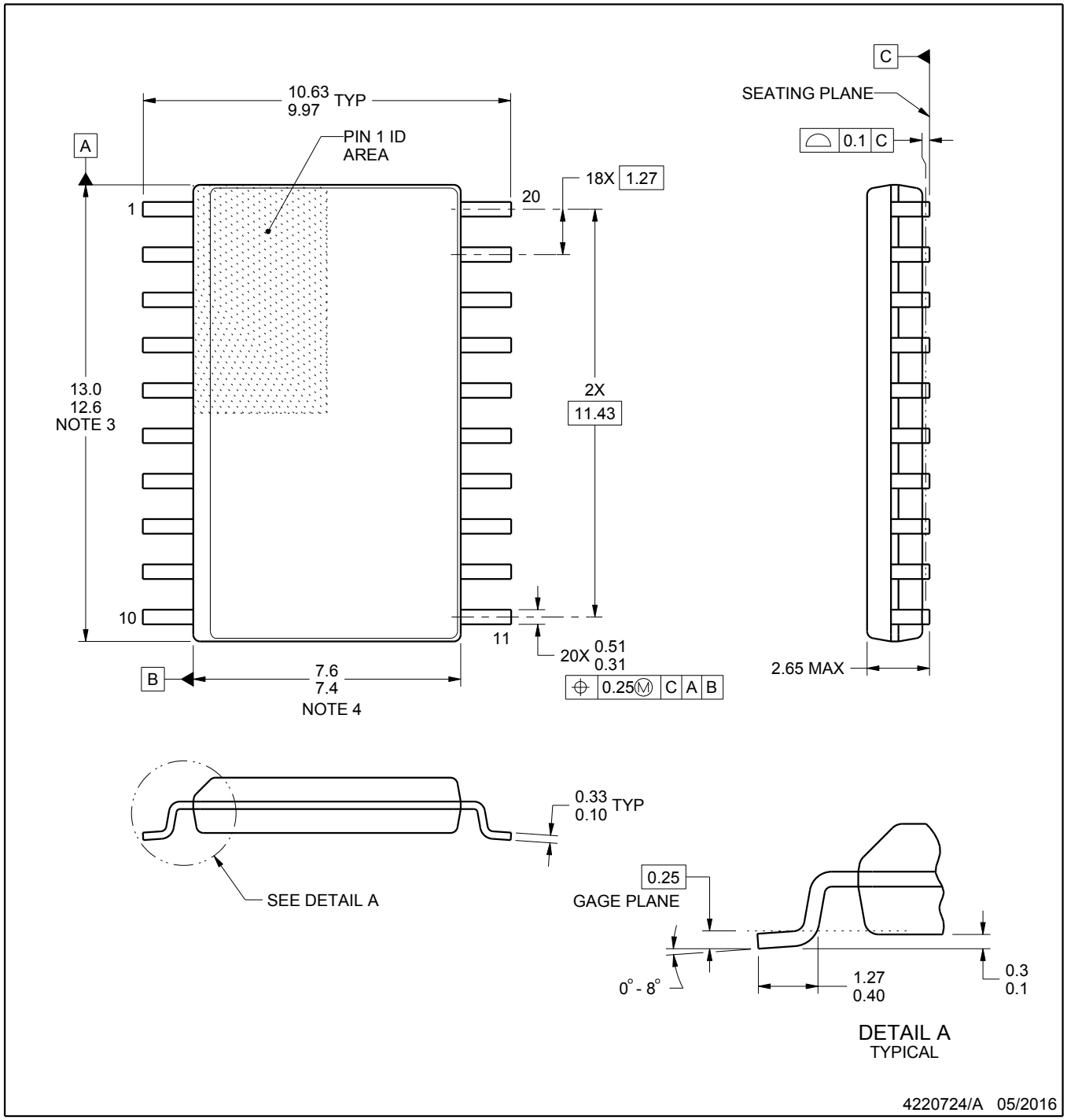


PACKAGE OUTLINE

DW0020A

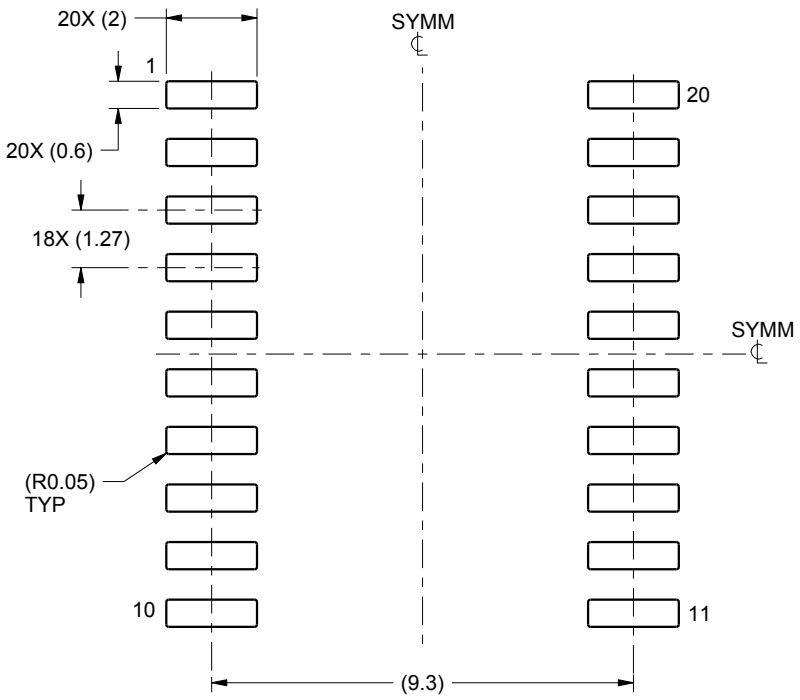
SOIC - 2.65 mm max height

SOIC

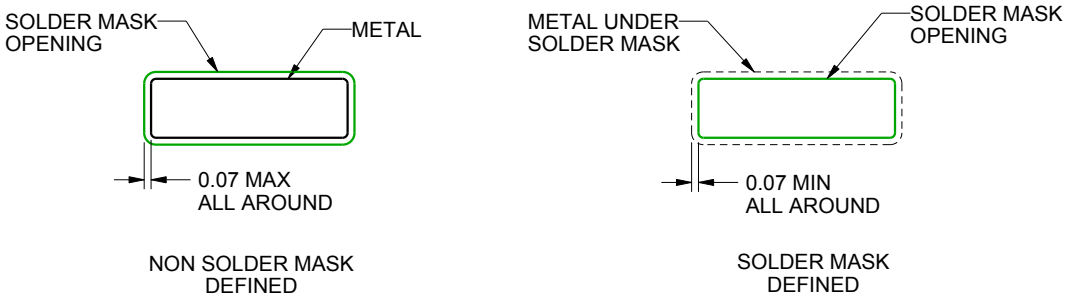


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

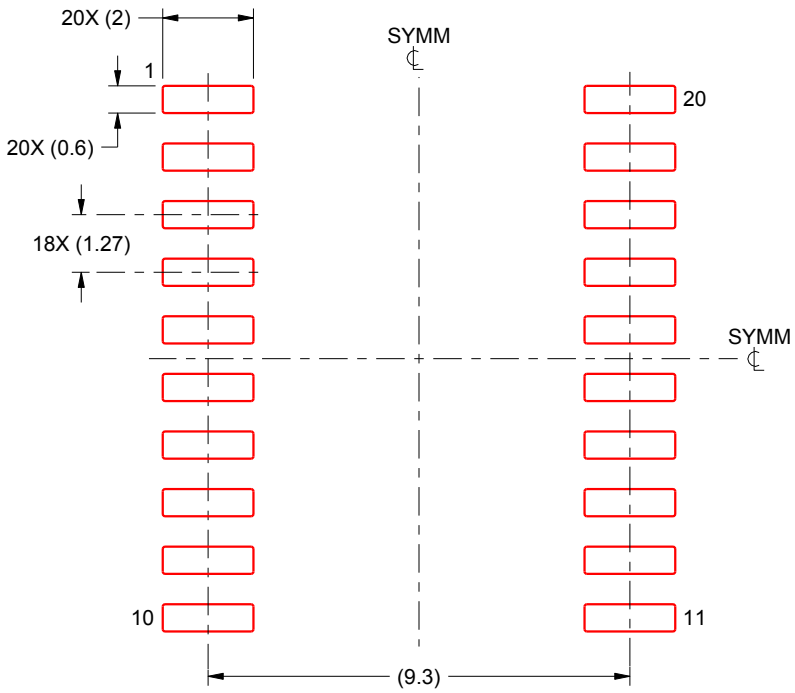


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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