DATA SHEET

74F597

8-bit shift register with input storage registers

Product specification

1991 Sep 13

IC15 Data Handbook

Philips
Semiconductors

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8-bit shift register with input storage registers 74F597

FEATURES

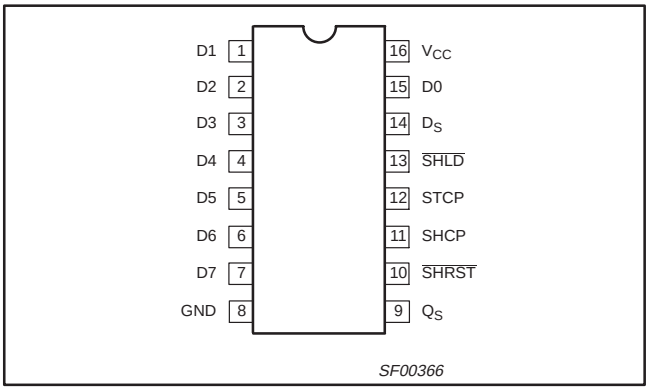
- High impedance PNP base inputs for reduced loading (20µA in High and Low states)
- 8-bit parallel storage register
- 3-State output buffers
- Shift register has asynchronous direct overriding reset
- Shift load $\overline{SHLD}$ is functional when SHCP is Low and locked out when SHCP is High
- Guaranteed shift frequency DC to 105MHz

DESCRIPTION

The 74F597 consists of an 8-bit storage register feeding a parallel-in/serial-in, serial-out 8-bit shift register. The storage register and shift register have separate positive edge triggered clocks. The shift register has asynchronous reset and when SHCP is Low, it has asynchronous load.

The shift register load function has been modified to load when both $\overline{SHLD}$ and SHCP are Low. When SHCP is High the shift register load operation is not performed. Data will be properly shifted on the rising edge of SHCP when $\overline{SHLD}$ is High.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F597	135MHz	42mA

ORDERING INFORMATION

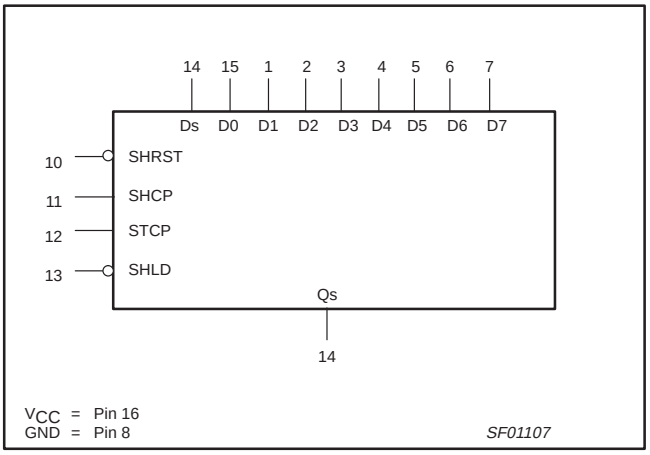
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F597N	SOT38-4
16-pin plastic SO	N74F597D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

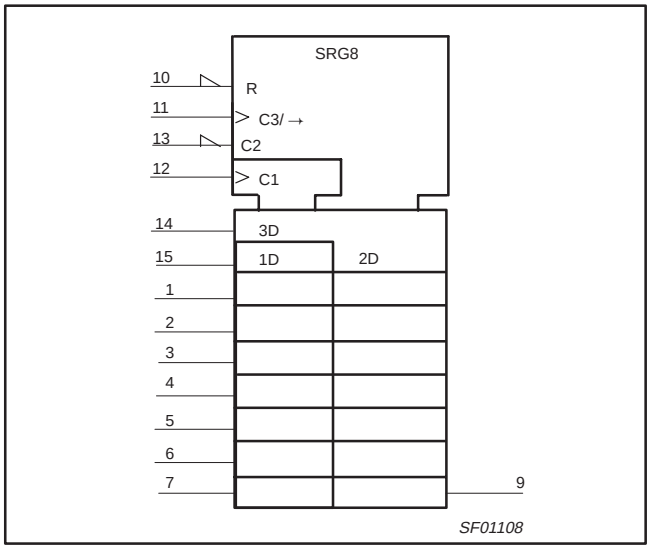
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ds	Serial data input	1.0/0.033	20µA/20µA
D0–D7	Parallel data inputs	1.0/0.033	20µA/20µA
SHCP	Shift register clock pulse input	1.0/0.033	20µA/20µA
STCP	Storage register clock pulse input	1.0/0.033	20µA/20µA
$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20µA/20µA
$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20µA/20µA
Qs	Serial data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



IEC/IEEE SYMBOL (IEEE/IEC)

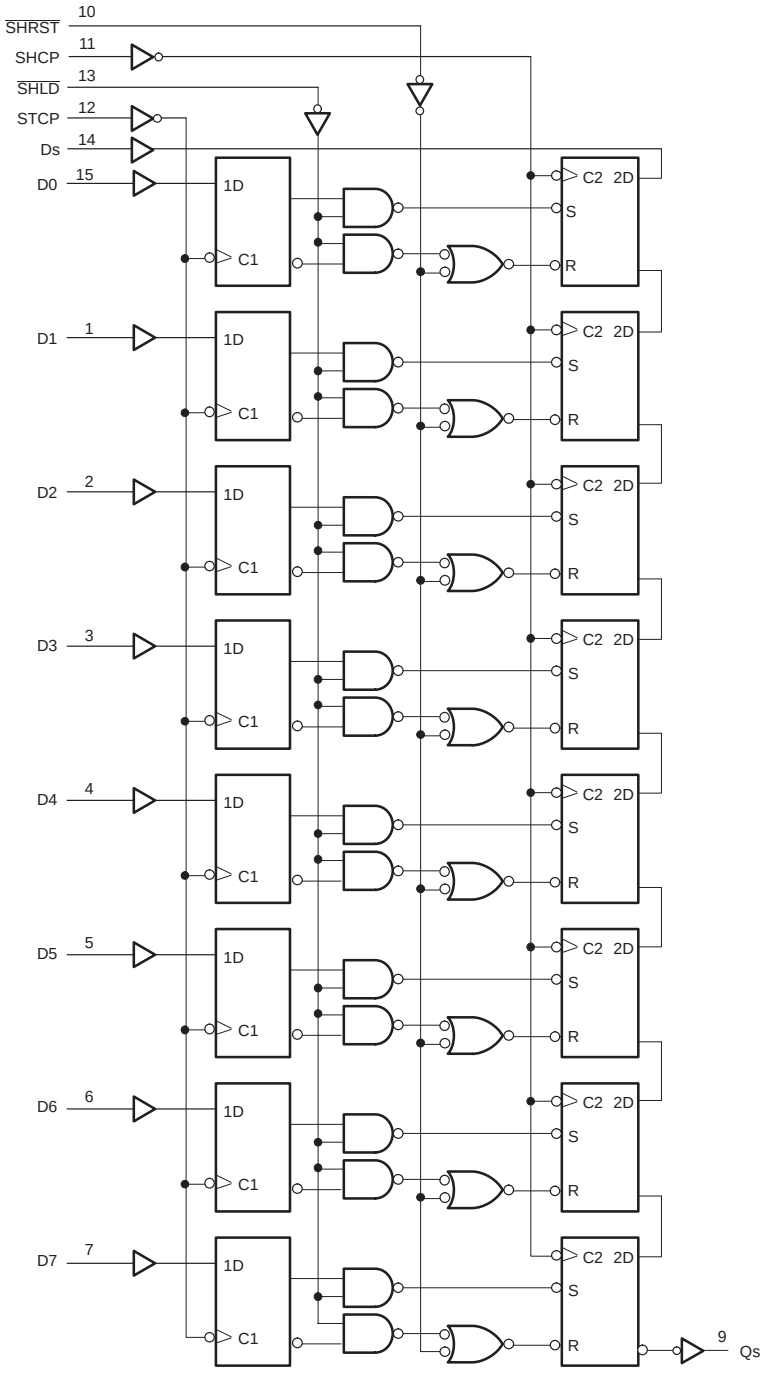


FUNCTION TABLE

INPUTS				OPERATING MODES
STCP	SHCP	$\overline{SHLD}$	$\overline{SHRST}$	
↑	X	X	X	Data loaded to storage registers
↑	L	L	H	Data loaded from inputs to shift register
↟	L	L	H	Data transferred from storage registers to shift registers
X	L	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	↑	H	H	Shift register clocked, Qn=Qn–1, Q0=Ds
↟	H	X	H	Hold

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
↟ = Not a Low-to-High clock transition

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

SF01109

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[NO TAG]			LIMITS			UNIT
						MIN	TYP NO TAG	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX		±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OS}	Short-circuit output current[NO TAG]		V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				43	65	mA
		I_{CCL}					41	60	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

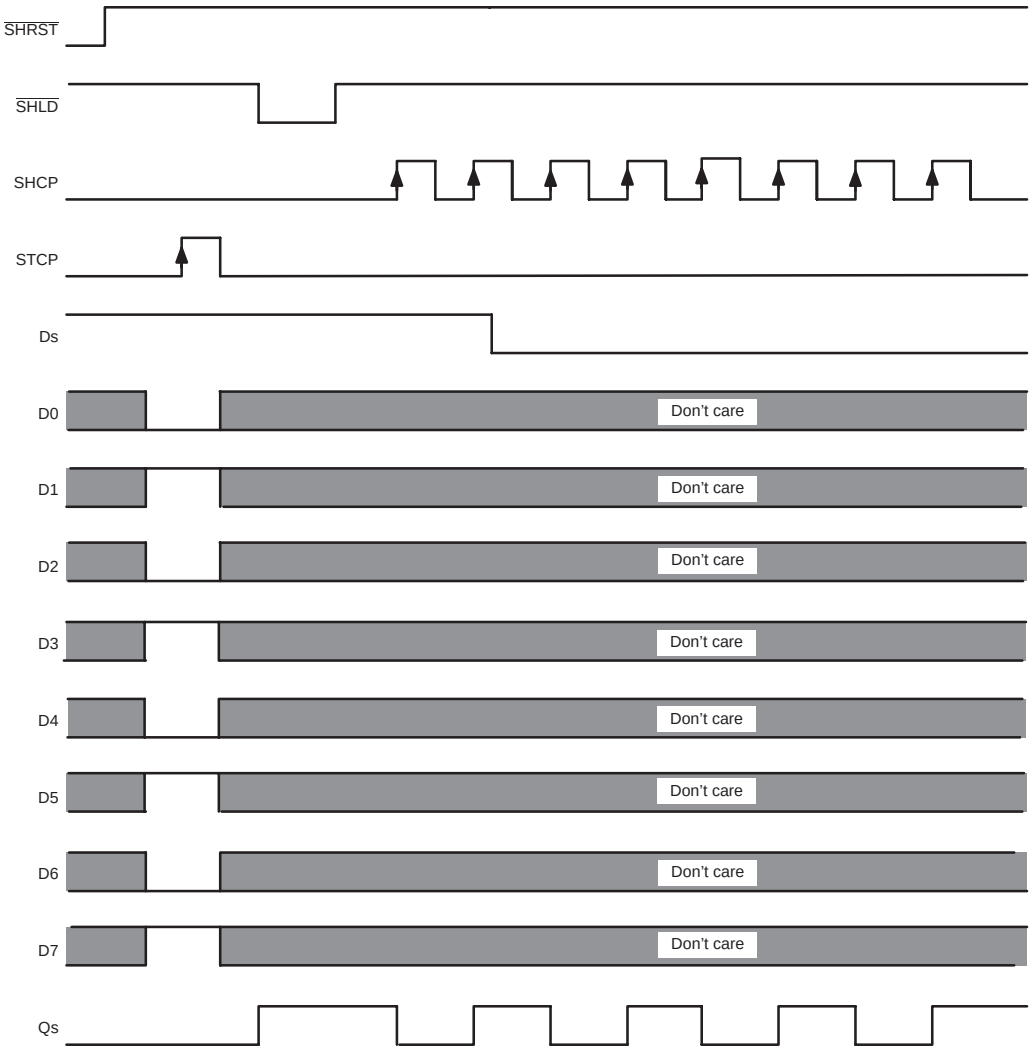
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform NO TAG	120	135		105		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Qs	Waveform NO TAG	7.0 6.0	8.5 7.5	11.0 10.0	6.0 5.5	12.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Qs	Waveform NO TAG	8.0 6.0	9.5 7.5	12.0 10.0	7.0 5.5	13.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Qs	Waveform NO TAG	7.5 8.0	9.5 9.5	11.5 12.0	6.5 7.5	13.0 13.0	ns
t_{PHL}	Propagation delay $\overline{SHRST}$ to Qs	Waveform NO TAG	2.5	5.5	9.0	2.5	9.5	ns

AC SETUP REQUIREMENTS

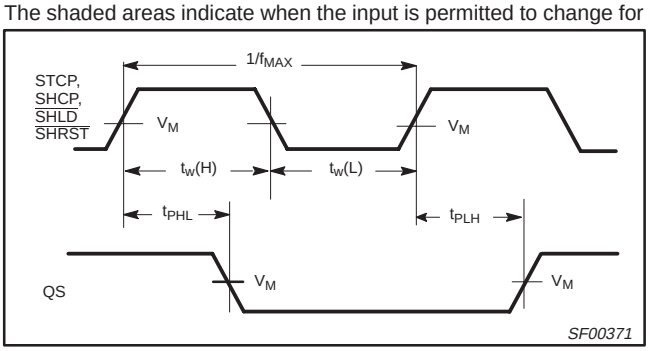
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to STCP	Waveform NO TAG	1.0 1.5			1.5 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to STCP	Waveform NO TAG	2.0 2.0			2.0 3.0		ns
t_s(H) t_s(L)	Setup time, High or Low Ds to SHCP	Waveform NO TAG	1.0 1.5			1.0 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low Ds to SHCP	Waveform NO TAG	1.5 2.0			2.0 2.5		ns
t_s(H)	Setup time, High STCP to $\overline{SHLD}$↑	Waveform 4	8.5			9.0		ns
t_h(L)	Hold time, Low STCP to $\overline{SHLD}$↑ (hold mode)	Waveform NO TAG	0.0			0.0		ns
t_s(H)	Setup time, High $\overline{SHLD}$ to SHCP↑	Waveform NO TAG	6.0			6.5		ns
t_W(H) t_W(L)	SHCP Pulse width High or Low	Waveform NO TAG	4.5 4.5			5.5 4.5		ns
t_W(H) t_W(L)	STCP Pulse width High or Low	Waveform NO TAG	4.5 4.5			5.0 4.5		ns
t_W(L)	$\overline{SHRST}$ Pulse width, Low	Waveform NO TAG	4.5			4.5		ns
t_W(L)	$\overline{SHLD}$ Pulse width, Low	Waveform NO TAG	4.5			4.5		ns
t_{REC}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform NO TAG	2.0			2.5		ns

TYPICAL TIMING DIAGRAM

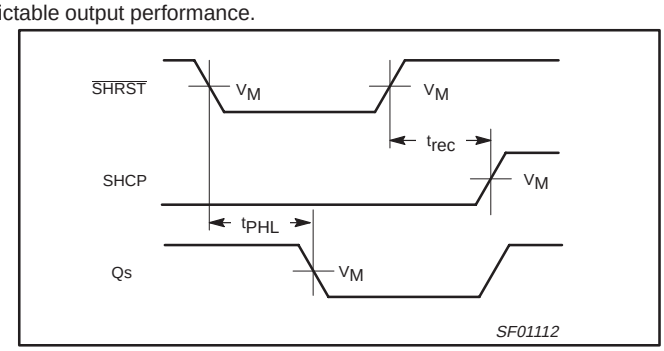


AC WAVEFORMS

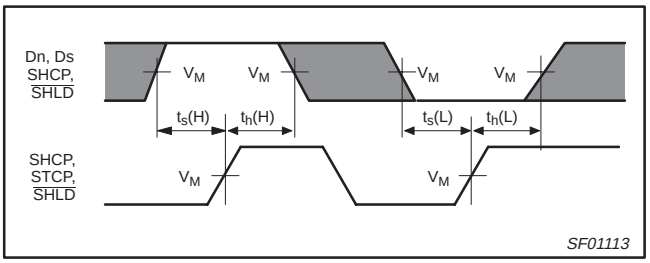
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



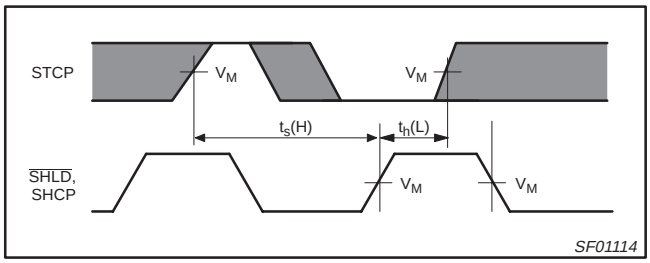
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Widths, and Maximum Clock Frequency, Shift Register Reset and Load Inputs to Serial Data Output



Waveform 2. Propagation Delay, Shift Register Reset and Load Inputs to Serial Data Output, Shift Register Reset and Load Inputs to Shift Register Clock Pulse Input Recovery Time

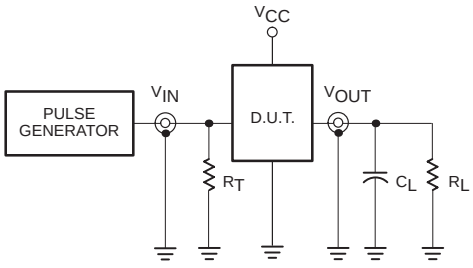


Waveform 3. Setup and Hold Times

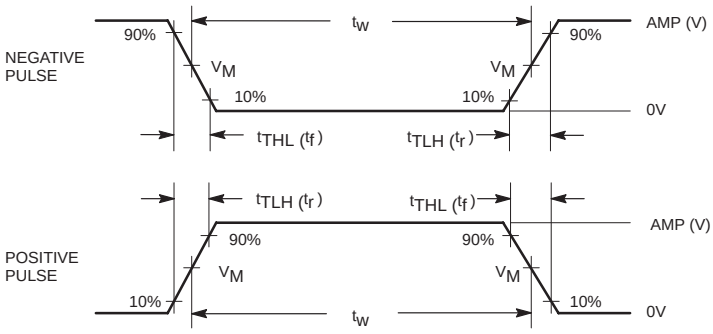


Waveform 4. Setup and Hold Time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

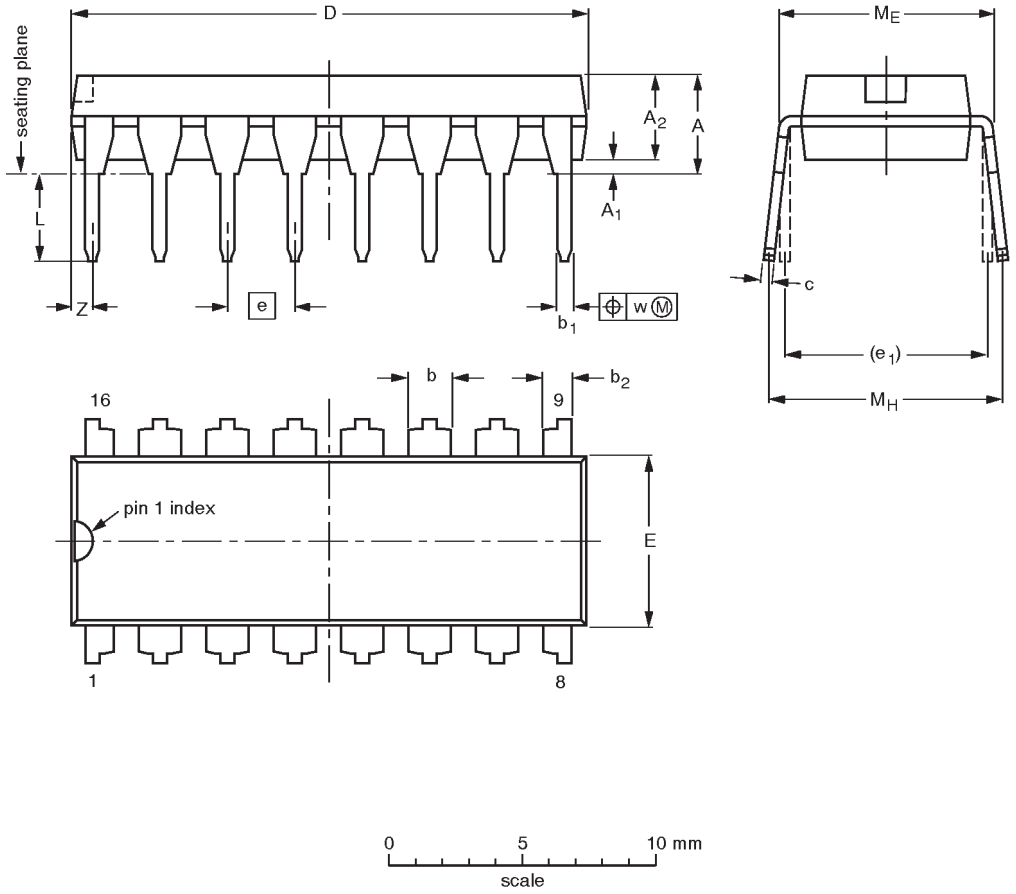
family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SF00006

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

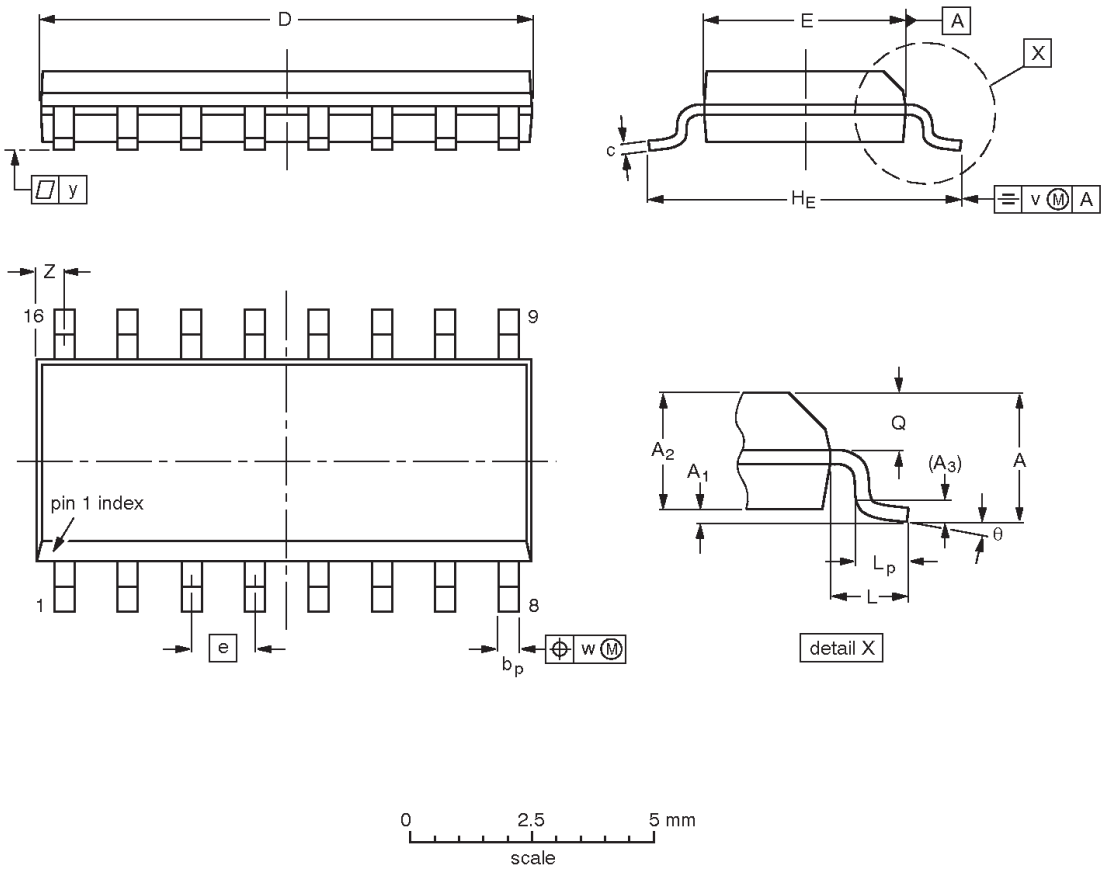
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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