DATA SHEET

74F2952
Registered transceiver, non-inverting (3-State)

74F2953
Registered transceiver, inverting (3-State)

Product specification

IC15 Data Handbook

1989 Sep 22

Philips
Semiconductors

PHILIPS

Transceivers 74F2952, 74F2953

74F2952 Registered transceiver, non-inverting (3-State)
74F2953 Registered transceiver, inverting (3-State)

FEATURES

- 8-bit registered transceivers
- Two 8-bit, back-to-back registers store data moving in both directions between two bidirectional buses
- Separate Clock, Clock Enable and 3-State Enable provided for each register
- 74F2952 non-inverting
- 74F2953 inverting
- AM2952/2953 functional equivalent
- 'A' outputs sink 24mA and source 3mA
- 'B' outputs sink 64mA and source 15mA
- 300 mil wide 24-pin Slim DIP package

DESCRIPTION

The 74F2952 and 74F2953 are 8-bit registered transceivers. Two 8-bit back-to-back registers store data flowing in both directions between two bi-directional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from 'A' inputs to 'B' outputs is the same as for 'B' inputs to 'A' outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F2952	160MHz	105mA
74F2953	160MHz	105mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PACKAGE DRAWING NUMBER
24-pin Plastic Slim DIP (300mil)	N74F2952N, N74F2953N	SOT222-1
24-pin Plastic SOL[1]	N74F2952D, N74F2953D	SOT137-1
28-pin Plastic Leaded Chip Carrier	N74F2952A, N74F2953A	SOT261-2

NOTE:
1. Thermal mounting techniques are recommended. See *SMD Process Applications* for a discussion of thermal consideration for surface mounted devices.

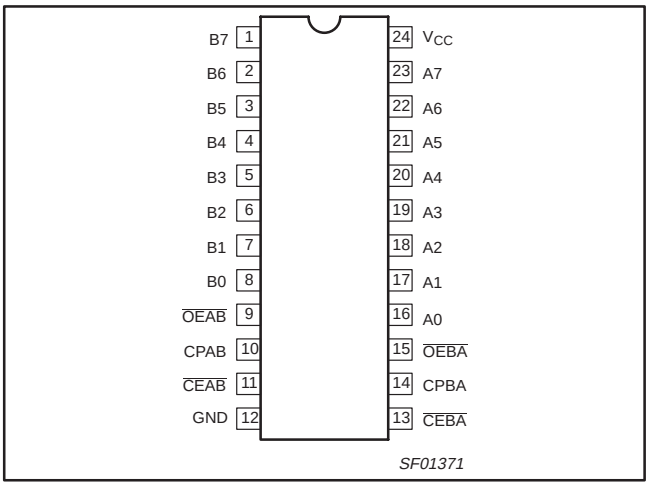
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	Port A, 3-State inputs	3.5/1.0	70µA/0.6mA
B0 – B7	Port B, 3-State inputs	3.5/1.0	70µA/0.6mA
CPAB, CPBA	Clock inputs	1.0/1.0	20µA/0.6mA
$\overline{CEAB}$, $\overline{CEBA}$	Clock Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable inputs	1.0/1.0	20µA/0.6mA
A0 – A7	Port A, 3-State outputs	150/40	3.0mA/24mA
B0 – B7	Port B, 3-State outputs	750/106.7	15mA/64mA

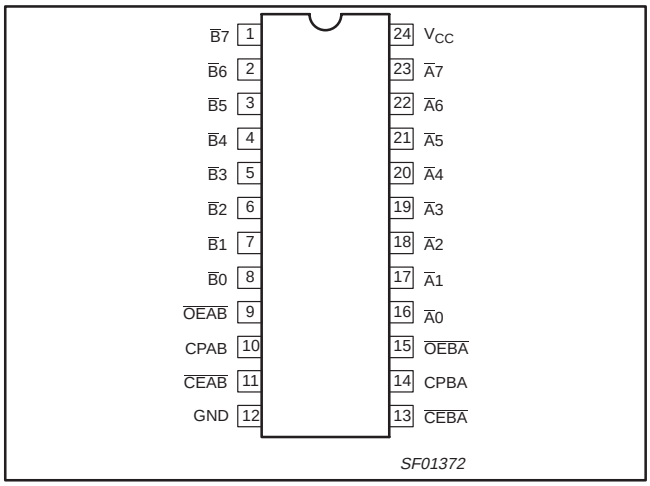
NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATIONS

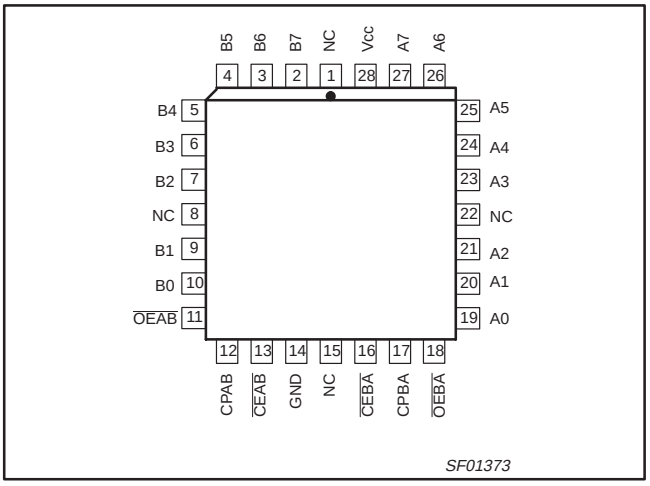
DIP – 74F2952



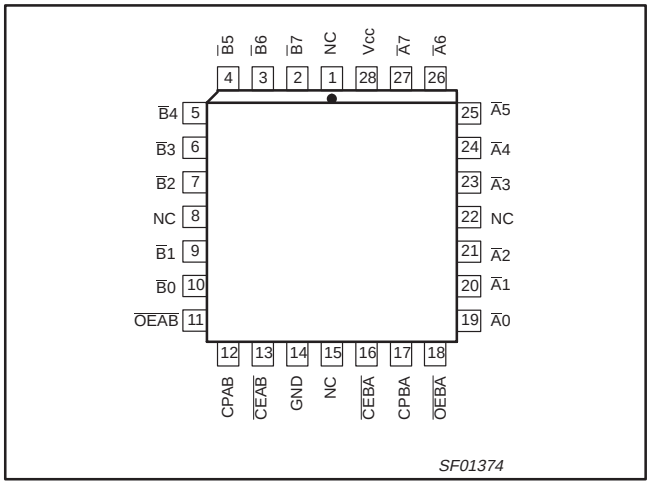
DIP – 74F2953



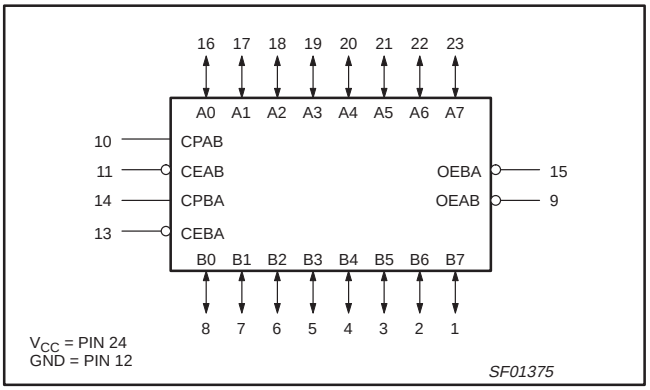
PLCC – 74F2952



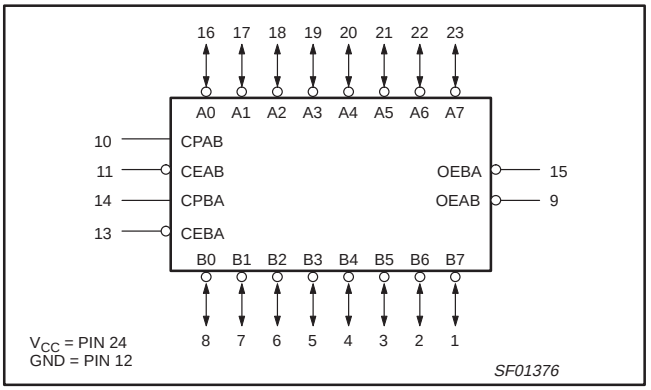
PLCC – 74F2953



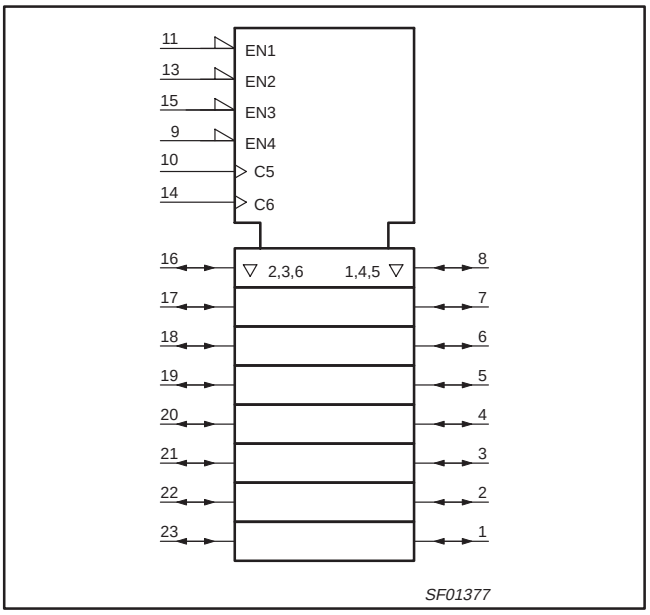
LOGIC SYMBOL – 74F2952



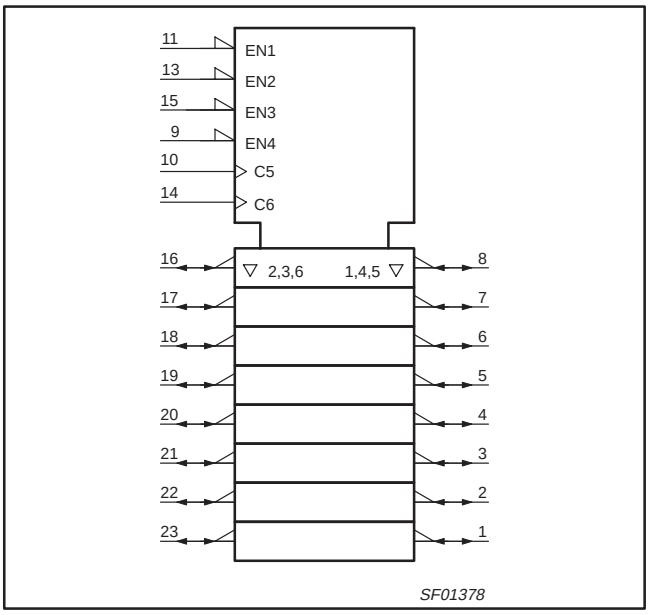
LOGIC SYMBOL – 74F2953



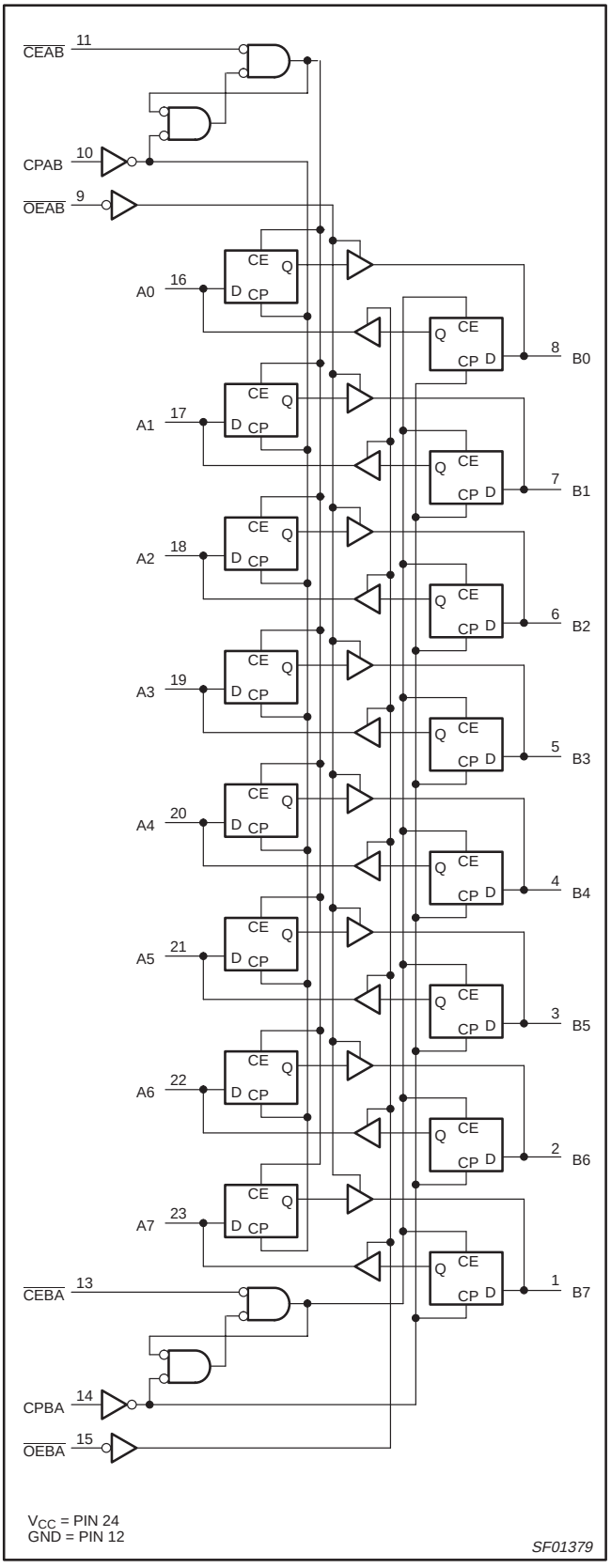
IEC/IEEE SYMBOL – 74F2952



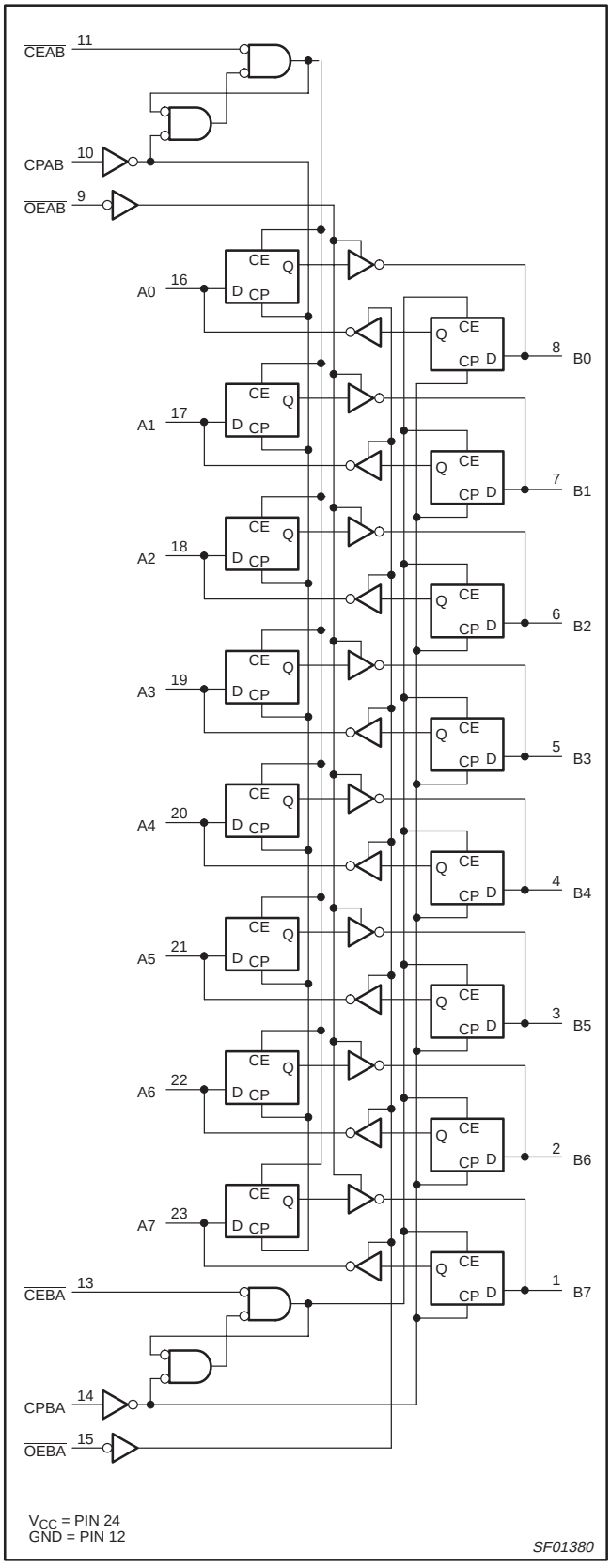
IEC/IEEE SYMBOL – 74F2953



LOGIC DIAGRAM – 74F2952



LOGIC DIAGRAM – 74F2953



FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't Care
XX = AB or BA
NC = No Change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	An or Bn OUTPUTS		OPERATING MODE
$\overline{OEXX}$		74F2952	74F2953	
H	X	Z	Z	Disable outputs
L	L	L	H	Enable outputs
L	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't Care
XX = AB or BA
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0 – A7	48	mA
		B0 – B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A0 – A7			–3	mA
		B0 – B7			–15	mA
I_{OL}	Low-level output current	A0 – A7			24	mA
		B0 – B7			64	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.3		V
		B0–B7		I_{OH} = –15mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10% V_{CC}		0.35	0.50	V
					±5% V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{CPAB}$, $\overline{CPBA}$, $\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A0–A7, B0–B7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{CPAB}$, $\overline{CPBA}$, $\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	$\overline{CPAB}$, $\overline{CPBA}$, $\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A0–A7, B0–B7	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	A0–A7, B0–B7	V_{CC} = MAX, V_O = 0.5V					–600	µA
I_{OS}	Short-circuit output current[3]	A0–A7	V_{CC} = MAX, V_O = 0V			–60		–150	mA
		B0–B7				–100		–225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	140	mA
		i_{CCL}					120	175	mA
		I_{CCZ}					105	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

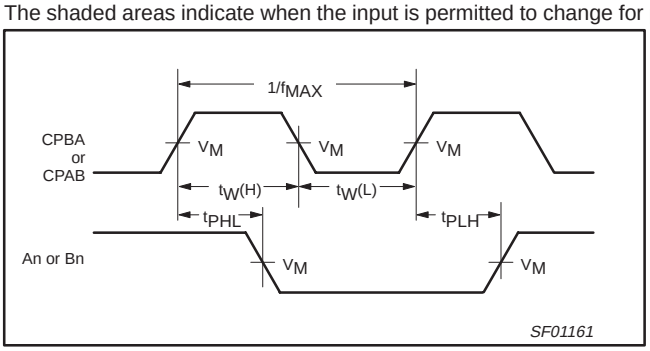
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	145	160		135		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to An or Bn	Waveform 1	3.0 3.5	5.0 6.0	7.5 8.5	2.5 3.5	8.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn	Waveform 3 Waveform 4	2.0 3.5	4.5 6.0	7.0 9.5	2.0 3.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn	Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	8.0 6.5	1.5 1.0	9.0 7.0	ns

AC SETUP REQUIREMENTS

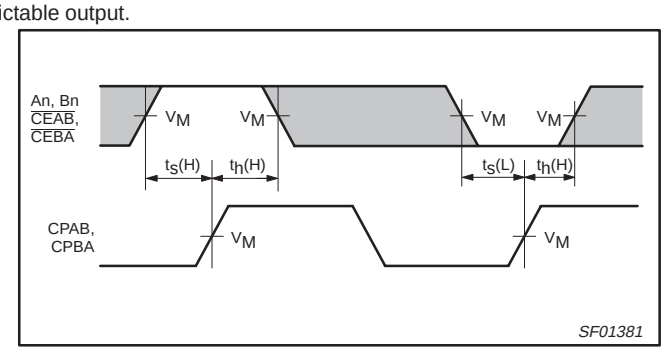
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = +5V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5V ± 10% C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low An or Bn to CPAB or CPBA	74F2952	Waveform 2	4.5 3.5			5.0 4.0		ns
t_s(H) t_s(L)	Setup time, High or Low An or Bn to CPAB or CPBA	74F2953	Waveform 2	4.0 3.5			4.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low An or Bn to CPAB or CPBA		Waveform 2	0.0 0.0			0.0 0.0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA		Waveform 2	0.0 4.0			0.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{CEAB}$, $\overline{CEBA}$ to CPAB, CPBA		Waveform 2	2.5 2.5			2.5 3.0		ns
t_w(H) t_w(L)	CPAB or CPBA pulse width, High or Low		Waveform 1	3.0 3.5			3.0 3.5		ns

AC WAVEFORMS

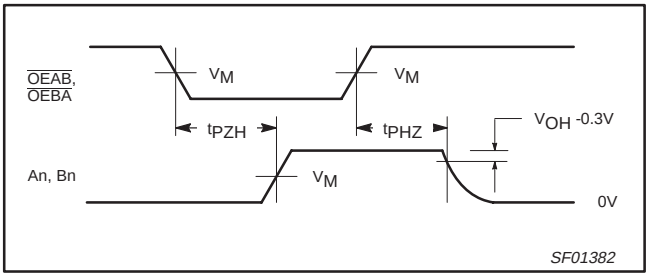
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output.



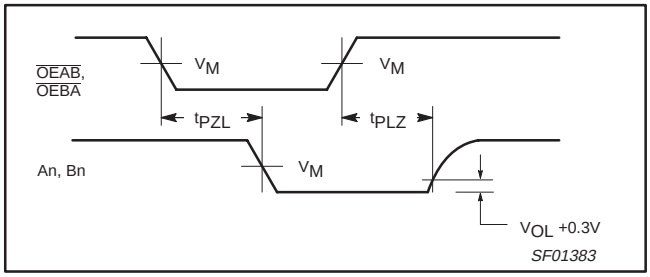
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

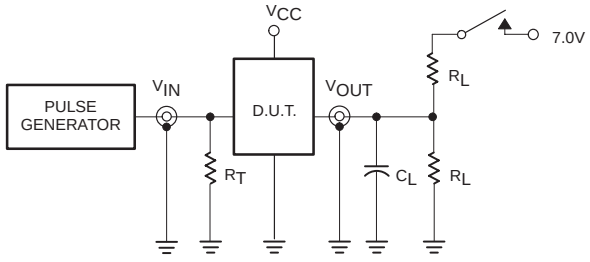


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

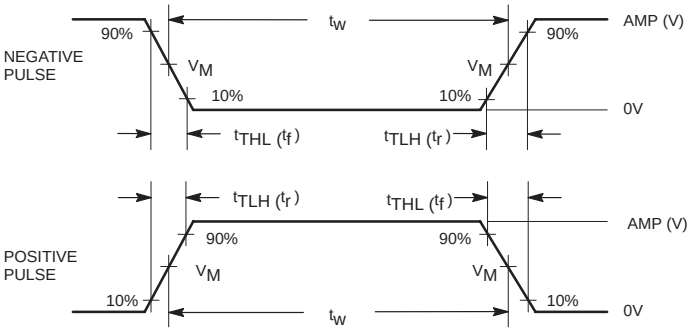


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

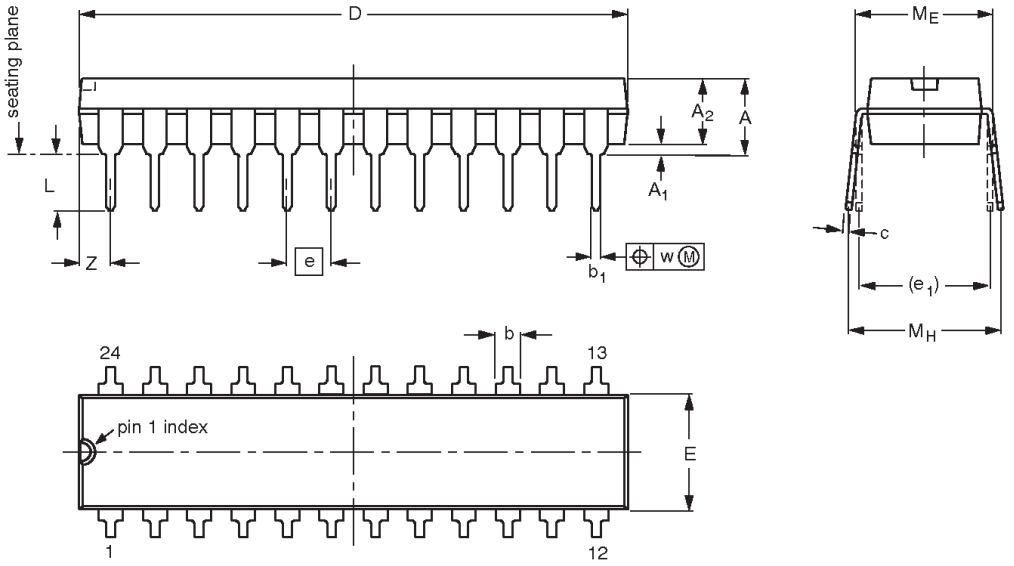
DEFINITIONS:

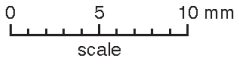
R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

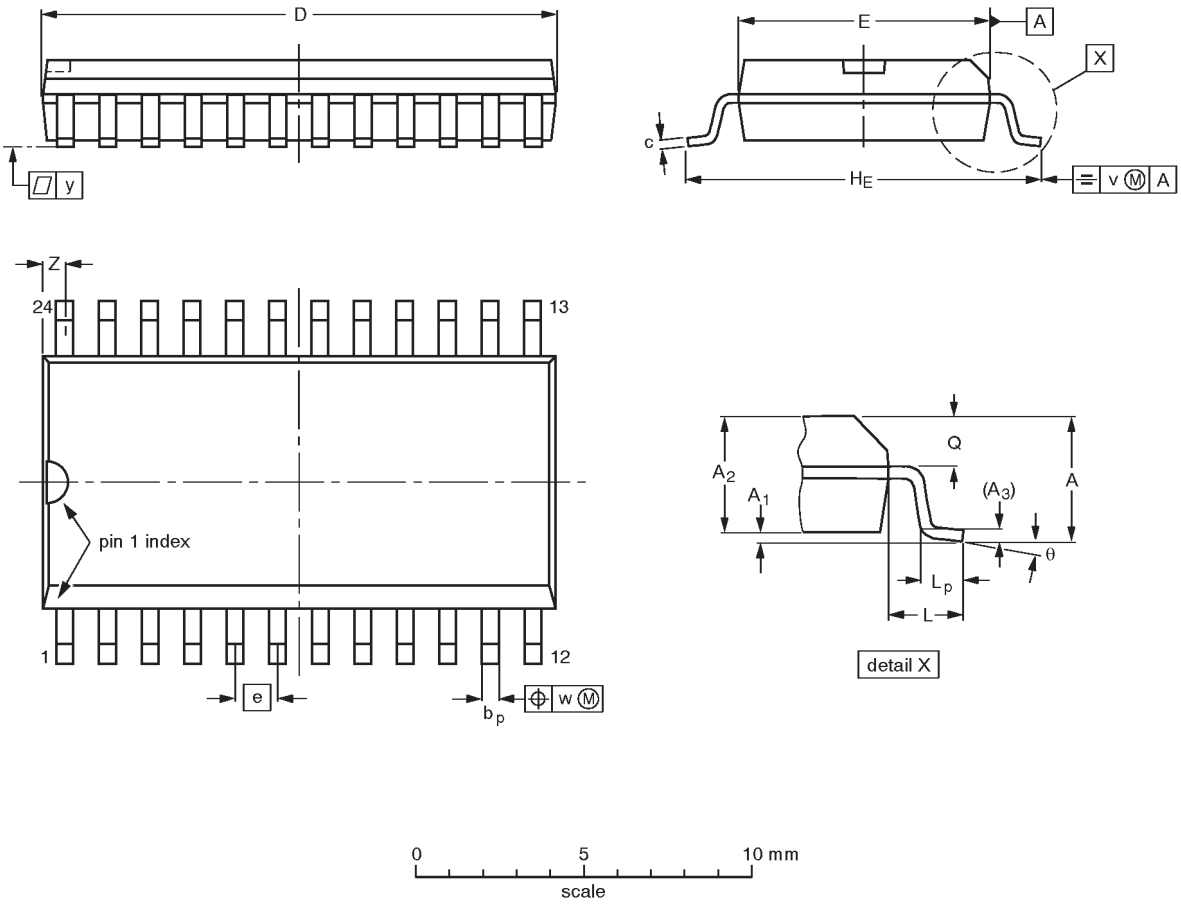
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

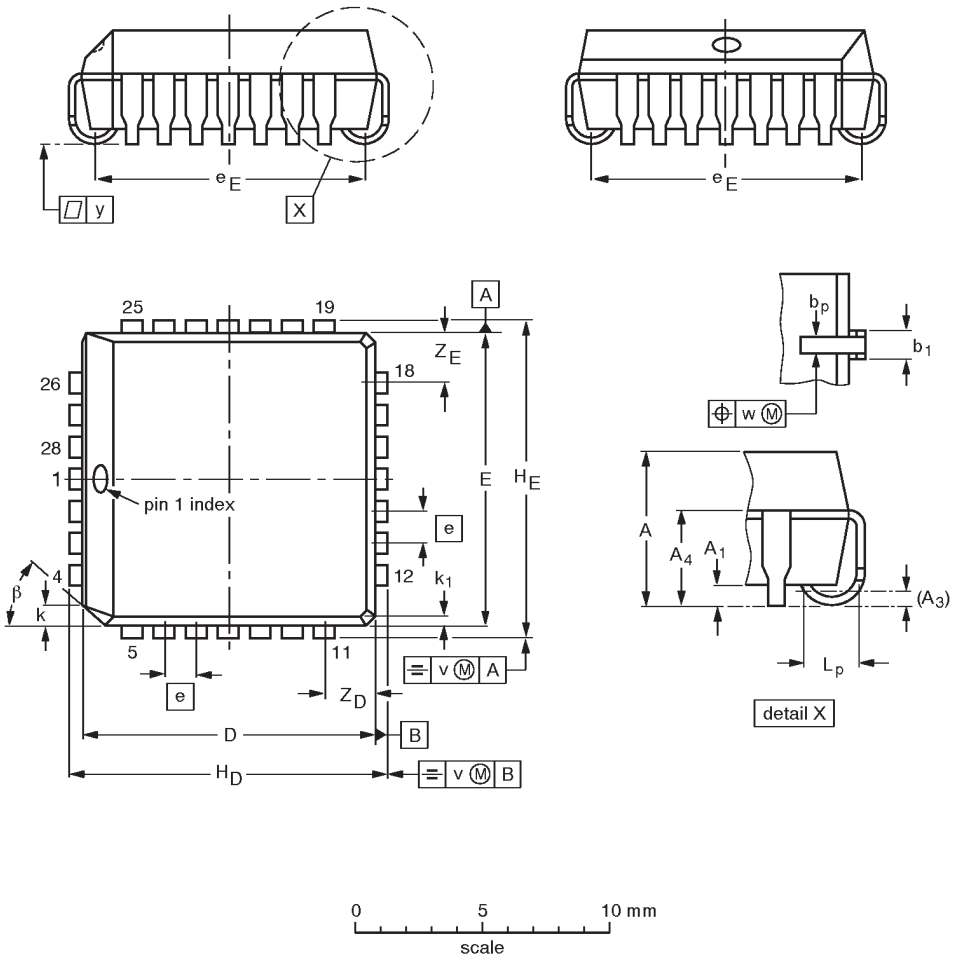
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

PLCC28: plastic leaded chip carrier; 28 leads SOT261-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-2						~~92-11-17~~ 95-02-25

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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