National Semiconductor

PRELIMINARY
May 1994

54/74ETL16245 16-Bit Data Transceiver with Incident Wave Switching

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General Description

The 54/74ETL16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE® outputs designed with incident wave switching, live insertion support and enhanced noise margin for TTL backplane applications.

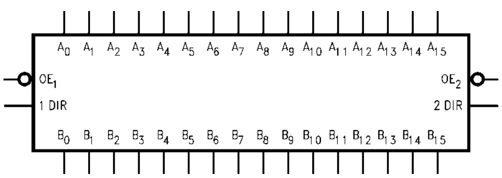
Both the A and B ports include a bus hold circuit to latch the output to the value last forced on that pin.

The B port of this device includes 25Ω series output resistors, which minimize undershoot and ringing.

Features

- Supports the VME64 ETL specification
- Functionally and pin compatible with industry standard TTL 16245 SSOP pinout
- Improved TTL-compatible input threshold range
- High drive TTL-compatible outputs ($I_{OH} = -60$ mA, $I_{OL} = 90$ mA)
- Supports 25Ω incident wave switching on the A port
- BiCMOS design significantly reduces power dissipation.
- Distributed V_{CC} and GND pin configuration minimizes high-speed switching noise
- 25Ω series-dampening resistor on B-port
- Available in 48-pin SSOP and ceramic flatpak
- Guaranteed output skew
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection

Logic Symbol



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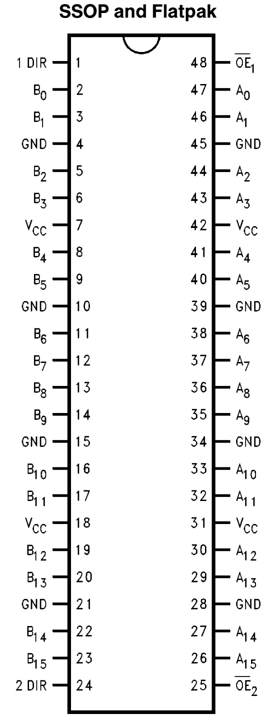
Pin Description

Pin Names	Description
DIR	Transmit/Receive Input
$\overline{OE}$	Output Enable Input (Active LOW)
A_n	Backplane Bus Data
B_n	Local Bus Data

Connection Diagram

Pin Assignment for SSOP and Flatpak



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RRD-B30M105/Printed in U. S. A.

Functional Description

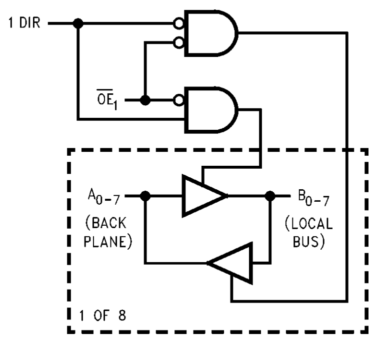
The device uses byte-wide Direction (DIR) control and Output Enable ($\overline{OE}$) controls. The DIR inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable the A and the B ports.

The part contains active circuitry which keeps all outputs disabled when V_{CC} is less than 2.2V to aid in live insertion applications.

Truth Table (Each 8-bit Section)

Inputs		Operation
$\overline{OE}$	DIR	
L	L	A Data to B Bus
L	H	B Data to A Bus
H	X	Isolation

Logic Diagrams (Positive Logic)



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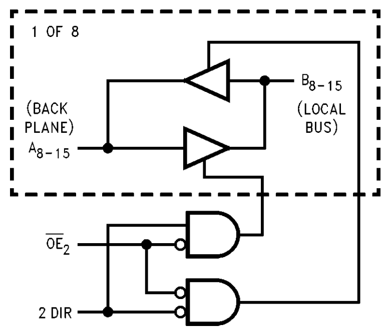

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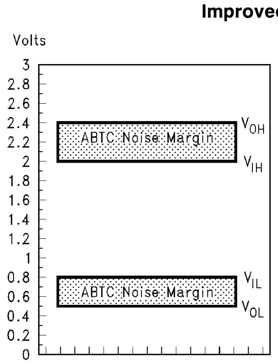
ETL's Improved Noise Immunity

TTL input thresholds are typically determined by temperature-dependent junction voltages which result in worst case input thresholds between 0.8V and 2.0V. By contrast, ETL provides greater noise immunity because its input thresholds are determined by current mode input circuits similar to those used for ECL or BTL. ETL's worst case input thresholds, between 1.4V and 1.6V, are compensated for temperature, voltage and process variations.

Incident Wave Switching

When TTL logic is used to drive fully loaded backplanes, the combination of low backplane bus characteristic impedance, wide TTL input threshold range and limited TTL drive generally require multiple waveform reflections before a valid signal can be received across the backplane. The VME International Trade Association (VITA) defined ETL to provide incident wave switching which increases the data transfer rate of a VME backplane and extends the life of VME applications. TTL compatibility with existing VME backplanes and modules was maintained.

Improved Input Threshold Characteristics of ETL



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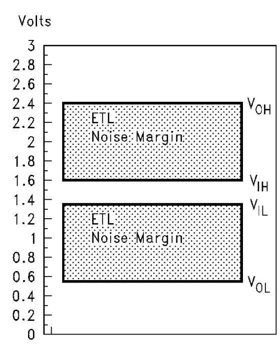
ABTC Worst Case V_{OUT}–V_{IN}



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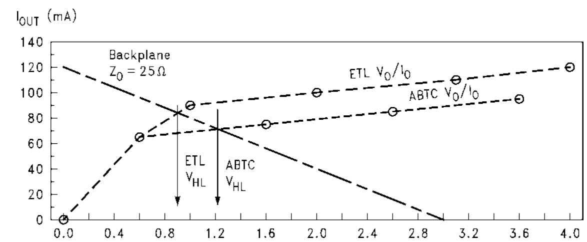
ETL Worst Case V_{OUT}–V_{IN}

Incident Wave Switching (Continued)

To demonstrate the incident wave switching capability, consider a VME application. A VME bus must be terminated to +2.94V with 190Ω at each end of its 21 card backplane. The surge impedance presented by a fully loaded VME backplane is approximately 25Ω. If the output voltage/current of an ABTC driver is plotted with this load, the intersection at 1.2V for a falling edge and at 1.6V for a rising edge does not reach the worst case input threshold of a second ABTC circuit. This is shown in the two figures below. However, an ETL driver located at one end of the backplane is able to provide incident wave switching because it has a higher drive and a tighter input threshold.

Estimated ETL/ABTC Initial Falling Edge Step



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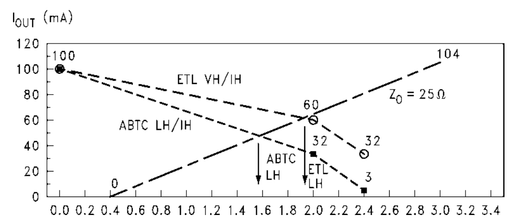
Because ETL has a much more precise input threshold region, an ETL receiver will interpret its predicted falling input of 0.85V as a logic ZERO and the initial rising edge of 1.9V as a logic ONE. This comparison is for the case of a 25Ω surge impedance backplane driven from one end.

Estimated ETL/ABTC Initial Rising Edge Step



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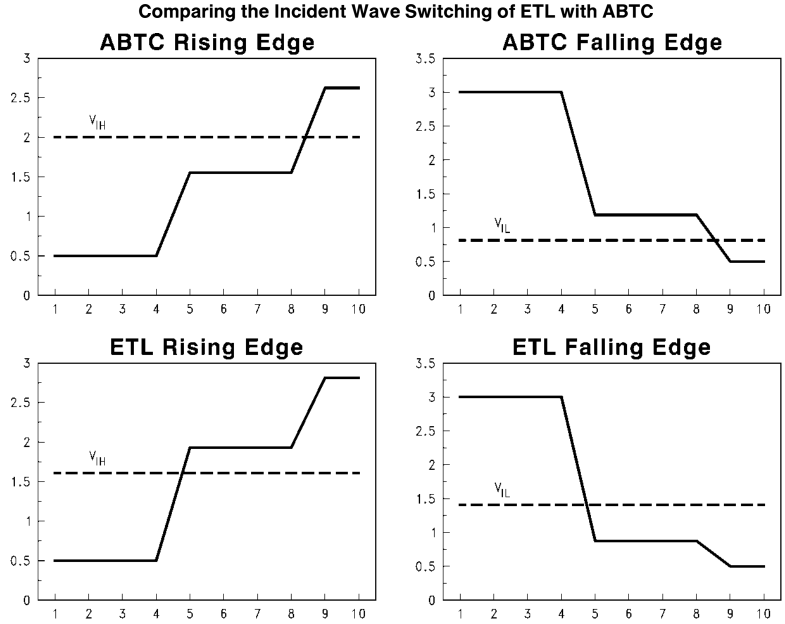
The resulting ABTC and ETL waveform predictions and their input thresholds are compared below. This shows how ETL can achieve backplane speeds not always possible with conventional TTL compatible logic families.

Comparing the Incident Wave Switching of ETL with ABTC



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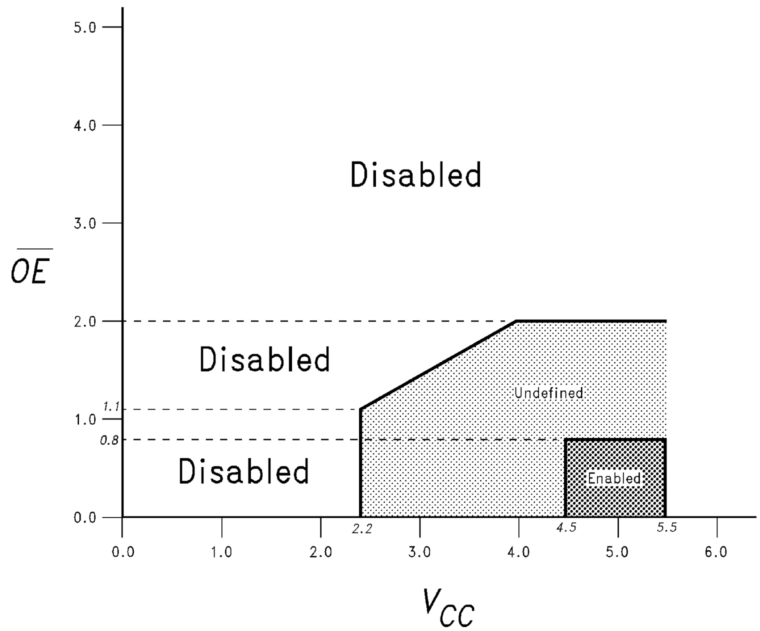
Incident Wave Switching (Continued)

The figure V_{CC} Power-up Critical Voltages shows the relationship between $\overline{OE}$ and V_{CC} while power is being applied and removed.



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V_{CC} and $\overline{OE}$ Power-up Relationship

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−50 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	128 mA
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(Δt/ΔV)
Data Input	20 ns/V
Enable Input	50 ns/V

DC Electrical Characteristics

Symbol	Parameter		ETL16245 Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	$\overline{OE}$	2.0			V		Recognized HIGH Signal
		Other Inputs	1.6					
V_{IL}	Input LOW Voltage	$\overline{OE}$			0.8	V		Recognized LOW Signal
		Other Inputs			1.4			
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	$I_{IN} = -18$ mA ($\overline{OE}_n$, DIR)
V_{OH}	Output HIGH Voltage	B Port	$V_{CC} - 1$ 2.4 2.0			V V V	Min	$I_{OH} = -100\ \mu A$ $I_{OH} = -1$ mA $I_{OH} = -12$ mA
		A Port	$V_{CC} - 1$ 2.4 2.0			V V V	Min	$I_{OH} = -1$ mA $I_{OH} = -32$ mA $I_{OH} = -60$ mA
V_{OL}	Output LOW Voltage	B Port			0.4 0.8	V V	Min	$I_{OL} = 1$ mA $I_{OL} = 12$ mA
		A Port			0.55 0.9	V V	Min	$I_{OL} = 64$ mA $I_{OL} = 90$ mA
I_{HOLD}	Bus Hold Current	A Port, B Port	100			μA	Min	$\overline{OE}$ = HIGH, $V_O = 0.8V$
			−100					$\overline{OE}$ = HIGH, $V_O = 2.0V$
I_{OFF}	Output Current, Power Down				100	μA	0.0	V_{CC} Bias = 0V V_I or $V_O \leq 4.5V$
I_I	Input Current Control Pins	54ETL			±10	μA	5.5	$V_{IN} = 0$ or V_{CC}
		74ETL			±5	μA	5.5	$V_{IN} = 0$ or V_{CC}
$I_{IH} + I_{OZH}$	Output Leakage Current				50	μA	5.5	$V_{OUT} = 2.7V$, $\overline{OE} = 2.0V$
$I_{IL} + I_{OZL}$	Output Leakage Current				−50	μA	5.5	$V_{OUT} = 0.5V$, $\overline{OE} = 2.0V$

DC Electrical Characteristics (Continued)

Symbol	Parameter	ETL16245			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{CCH}	Power Supply Current			40	mA	Max	All Outputs HIGH, $\overline{OE}$ = LOW, DIR = HIGH or LOW
I_{CCL}	Power Supply Current			80	mA	Max	All Outputs LOW, $\overline{OE}$ = LOW, DIR = HIGH or LOW
I_{CCZ}	Power Supply Current			40	mA	Max	$\overline{OE}$ = HIGH All Others at V_{CC} or GND DIR = HIGH or LOW
I_{CCD}	Dynamic I_{CC} No Load (Note 1)			0.15	mA/ MHz	Max	Outputs Open $\overline{OE}_n$ = GND, DIR = HIGH One Bit Toggling, 50% Duty Cycle
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}			1.0	V	5.0	T_A = 25°C (Note 2) C_L = 50 pF; R_L = 500Ω
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.4			V	5.0	T_A = 25°C (Note 2) C_L = 50 pF; R_L = 500Ω
V_{OHV}	Minimum High Level Dynamic Output Voltage (Note 1)		2.7		V	5.0	T_A = 25°C (Note 4) C_L = 50 pF; R_L = 500Ω
V_{IHD}	Minimum High Level Dynamic Input Voltage (Note 1)	2.0	1.5		V	5.0	T_A = 25°C (Note 3) C_L = 50 pF; R_L = 500Ω
V_{ILD}	Maximum Low Level Dynamic Input Voltage (Note 1)		1.2	0.8	V	5.0	T_A = 25°C (Note 3) C_L = 50 pF; R_L = 500Ω

Note 1: Guaranteed, but not tested.

Note 2: Max. number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 3: Max. number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 4: Max. number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	74ETL			54ETL		74ETL		Units	Fig. No.
		T_A = +25°C V_{CC} = +5V			T_A = −55°C to +125°C V_{CC} = 4.5V–5.5V		T_A = −40°C to +85°C V_{CC} = 4.5V–5.5V			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n	1.5 1.5		7.0 7.0			1.5 1.5	7.0 7.0	ns	1, 2, 4
t_{PLH} t_{PHL}	Propagation Delay B_n to A_n	1.5 1.5		7.0 7.0			1.5 1.5	7.0 7.0	ns	1, 2, 4
t_{PZH} t_{PZL}	Output Enable Time	1.0 1.0		7.0 7.0			1.0 1.0	7.0 7.0	ns	1, 2, 3
t_{PHZ} t_{PLZ}	Output Disable Time	1.0 1.0		7.0 7.0			1.0 1.0	7.0 7.0	ns	1, 2, 3
t_r	Rise Time 1V → 2V, A_n Outputs	1.2		3.0			1.2	3.0	ns	1, 2, 4
t_f	Fall Time 2V → 1V, A_n Outputs	1.2		3.0			1.2	3.0	ns	1, 2, 4

Skew

Symbol	Parameter	74ETL	54ETL	Units	Conditions
		$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ 16 Outputs Switching	$T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V–5.5V$ 16 Outputs Switching		
		Max	Max		
t_{OHS} (Notes 1, 2)	Pin-to-Pin Skew LH/HL An to Bn	1.3		ns	*Figures 1, 2, 4*
t_{OHS} (Notes 1, 2)	Pin-to-Pin Skew LH/HL Bn to An	1.3		ns	*Figures 1, 2, 4*
t_{PS} (Notes 1, 2)	Duty Cycle Skew Bn to An	2.0		ns	*Figures 1, 2, 4*
t_{PS} (Notes 1, 2)	Duty Cycle Skew An to Bn	2.0		ns	*Figures 1, 2, 4*

VME Extended Skew

Symbol	Parameter	74ETL	54ETL	Units	Conditions
		$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ 16 Outputs Switching	$T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V–5.5V$ 16 Outputs Switching		
		Max	Max		
t_{PV} (Notes 1, 2)	Device-to-Device Skew LH/HL Transitions Bn to An	4.0		ns	*Figures 1, 2, 4*
t_{CP} (Notes 1, 2)	Device-to-Device Skew LH/HL Transitions An to Bn	2.5		ns	*Figures 1, 2, 4*
t_{CP} (Note 1, 3)	Change in Propagation Delay with Load Bn to An	4.0		ns	*Figures 1, 2, 4*
t_{CPV} (Notes 1, 2, 3)	Device-to-Device, Change in Propagation Delay with with Load Bn to An	6.0		ns	*Figures 1, 2, 4*

Note 1: Skew is defined as the absolute difference in delay between two outputs. The specification applies to any outputs switching HIGH to LOW, LOW to HIGH, or any combination switching HIGH-to-LOW or LOW-to-HIGH. This specification is guaranteed but not tested.

Note 2: This is measured with both devices at the same value of V_{CC} ±1% and with package temperature differences of 20°C from each other.

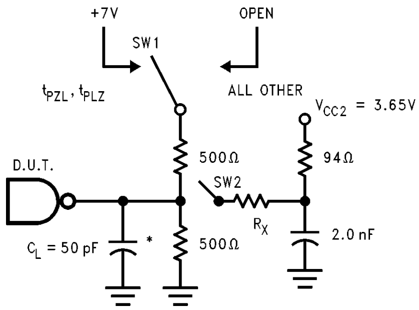
Note 3: This is measured with Rx in *Figure 1* at 13Ω for one unit and at 56Ω for the other unit.

Capacitance

Symbol	Parameter	Typ	Max	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5	8	pF	$V_{CC} = 0.0V$ ($\overline{OE}_n$, DIR)
$C_{I/O}$ (Note 1)	Output Capacitance	9	12	pF	$V_{CC} = 5.0V$ (A_n)

Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

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FIGURE 1. Standard AC Test Load

Note 1: Defined to emulate the range of VME bus transmission line loading as a function of board population and driver location. Rx = 13Ω, 26Ω or 56Ω depending on test.

Test	Port	SW1	SW2	Rx
t_{PHZ}, t_{PLZ}	A, B	+7	Open	
t_{PZH}, t_{PZL}	A, B	+7	Open	
t_{PLH}, t_{PHL}	A	Open	Closed	26
t_{PLH}, t_{PHL}	B	Open	Open	
t_r, t_f	A	Open	Closed	26
t_{PV}	A	Open	Closed	26
t_{CP}	B	Open	Open	
t_{CP}	A	Open	Closed	13 then 56
t_{CPV}	A	Open	Closed	13 and 56

FIGURE 1a

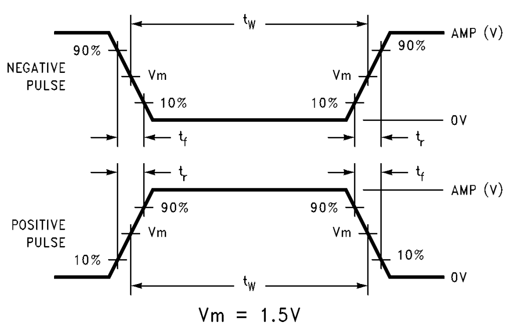

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FIGURE 2. Input Pulse Requirements

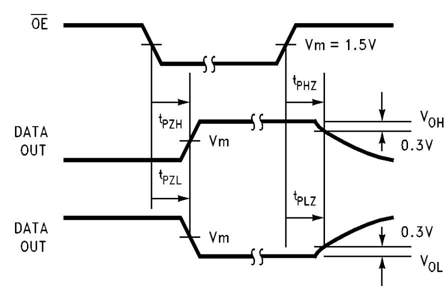

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FIGURE 3. TRI-STATE Output HIGH and LOW Enable and Disable Times

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2a. Test Input Signal Requirements

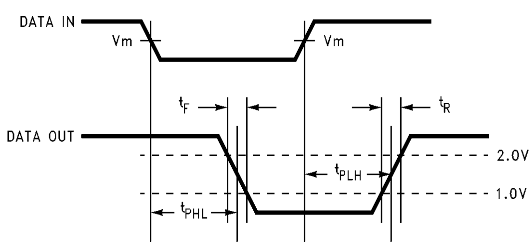

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FIGURE 4. Rise, Fall Time and Propagation Delay Waveforms

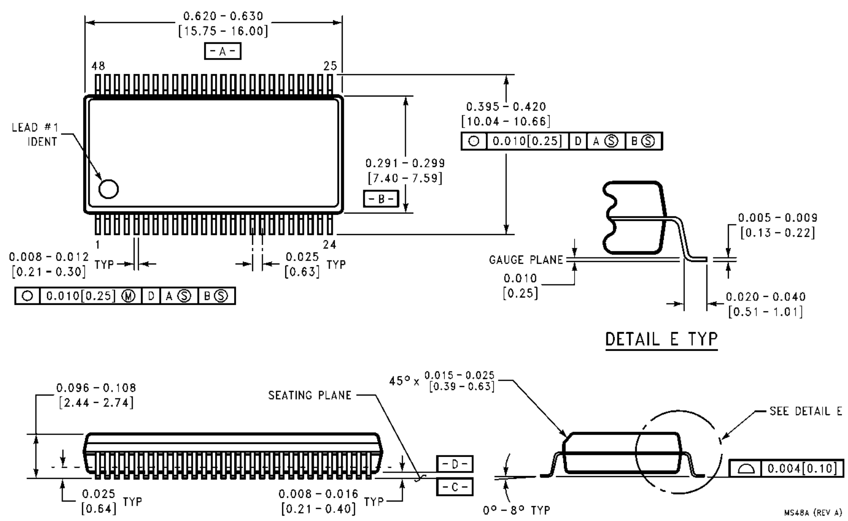
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

54/74 ETL16245 SS C X

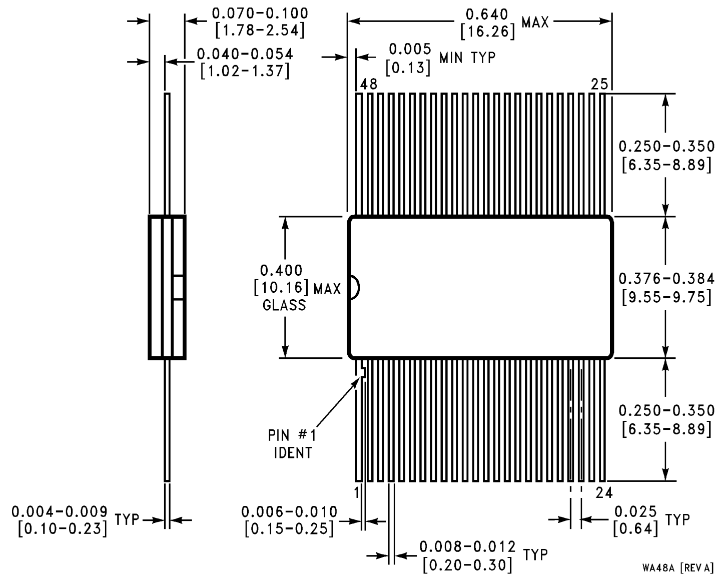
- **Temperature Range Family**
  - VME74 = Commercial
  - VME54 = Military
- **Device Type**
- **Package Code**
  - SS = Small Outline (SSOP)
  - FPFP = Fine Pitch Flatpak
- **Temperature Range**
  - C = Commercial (−40°C to +85°C)
  - M = Military (−55°C to +125°C)
- **Special Variations**
  - X = Devices shipped in 13″ reels
  - QB = Military grade device with environmental and burn-in processing shipped in tubes.

Physical Dimensions inches (millimeters)



48-Lead SSOP (0.300″ Wide) (SS)
NS Package Number MS48A

Physical Dimensions inches (millimeters) (Continued)



48-Pin Ceramic Flatpak (FPFP)
NS Package Number WA48A

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