DATA SHEET

74AUC1G08
Single 2-input AND gate

Preliminary specification
File under Integrated Circuits, IC24

2002 Nov 12

Philips
Semiconductors

PHILIPS

Single 2-input AND gate 74AUC1G08

FEATURES

- Wide supply voltage range from 0.8 to 2.7 V
- Performance optimised for V_{CC} = 1.8 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD76 (1.65 to 1.95 V)
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- 8 mA output drive (V_{CC} = 1.65 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- 3.3 V tolerant inputs/outputs
- SC-88A and SC-74A package.

DESCRIPTION

The 74AUC1G08 is a high-performance, low-power, low-voltage, Si-gate CMOS device.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging current backflow through the device when it is powered down.

The 74AUC1G08 provides the single 2-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; input slewrate ≥ 1 V/ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay inputs A and B to output Y	V_{CC} = 0.8 V; C_L = 15 pF; R_L = 2 kΩ	4.7	ns
		V_{CC} = 1.2 V; C_L = 15 pF; R_L = 2 kΩ	1.9	ns
		V_{CC} = 1.5 V; C_L = 15 pF; R_L = 2 kΩ	1.4	ns
		V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	1.4	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	1.2	ns
C_I	input capacitance		4	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 1.8 V; notes 1 and 2	14	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74AUC1G08GW	–40 to +85 °C	5	SC-88A	plastic	SOT353	FE
74AUC1G08GV	–40 to +85 °C	5	SC-74A	plastic	SOT753	F08

PINNING

PIN	SYMBOL	DESCRIPTION
1	B	data input B
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V_{CC}	supply voltage

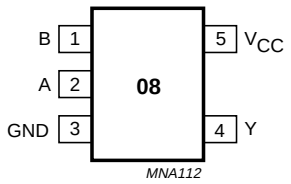


Fig.1 Pin configuration.

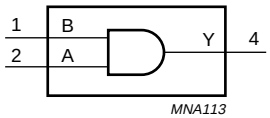


Fig.2 Logic symbol.

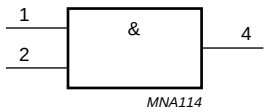


Fig.3 IEE/IEC logic symbol.

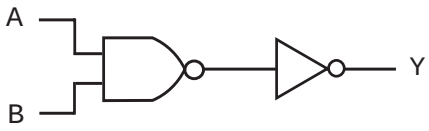


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0.8	2.7	V
V_I	input voltage		0	2.7	V
V_O	output voltage	active mode	0	V_{CC}	V
		V_{CC} = 0 V; Power-down mode	0	2.7	V
T_{amb}	operating ambient temperature		–40	+85	°C
t_r, t_f ($\Delta t/\Delta f$)	input rise and fall times		0	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+3.6	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage	note 1	–0.5	+3.6	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	active mode; notes 1 and 2	–0.5	V_{CC} + 0.5	V
		Power-down mode; notes 1 and 2	–0.5	+3.6	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±60	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +85 °C	–	250	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} =0 (Powered-down mode), the output voltage can be 2.7 V in normal operation.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			UNIT
		OTHER	V_{CC} (V)	–40 to +85			
				MIN.	TYP.(1)	MAX.	
V_{IH}	HIGH-level input voltage		0.8	V_{CC}	–	–	V
			1.1 to 2.3	$0.65 \times V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
V_{IL}	LOW-level input voltage		0.8	–	–	GND	V
			1.1 to 2.3	–	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -100$ µA	0.8 to 2.7	$V_{CC} - 0.1$	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -700$ µA	0.8	–	0.55	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -3$ mA	1.1	$V_{CC} - 0.3$	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -5$ mA	1.5	$V_{CC} - 0.4$	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8$ mA	1.65	$V_{CC} - 0.45$	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -9$ mA	2.3	1.8	–	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 100$ µA	0.8 to 2.7	–	–	0.2	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 700$ µA	0.8	–	0.25	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 3$ mA	1.1	–	–	0.3	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 5$ mA	1.5	–	–	0.4	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8$ mA	1.65	–	–	0.45	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 9$ mA	2.3	–	–	0.6	V
I_I	input leakage current	$V_I = V_{CC}$ or GND	0 to 2.7	–	±0.1	±5	µA
I_{off}	power OFF leakage current	V_I or V_O = 2.7 V	0	–	±0.1	±10	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	0.8 to 2.7	–	0.1	10	µA

Note

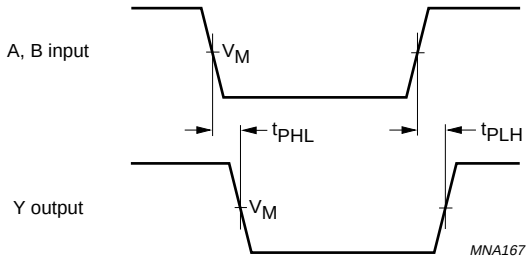
1. All typical values are measured at T_{amb} = 25 °C.

AC CHARACTERISTICS

GND = 0 V; input slewrate ≥ 1 V/ns.

SYMBOL	PARAMETER	TEST CONDITIONS			T_{amb} (°C)			UNIT
		WAVEFORMS	V_{CC} (V)	C_L(pF)	–40 to +85			
					MIN.	TYP.	MAX.	
t_{PHL}/t_{PLH}	propagation delay inputs A and B to output Y	see Figs 5 and 6	0.8	15	–	4.7		ns
			1.1 to 1.3	15	0.9	1.9	3.3	ns
			1.4 to 1.6	15	0.6	1.4	2.3	ns
			1.65 to 1.95	30	0.7	1.4	2.4	ns
			2.3 to 2.7	30	0.5	1.2	2.0	ns

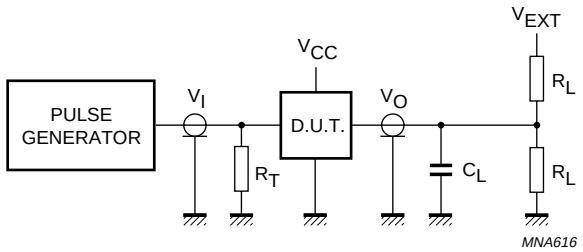
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	Slewrate
0.8 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≥ 1 V/ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 Inputs A, B to output Y propagation delay times.



				V_{EXT}		
V_{CC}	**V_I**	**C_L**	**R_L**	**T_{PLH}/T_{PHL}**	**T_{PZH}/T_{PHZ}**	**T_{PZL}/T_{PLZ}**
<1.65 V	V_{CC}	15 pF	2 kΩ	open	GND	$2 \times V_{CC}$
1.65 to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 to 2.7 V	V_{CC}	30 pF	0.5 kΩ	open	GND	$2 \times V_{CC}$

Definitions for test circuits:

R_L = Load resistor.

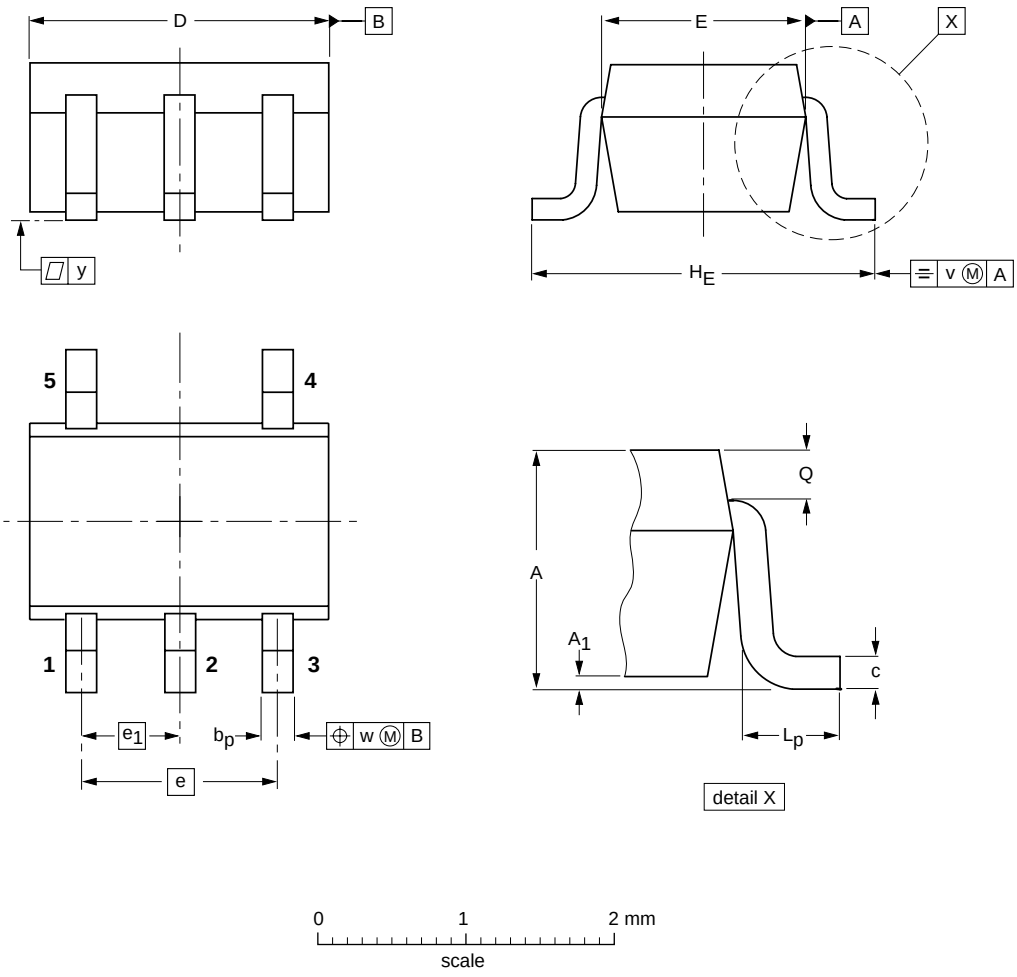
C_L = Load capacitance including jig and probe capacitance (see Chapter “AC characteristics”).

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.6 Load circuitry for switching times.

PACKAGE OUTLINE

Plastic surface mounted package; 5 leads **SOT353**

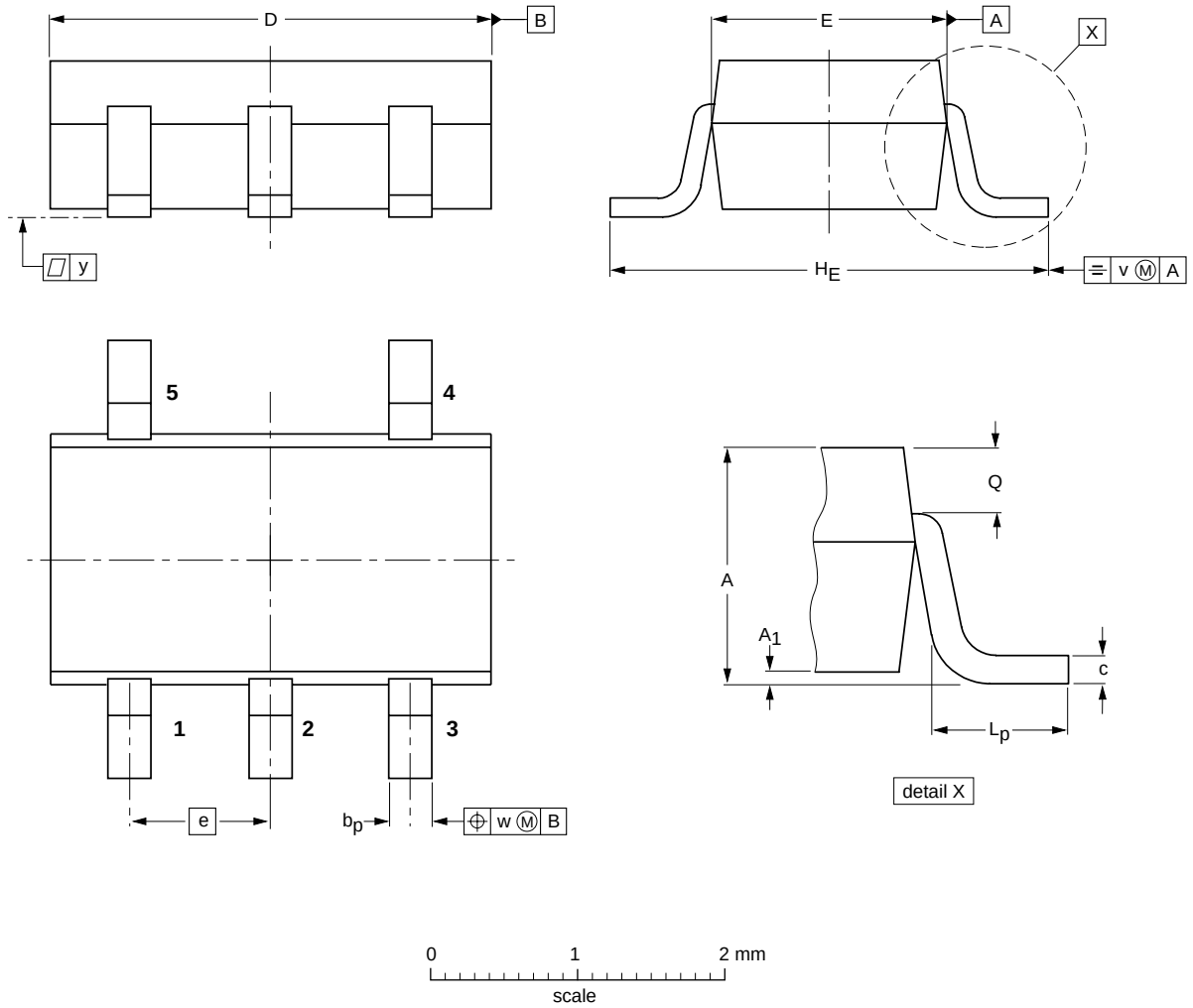


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Plastic surface mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.