FAIRCHILD SEMICONDUCTOR™

September 1991
Revised November 1999

74ACTQ18823
18-Bit D-Type Flip-Flop with 3-STATE Outputs

General Description

The ACTQ18823 contains eighteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP), Clear ($\overline{CLR}$), Clock Enable ($\overline{EN}$) and Output Enable ($\overline{OE}$) are common to each byte and can be shorted together for full 18-bit operation.

The ACTQ18823 utilizes Fairchild's Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector for superior performance.

Features

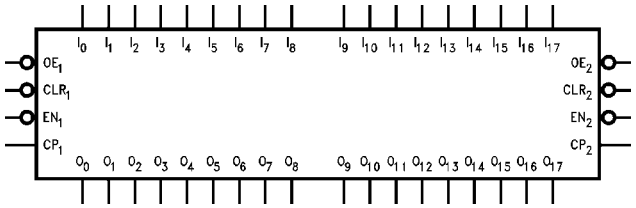
- Utilizes Fairchild's FACT Quiet Series technology
- Broadside pinout allows for easy board layout
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Separate control logic for each byte
- Extra data width for wider address/data paths or buses carrying parity
- Outputs source/sink 24 mA
- Additional specs for Multiple Output Switching
- Output loading specs for both 50 pF and 250 pF loads

Ordering Code:

Order Number	Package Number	Package Description
74ACTQ18823SSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACTQ18823MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$\overline{CLR}_n$	Clear (Active LOW)
$\overline{EN}_n$	Clock Enable (Active LOW)
CP_n	Clock Pulse Input
I_0–I_{17}	Inputs
O_0–O_{17}	Outputs

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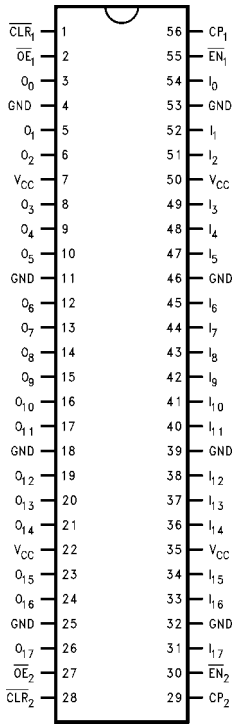
Connection Diagram



Functional Description

The ACTQ18823 consists of eighteen D-type edge-triggered flip-flops. These have 3-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. The buffered clock (CP_n) and buffered Output Enable ($\overline{OE}_n$) are common to all flip-flops within that byte. The flip-flops will store the state of their individual D inputs that meet set-up and hold time requirements on the LOW-to-HIGH CP_n transition. With $\overline{OE}_n$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the impedance state. Operation of the $\overline{OE}_n$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear ($\overline{CLR}_n$) and Clock Enable ($\overline{EN}_n$) pins. These devices are ideal for parity bus interfacing in high performance systems.

When $\overline{CLR}_n$ is LOW and $\overline{OE}_n$ is LOW, the outputs are LOW. When $\overline{CLR}_n$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}_n$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}_n$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table (Note 1)

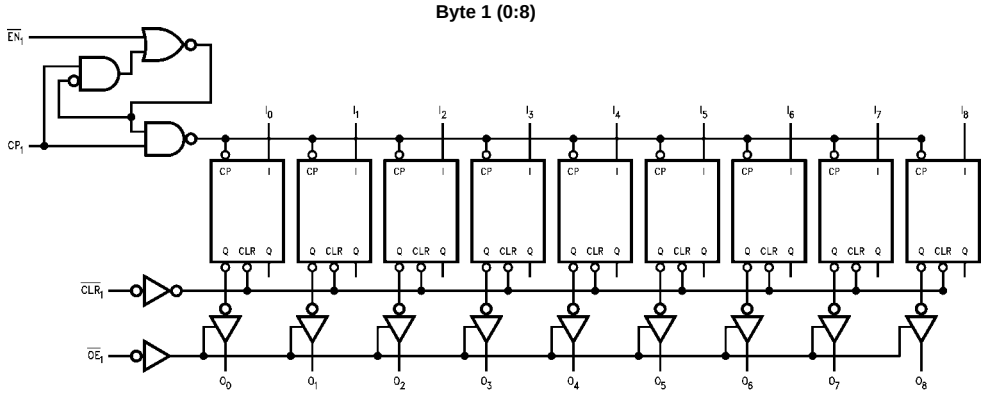
Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	I_n	Q	O_n	
H	X	L	⌐	L	L	Z	High Z
H	X	L	⌐	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	⌐	L	L	Z	Load
H	H	L	⌐	H	H	Z	Load
L	H	L	⌐	L	L	L	Load
L	H	L	⌐	H	H	H	Load

H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance
⌐= LOW-to-HIGH Transition
NC= No Change

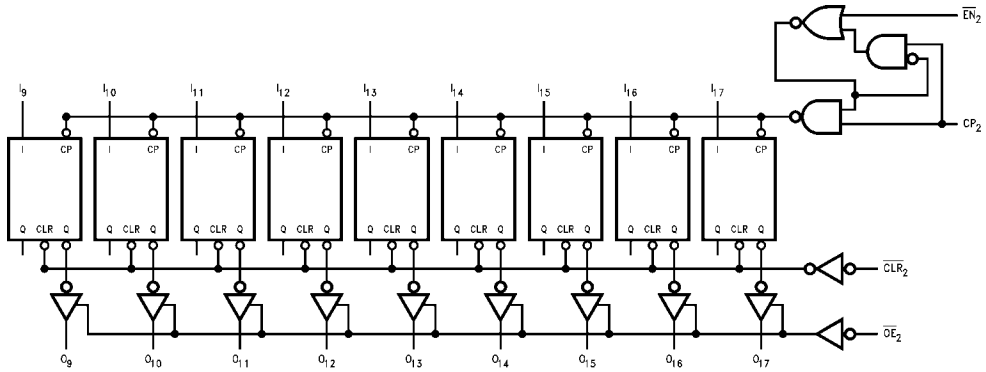
Note 1: The table represents the logic for one byte. The two bytes are independent of each other and function identically.

Logic Diagrams

Byte 1 (0:8)



Byte 2 (9:17)



Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
Per Output Pin	± 50 mA
Junction Temperature	
PDIP/SOIC	+140°C
Storage Temperature	−65°C to +150°C
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	T_A = +25°C	T_A = −40°C to +85°C		Units	Conditions
		(V)	Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 3)
V_{OL}	Maximum LOW Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 3)
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		±0.5	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} −2.1V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 4)				−75	mA	V_{OHD} = 3.85V Min
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.5	0.8		V	(Note 6)(Note 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.5	−0.8		V	(Note 6)(Note 7)
V_{OHP}	Maximum Overshoot	5.0	V_{OH} + 1.0	V_{OH} + 1.5		V	(Note 5)(Note 7)
V_{OHV}	Minimum V_{CC} Droop	5.0	V_{OH} − 1.0	V_{OH} − 1.8		V	(Note 5)(Note 7)
V_{IHD}	Minimum High Voltage Level	5.0	1.7	2.0		V	(Note 5)(Note 8)
V_{ILD}	Maximum Low Dynamic Input Voltage Level	5.0	1.2	1.2		V	(Note 5)(Note 8)

Note 3: All outputs loaded; thresholds associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: Worst case package.

Note 6: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched LOW and one output held LOW.

Note 7: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched HIGH and one output held HIGH.

Note 8: Maximum number of data inputs (n) switching. (n − 1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	5.0	100			90		MHz
t_{PHL}	Propagation Delay	5.0	2.0		9.0	2.0	9.5	ns
t_{PLH}	CP_n to O_n		2.0		9.0	2.0	9.5	
t_{PHL}	Propagation Delay $\overline{CLR}_n$ to O_n	5.0	2.0		9.0	2.0	9.5	ns
t_{PZL}	Output Enable Time	5.0	2.0		9.0	2.0	10.0	ns
t_{PZH}			2.0		9.0	2.0	10.0	
t_{PLZ}	Output Disable Time	5.0	1.5		7.0	1.5	7.5	ns
t_{PHZ}			1.5		8.0	1.5	8.5	

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 10)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW, Input to Clock	5.0		3.0	3.0	ns
t_H	Hold Time, HIGH or LOW, Input to Clock	5.0		1.5	1.5	ns
t_S	Setup Time, HIGH or LOW, Enable to Clock	5.0		3.0	3.0	ns
t_H	Hold Time, HIGH or LOW, Enable to Clock	5.0		1.5	1.5	ns
t_W	$\overline{CP}_n$ Pulse Width, HIGH or LOW	5.0		4.0	4.0	ns
t_W	$\overline{CLR}_n$ Pulse Width, HIGH or LOW	5.0		4.0	4.0	ns
t_{REC}	Recovery Time, $\overline{CLR}_n$ to CP_n	5.0		6.0	6.0	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V.

Extended AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, V_{CC} = Com, C_L = 50 pF, 16 Outputs Switching (Note 12)			$T_A = -40°C$ to $+85°C$, V_{CC} = Com, C_L = 250 pF (Note 13)		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	5.2	6.5	7.6	7.0	9.8	ns
t_{PHL}	CP_n to O_n	5.3	6.5	7.8	6.8	10.0	
t_{PHL}	Propagation Delay $\overline{CLR}_n$ to O_n	4.8	5.3	6.2	5.2	7.5	ns
t_{PZH}	Output Enable Time	4.2	4.8	6.5	(Note 14)		ns
t_{PZL}		4.4	5.3	6.0			
t_{PHZ}	Output Disable Time	3.5	4.2	4.8	(Note 15)		ns
t_{PZL}		4.6	5.2	6.0			
t_{OSHL} (Note 11)	Pin to Pin Skew CP_n to O_n			1.0			ns
t_{OSLH} (Note 11)	Pin to Pin Skew CP_n to O_n			1.0			ns
t_{OSHL} (Note 11)	Pin to Pin Skew $\overline{CLR}_n$ to Output			1.0			ns
t_{OST} (Note 11)	Pin to Pin Skew CP_n to Output			1.5			ns

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}).

Note 12: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (il.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 13: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 14: 3-STATE delays are load dominated and have been excluded from the datasheet.

Note 15: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	95	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

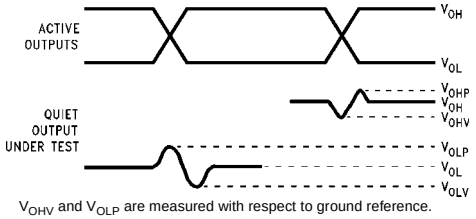
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.



V_{OHV} and V_{OLP} are measured with respect to ground reference.

Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

FIGURE 1. Quiet Output Noise Voltage Waveforms

5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillator steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

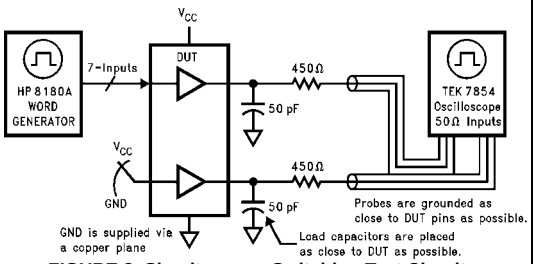
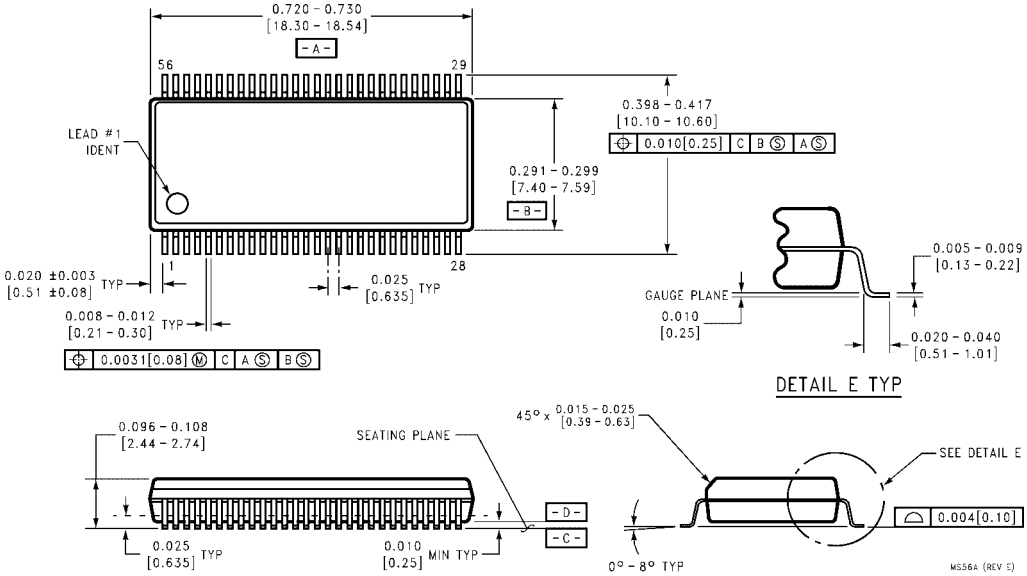


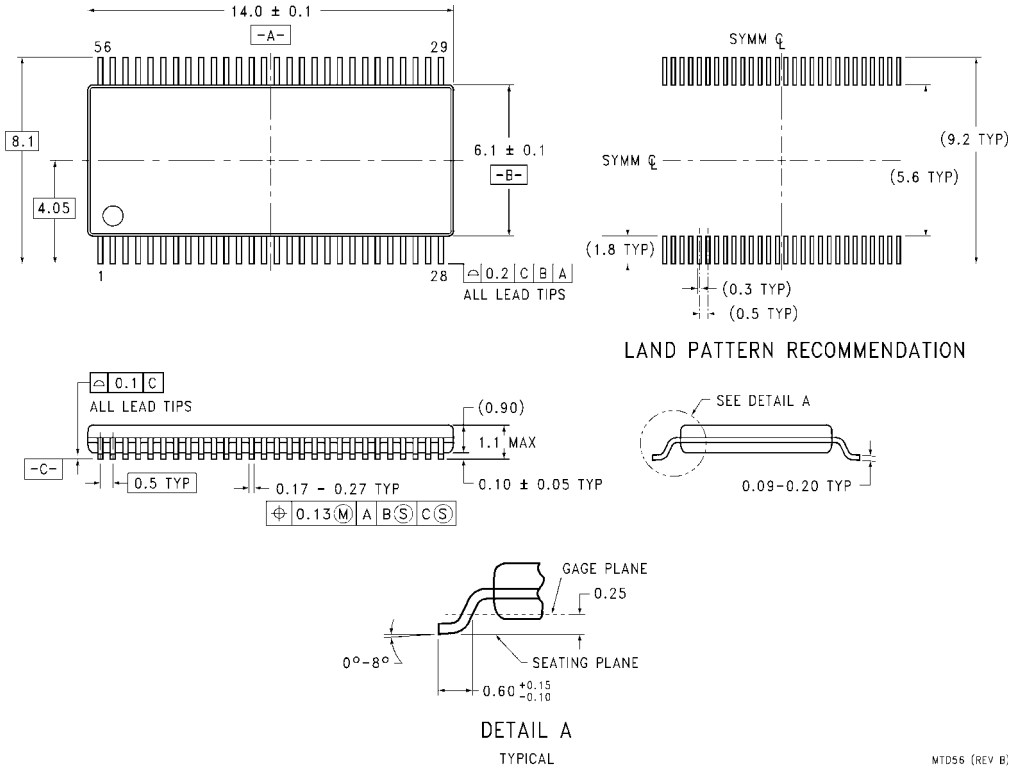
FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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