National Semiconductor

March 1993

54ACTQ/74ACTQ16646 16-Bit Transceiver/Register with TRI-STATE® Outputs

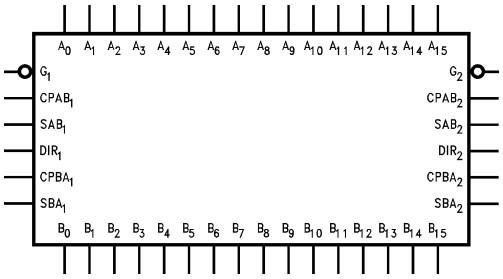
General Description

The 'ACTQ16646 contains sixteen non-inverting bidirectional registered bus transceivers providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition. The 'ACTQ16646 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector for superior performance.

Features

- Utilizes NSC FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- Separate control logic for each byte
- 16-bit version of the 'ACTQ646
- Outputs source/sink 24 mA
- Additional specs for Multiple Output Switching
- Output loading specs for both 50 pF and 250 pF loads

Logic Symbol



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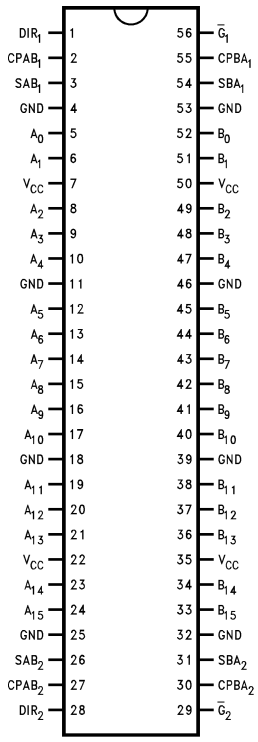
Connection Diagram

Pin Assignment for SSOP and CERPAK



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Real Time Transfer A-Bus to B-Bus

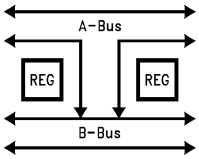

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FIGURE 1

Real Time Transfer B-Bus to A-Bus

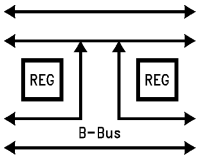

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FIGURE 2

Storage from Bus to Register

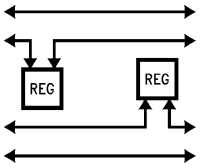

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FIGURE 3

Transfer from Register to Bus

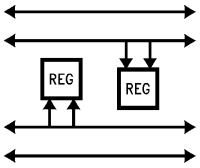

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FIGURE 4

Function Table

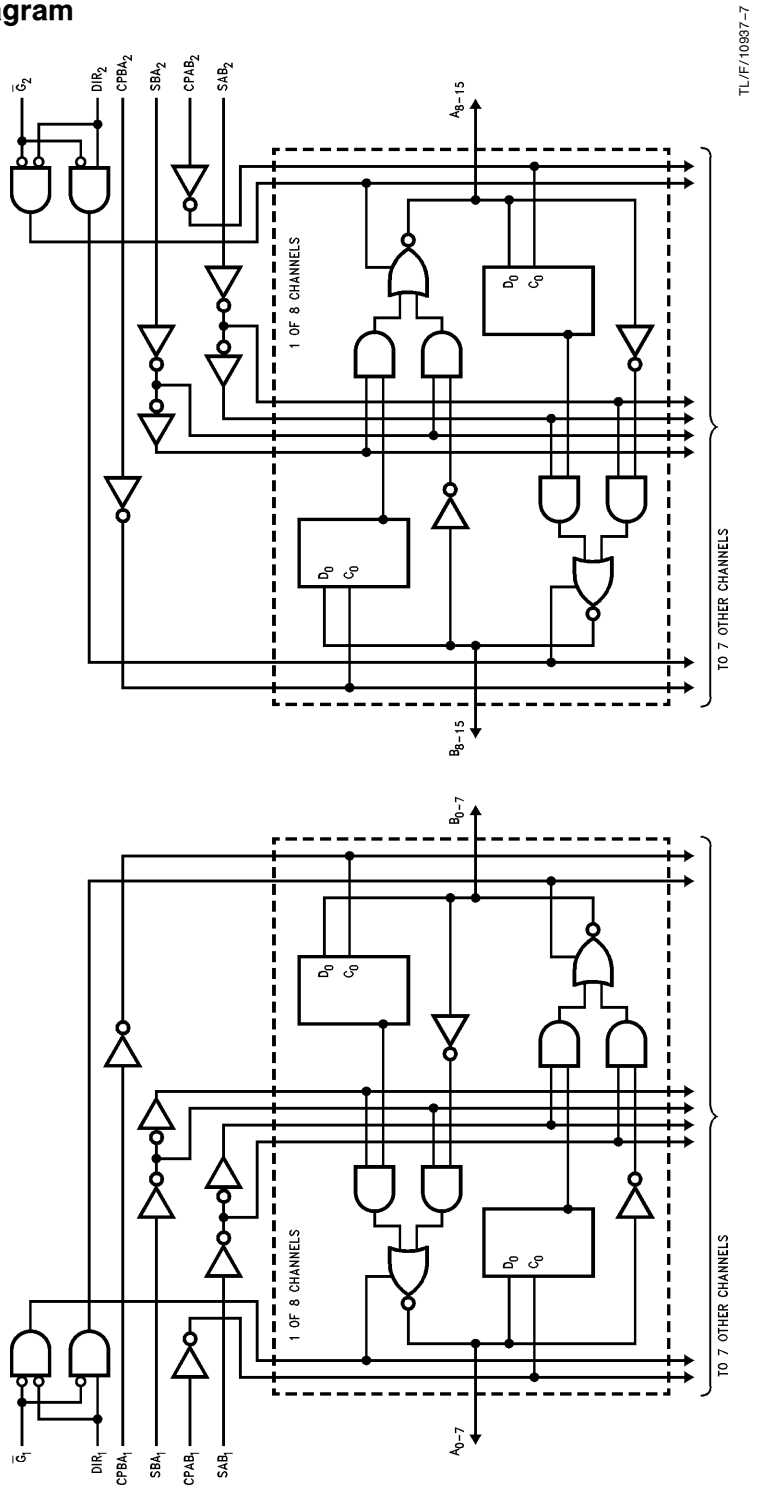
Inputs						Data I/O*		Output Operation Mode
G_1	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_{0-7}	B_{0-7}	
H	X	H or L	H or L	X	X			Isolation
H	X	⌐	X	X	X	Input	Input	Clock An Data into A Register
H	X	X	⌐	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X			An to Bn—Real Time (Transparent Mode)
L	H	⌐	X	L	X	Input	Output	Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	⌐	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L			Bn to An—Real Time (Transparent Mode)
L	L	X	⌐	X	L	Output	Input	Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	⌐	X	H			Clock Bn into B Register and Output to An

*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

H = HIGH Voltage Level X = Immaterial

L = LOW Voltage Level ⌐ = LOW-to-HIGH Transition.

Logic Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	±50 mA
Junction Temperature	
CDIP	+175°C
PDIP/SOIC	+140°C
Storage Temperature	−65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Note 2: For qualification information, please refer to the NSC SSOP Qualification Handbook.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACTQ	−40°C to +85°C
54ACTQ	−55°C to +125°C
Minimum Input Edge Rate (dV/dt)	
'ACTQ Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ T_A = +25°C	54ACTQ T_A = −55°C to +125°C	74ACTQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum Low Input Voltage	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum High Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN}* = V_{IL} or V_{IH}
		4.5		3.86	3.70	V	I_{OH} −24 mA
		5.5		4.86	4.70		I_{OH} −24 mA
V_{OL}	Maximum Low Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN}* = V_{IL} or V_{IH}
		4.5		0.36	0.50	V	I_{OL} 24 mA
		5.5		0.36	0.50		I_{OL} 24 mA
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_{IN} = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{CC}	Max Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND (Note 5)

*All outputs loaded; thresholds associated with output under test.

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}					50	−75	mA	V_{OHD} = 3.85V Min
V_{OLP}	Quick Output Maximum Dynamic V_{OL}	5.0	0.5	0.8			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quick Output Minimum Dynamic V_{OL}	5.0	−0.5	−0.8			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OHP}	Maximum Overshoot	5.0	V_{OH} + 1.0	V_{OH} + 1.5			V	*Figures 2-12, 13* (Notes 1, 3)
V_{OHV}	Minimum V_{CC} Droop	5.0	V_{OH} − 1.0	V_{OH} − 1.8			V	*Figures 2-12, 13* (Notes 1, 3)
V_{IHD}	Minimum High Dynamic Input Voltage Level	5.0	1.7	2.0			V	(Notes 1, 4)
V_{ILD}	Maximum Low Dynamic Input Voltage Level	5.0	1.2	0.8			V	(Notes 1, 4)

†Maximum test duration 2.0 ms; one output loaded at a time.

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n − 1) inputs switching 0V to 3V ('ACTQ). Input under test switching 3V to threshold (V_{ILD}).

Note 5: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	5.0	4.6	6.9	9.4			3.6	10.1	ns
t_{PLH}	Clock to Bus		4.3	6.5	8.9			3.3	9.7	
t_{PHL}	Propagation Delay	5.0	4.0	6.2	8.5			2.9	9.2	ns
t_{PLH}	Bus to Bus		4.1	6.4	8.6			3.2	9.3	
t_{PHL}	Propagation Delay	5.0	4.0	6.4	8.9			3.1	9.6	ns
t_{PLH}	Select to Bus (w/An or Bn HIGH or LOW)		4.2	6.7	9.5			3.2	10.4	
t_{PZL}	Enable Time	5.0	5.3	7.8	10.5			3.8	11.4	ns
t_{PZH}	G to An/Bn		4.6	6.9	9.4			3.3	10.2	
t_{PLZ}	Disable Time	5.0	3.0	5.5	8.1			2.3	8.6	ns
t_{PHZ}	G to An/Bn		3.4	5.7	8.3			2.6	8.6	
t_{PZL}	Enable Time	5.0	5.1	8.2	11.8			4.3	12.7	ns
t_{PZH}	DIR to An/Bn		4.6	7.5	10.8			3.7	11.7	
t_{PLZ}	Disable Time	5.0	2.9	5.8	9.2			2.0	9.8	ns
t_{PHZ}	DIR to An/Bn		3.4	6.1	9.2			2.5	9.7	

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF	54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units
			Guaranteed Minimum			
t_S	Setup Time, H or L Bus to Clock	5.0	3.0		3.0	ns
t_H	Hold Time, H or L Bus to Clock	5.0	1.5		1.5	ns
t_W	Clock Pulse Width H or L	5.0	4.0		4.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V.

Extended AC Electrical Characteristics

Symbol	Parameter	74ACTQ $T_A = -40°C$ to $+85°C$ V_{CC} = Com $C_L = 50$ pF 16 Outputs Switching (Note 2)			54ACTQ T_A = Mil V_{CC} = Mil $C_L = 50$ pF 16 Outputs Switching (Note 2)		74ACTQ $T_A = -40°C$ to $+85°C$ V_{CC} = Com $C_L = 250$ pF (Note 3)		54ACTQ T_A = Mil V_{CC} = Mil $C_L = 250$ pF (Note 3)		Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	4.1 4.2		10.1 10.1			6.1 6.0	14.5 14.8			ns
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	4.0 4.7		10.0 10.7			5.4 5.9	13.7 13.5			ns
t_{PHL} t_{PLH}	Propagation Delay Select to Bus (w/An or Bn HIGH or LOW)	3.8 4.3		9.6 10.9			5.7 6.1	14.2 15.5			ns
t_{PZL} t_{PZH}	Enable Time G to An/Bn	5.0 4.1		12.7 11.3			(Note 4)				ns
t_{PLZ} t_{PHZ}	Disable Time G to An/Bn	3.2 3.5		8.3 8.6			(Note 5)				ns
t_{PZL} t_{PZH}	Enable Time DIR to An/Bn	4.1 4.4		11.3 13.0			(Note 4)				ns
t_{PLZ} t_{PHZ}	Disable Time DIR to An/Bn	2.9 3.4		9.5 9.7			(Note 5)				ns
t_{OSHL} (Note 1)	Pin-to-Pin Skew Clock to Bus			1.0							ns
t_{OSLH} (Note 1)	Pin-to-Pin Skew Clock to Bus			1.0							ns
t_{OSHL} (Note 1)	Pin-to-Pin Skew Bus to Bus			1.0							ns
t_{OSLH} (Note 1)	Pin-to-Pin Skew Bus to Bus			1.0							ns

Extended AC Electrical Characteristics (Continued)

Symbol	Parameter	74ACTQ			54ACTQ		74ACTQ		54ACTQ		Units
		$T_A = -40°C$ to $+85°C$ V_{CC} = Com C_L = 50 pF 16 Outputs Switching (Note 2)			T_A = Mil V_{CC} = Mil C_L = 50 pF 16 Outputs Switching (Note 2)		$T_A = -40°C$ to $+85°C$ V_{CC} = Com C_L = 250 pF (Note 3)		T_A = Mil V_{CC} = Mil C_L = 250 pF (Note 3)		
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{OSHL} (Note 1)	Pin-to-Pin Skew Select to Bus (w/An or Bn HIGH or LOW)			1.0							ns
t_{OSLH} (Note 1)	Pin-to-Pin Skew Select to Bus (w/An or Bn HIGH or LOW)			1.2							ns
t_{OST} (Note 1)	Pin-to-Pin Skew Clock to Bus			2.1							ns
t_{OST} (Note 1)	Pin-to-Pin Skew Bus to Bus			1.0							ns
t_{OST} (Note 1)	Pin-to-Pin Skew Select to Bus			2.7							ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 3: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 4: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 5: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	95	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.

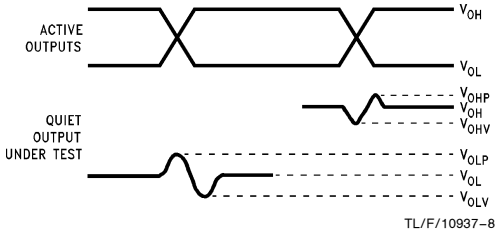


FIGURE 1. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

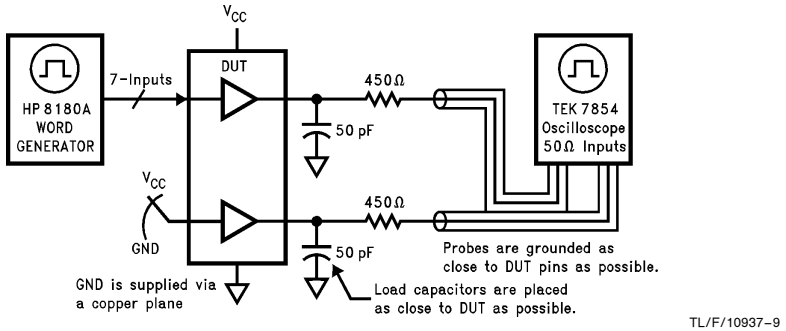


FIGURE 2. Simultaneous Switching Test Circuit

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74ACTQ 16646 SS C X

Temperature Range Family
74ACTQ = Commercial—TTL Compatible
54ACTQ = Military—TTL Compatible

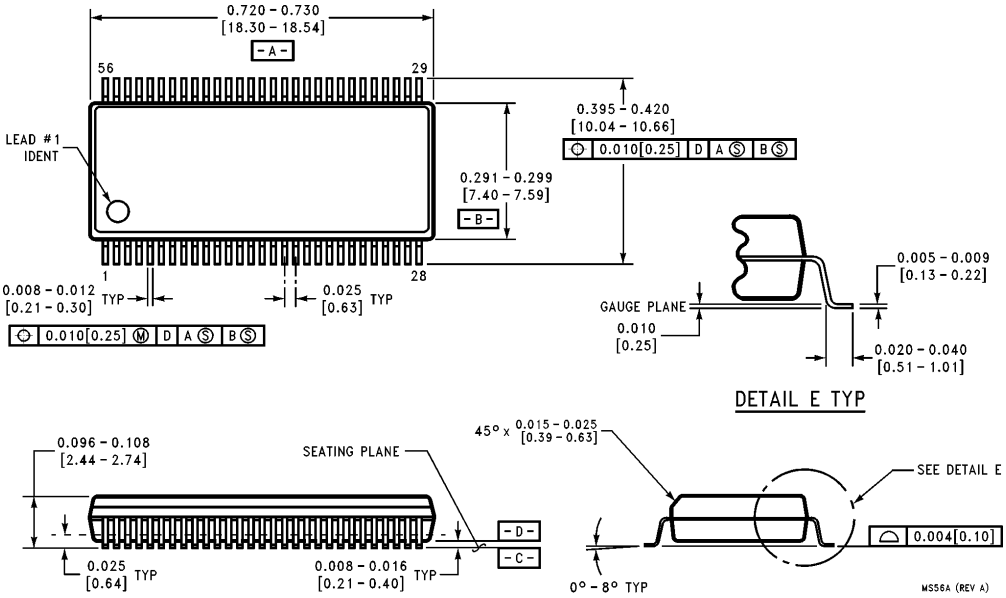
Device Type

Package Code
SS = Small Outline (SSOP)
F = CERPAK

Temperature Range
C = Commercial Product (−45°C to +85°C)
M = Military (−55°C to +125°C)

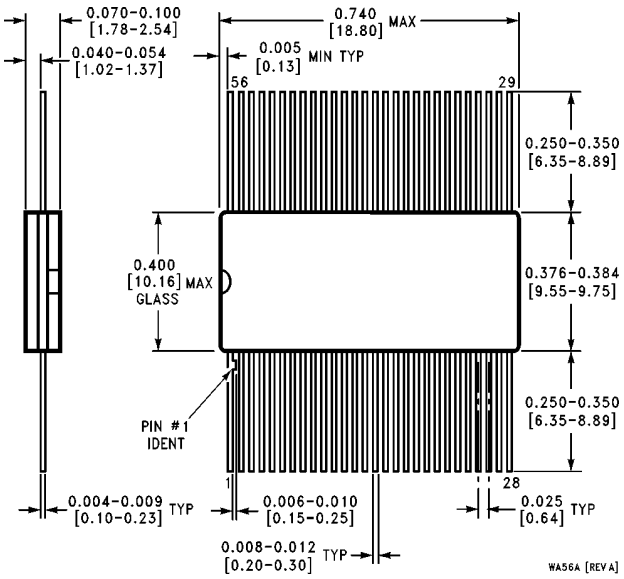
Special Variations
X = Devices shipped in 13″ reels
QB = 883 Processing

Physical Dimensions inches (millimeters)



56-Lead SSOP (0.300″ Wide) (SS)
NS Package Number MS56A

Physical Dimensions inches (millimeters) (Continued)



56-Lead CERPAK (F)
NS Package Number WA56A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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