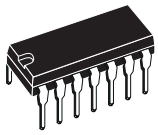
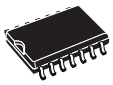
74ACT74

DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED:
  f_{MAX} = 250MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION:
  I_{CC} = 4µA(MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.), V_{IL} = 0.8V (MAX.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 74
- IMPROVED LATCH-UP IMMUNITY



DIP



SOP

TSSOP

ORDER CODES

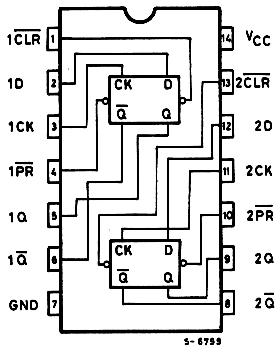
PACKAGE	TUBE	T & R
DIP	74ACT74B	
SOP	74ACT74M	74ACT74MTR
TSSOP		74ACT74TTR

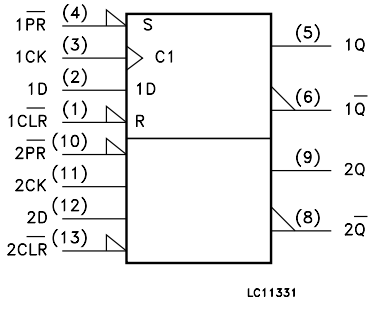
DESCRIPTION

The 74ACT74 is an advanced high-speed CMOS DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS tecnology.
A signal on the D INPUT is transferred to the Q and $\overline{Q}$ OUTPUTS during the positive going transition of the clock pulse.

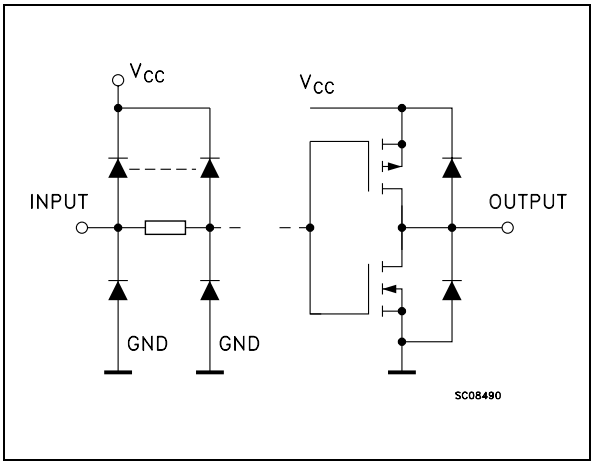
CLEAR and PRESET are independent of the clock and accomplished by a low setting on the appropriate input.
The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

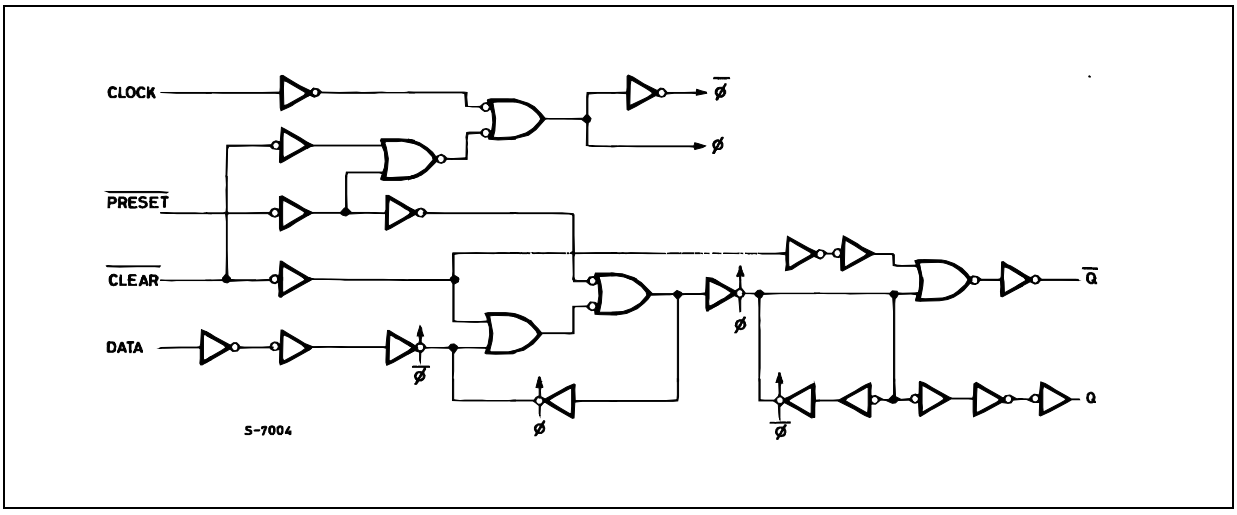
PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CLR}$, $2\overline{CLR}$	Asyncronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW to HIGH, Edge Triggered)
4, 10	$1\overline{PR}$, $2\overline{PR}$	Asyncronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	L	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L	⌐	L	H	
H	H	H	⌐	H	L	
H	H	X	¬	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 200	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time V_{CC} = 4.5 to 5.5V (note 1)	8	ns/V

1) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5	V_O = 0.1 V or V_{CC}-0.1V	2.0	1.5		2.0		2.0		V
		5.5		2.0	1.5		2.0		2.0		
V_{IL}	Low Level Input Voltage	4.5	V_O = 0.1 V or V_{CC}-0.1V		1.5	0.8		0.8		0.8	V
		5.5			1.5	0.8		0.8		0.8	
V_{OH}	High Level Output Voltage	4.5	I_O=-50 µA	4.4	4.49		4.4		4.4		V
		5.5	I_O=-50 µA	5.4	5.49		5.4		5.4		
		4.5	I_O=-24 mA	3.86			3.76		3.7		V
		5.5	I_O=-24 mA	4.86			4.76		4.7		
V_{OL}	Low Level Output Voltage	4.5	I_O=50 µA		0.001	0.1		0.1		0.1	V
		5.5	I_O=50 µA		0.001	0.1		0.1		0.1	
		4.5	I_O=24 mA			0.36		0.44		0.5	
		5.5	I_O=24 mA			0.36		0.44		0.5	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CCT}	Max I_{CC}/Input	5.5	V_I = V_{CC} - 2.1V		0.6			1.5		1.6	mA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			4		40		40	µA
I_{OLD}	Dynamic Output Current (note 1, 2)	5.5	V_{OLD} = 1.65 V max					75		50	mA
I_{OHD}			V_{OHD} = 3.85 V min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q or Q	5.0(*)			5.0	10.0		11.0		11.0	ns
t_{PLH} t_{PHL}	Propagation Delay Time PR or CLR to Q or Q	5.0(*)			5.0	10.0		11.0		11.0	ns
t_W	Pulse Width HIGH or LOW, CK or PR or CLR	5.0(*)			1.5	5.0		6.0		6.0	ns
t_s	Setup Time D to CK HIGH or LOW	5.0(*)			0.5	3.0		3.5		3.5	ns
t_h	Hold Time D to CK HIGH or LOW	5.0(*)			-0.5	1.0		1.0		1.0	ns
t_{REM}	Removal Tim| PR or CLR to CK	5.0(*)			-0.7	1.0		1.0		1.0	ns
f_{MAX}	Maximum Clock Frequency	5.0(*)		100	250		85		85		MHz

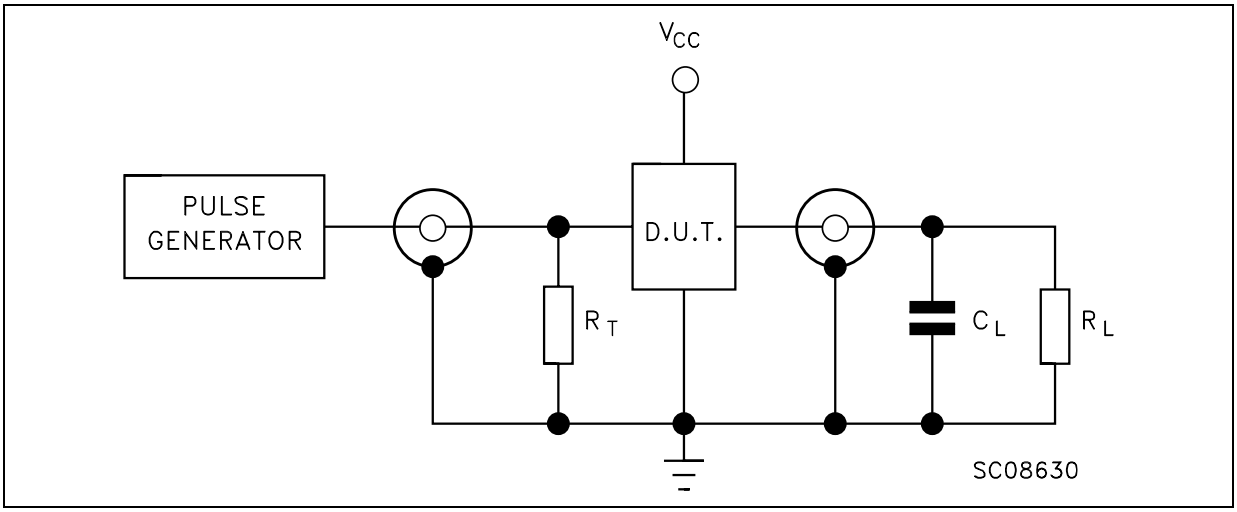
(*) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			3						pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0	f_{IN} = 10MHz		43						pF

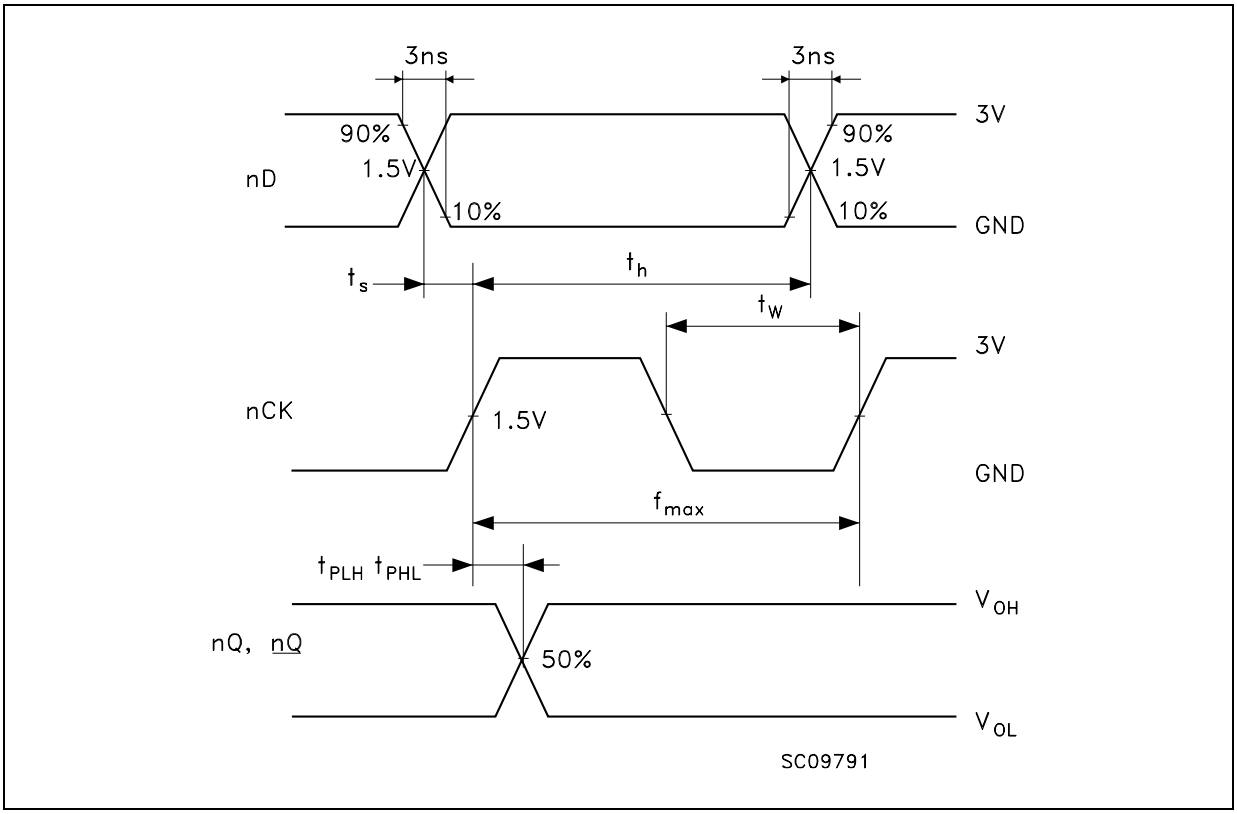
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per Flip-Flop)

TEST CIRCUIT

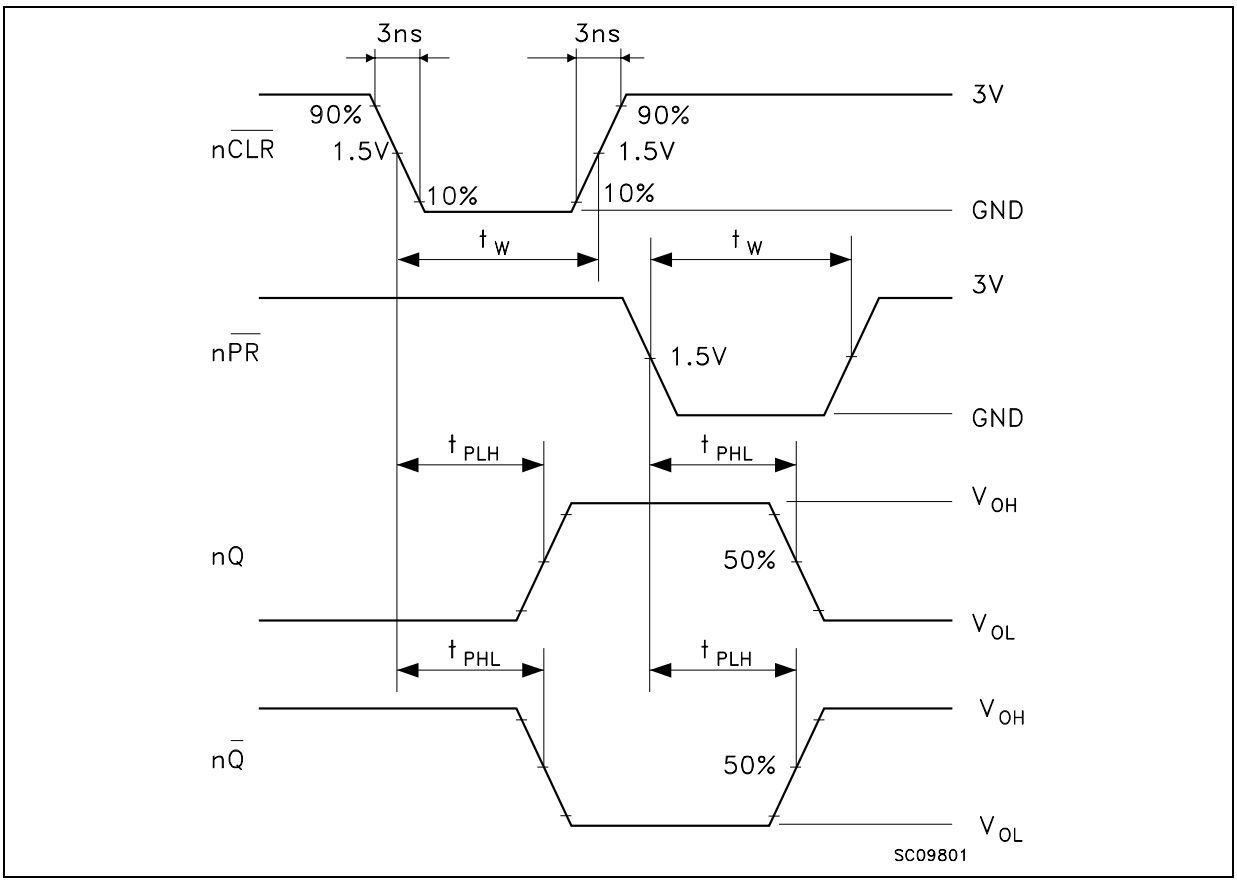


C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

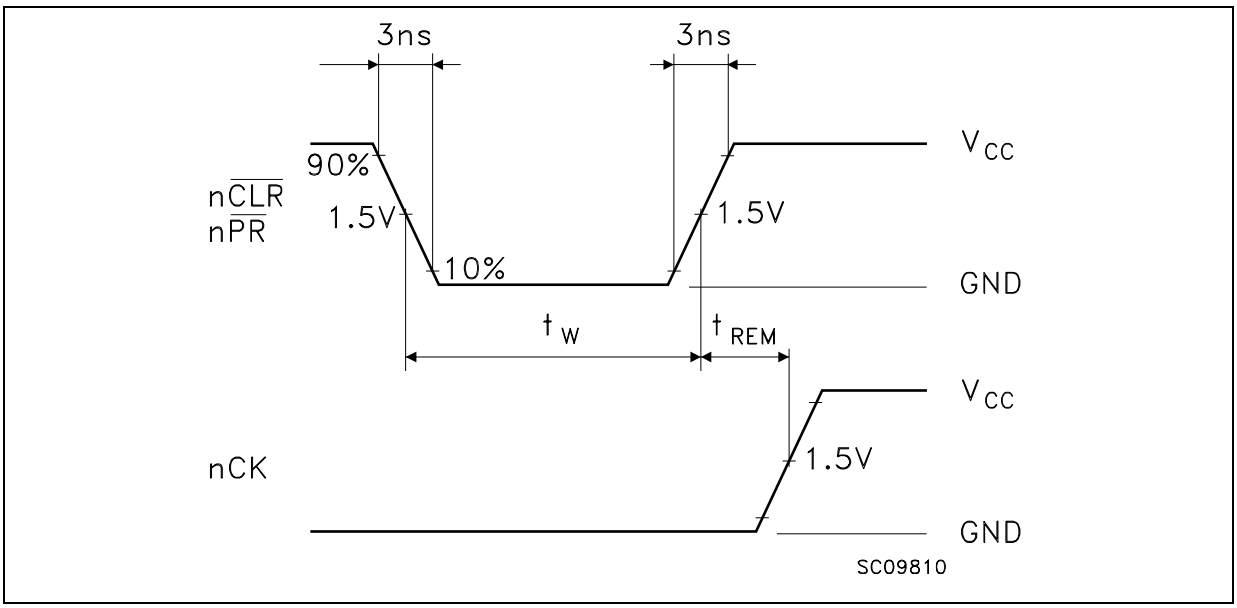
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



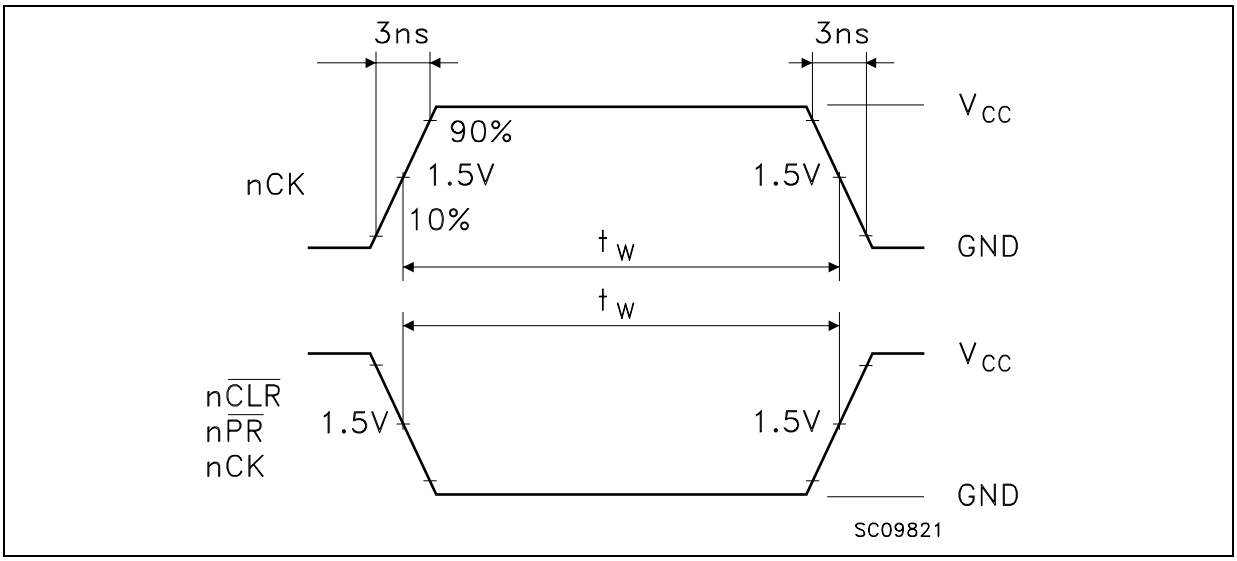
WAVEFORM 2: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



WAVEFORM 3: RECOVERY TIMES (f=1MHz; 50% duty cycle)

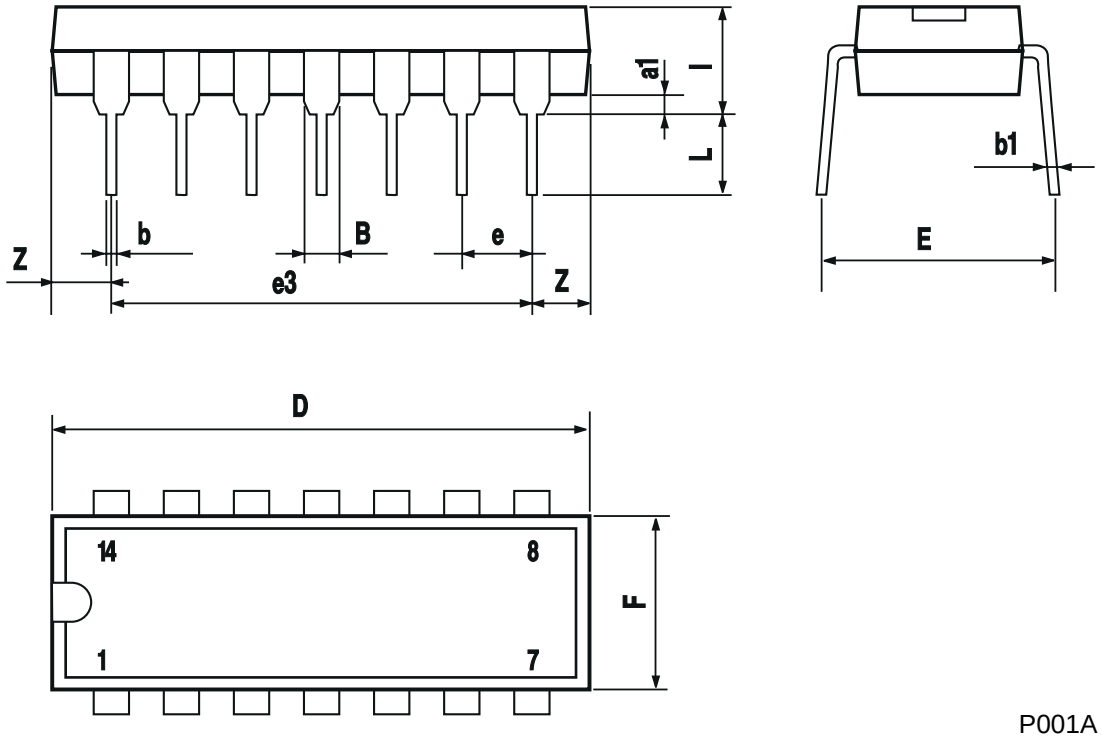


WAVEFORM 4: PULSE WIDTH



Plastic DIP-14 MECHANICAL DATA

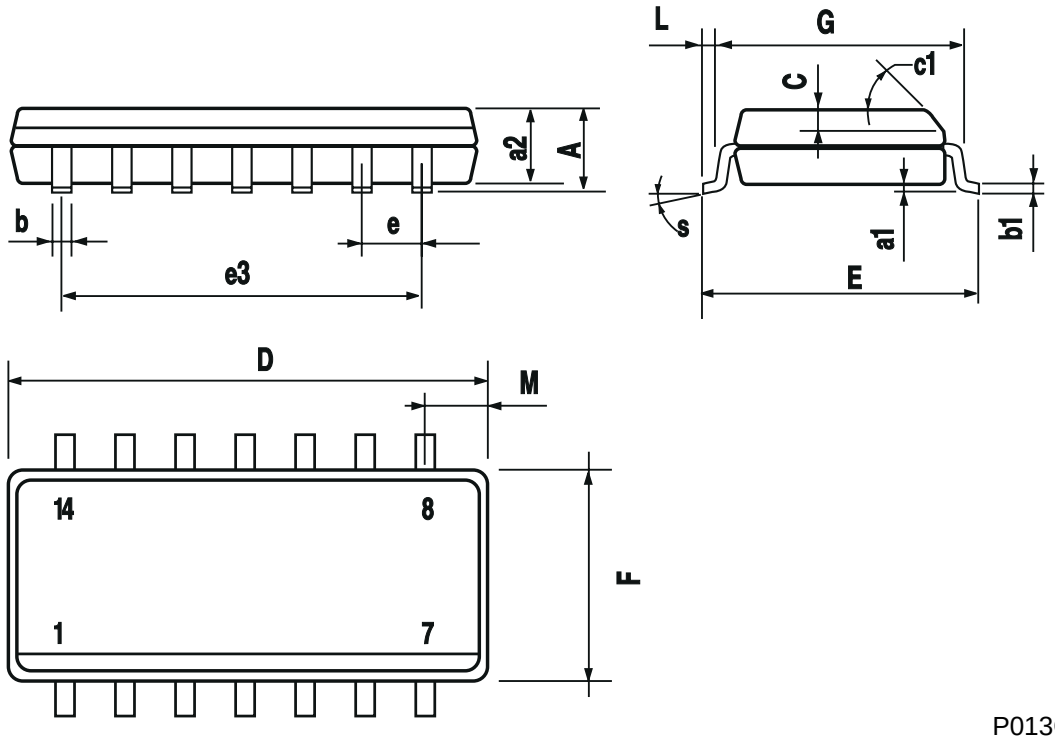
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

SO-14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



P013G

TSSOP14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0^o	4^o	8^o	0^o	4^o	8^o
L	0.50	0.60	0.70	0.020	0.024	0.028