DATA SHEET

74ABT16825A
74ABTH16825A

18-bit buffer/line driver; non-inverting (3-State)

Product specification
Supersedes data of 1995 Jul 14
IC23 Data Handbook

1998 Feb 25

Philips
Semiconductors

PHILIPS

18-bit buffer/line driver; non-inverting (3-State)

74ABT16825A
74ABTH16825A

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- 74ABTH16825A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The74ABT16825A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The74ABT16825A 18-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($n\overline{OE}1$, $n\overline{OE}2$) for maximum control flexibility.

Two options are available, 74ABT16825A which does not have the bus-hold feature and 74ABTH16825A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 5V	1.8 1.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	500	µA
I_{CCL}		Outputs Low; V_{CC} = 5.5V	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-pin SSOP Type III	–40°C to +85°C	74ABT16825A DL	BT16825A DL	SOT371-1
56-pin TSSOP Type II	–40°C to +85°C	74ABT16825A DGG	BT16825A DGG	SOT364-1
56-pin SSOP Type III	–40°C to +85°C	74ABTH16825A DL	BH16825A DL	SOT371-1
56-pin TSSOP Type II	–40°C to +85°C	74ABTH16825A DGG	BH16825A DGG	SOT364-1

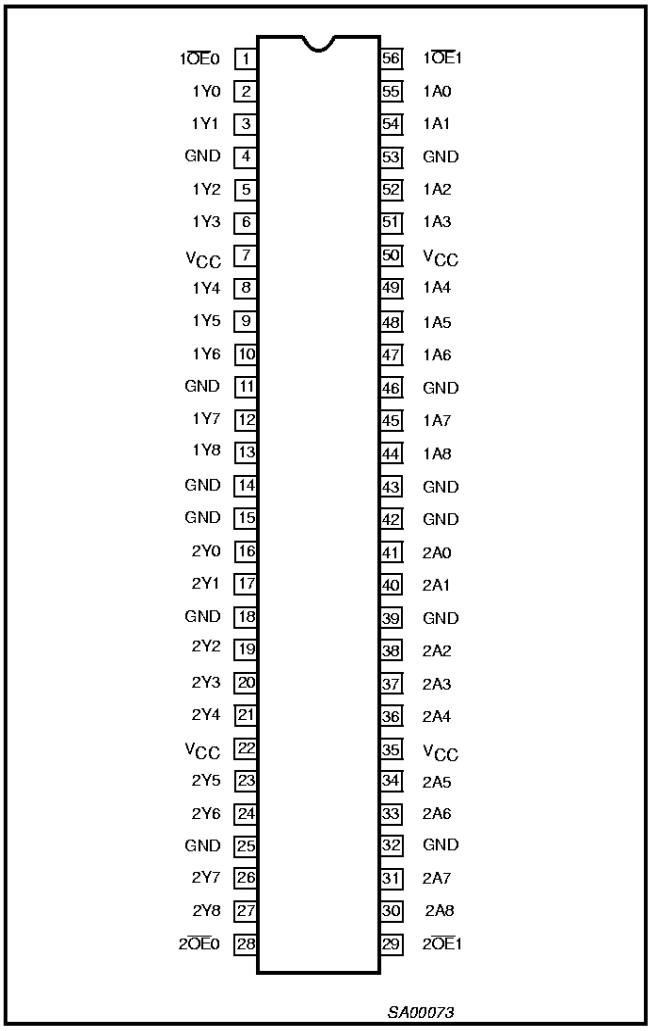
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 – 1A9 2A0 – 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 – 1Y9 2Y0 – 2Y9	Data outputs
1, 56 28, 29	$1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$	Output enable inputs (active-Low)
4, 11, 14, 15, 18, 25, 32, 39, 42, 43, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

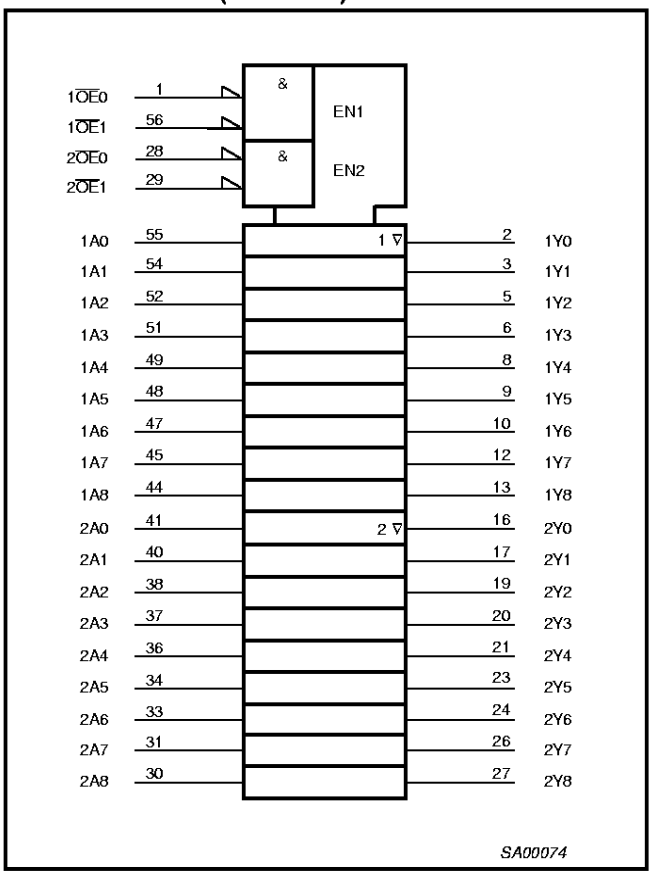
18-bit buffer/line driver; non-inverting (3-State)

74ABT16825A
74ABTH16825A

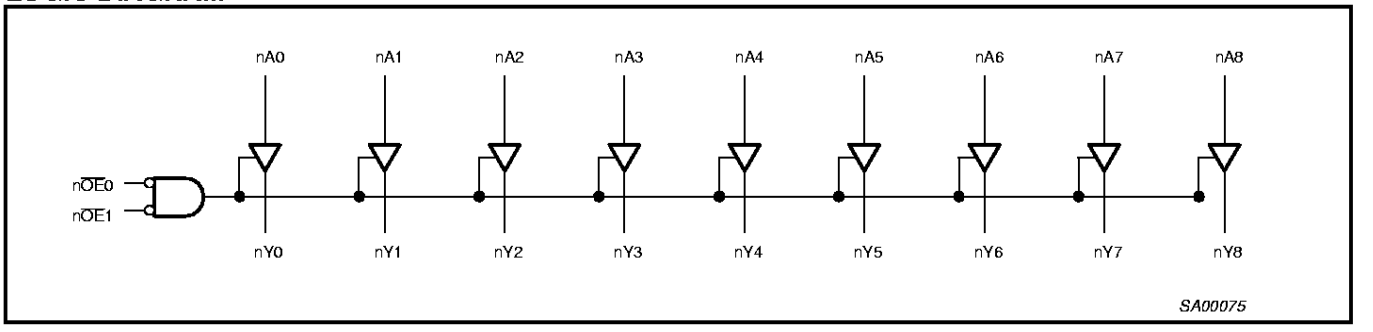
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM

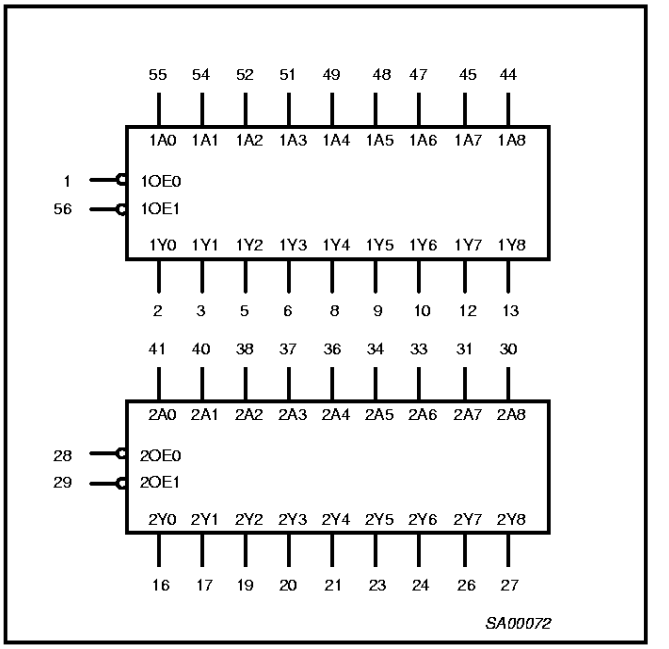


FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
$n\overline{OE}x$	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA			–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current ABT16825A	V_{CC} = 5.5V; V_I = GND or 5.5V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH16825A	V_{CC} = 5.5V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5V; V_I = V_{CC}	Data pins[4]		0.01	1		1	µA
		V_{CC} = 5.5V; V_I = 0	Data pins[4]		–1	–3		–5	µA
I_{HOLD}	Bus Hold current A inputs[5] 74ABTH16825A	V_{CC} = 4.5V; V_I = 0.8V		35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V		–75			–75		µA
		V_{CC} = 5.5V; V_I = 0 to 5.5V		±500					µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O = 4.5V; V_I = 0V or 5.5V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = Don't care			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}			–1.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V		–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}			0.5	1		1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}			9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1		1	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16825A	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			10	500		500	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16825A	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND			0.2	1		1	mA

NOTES:

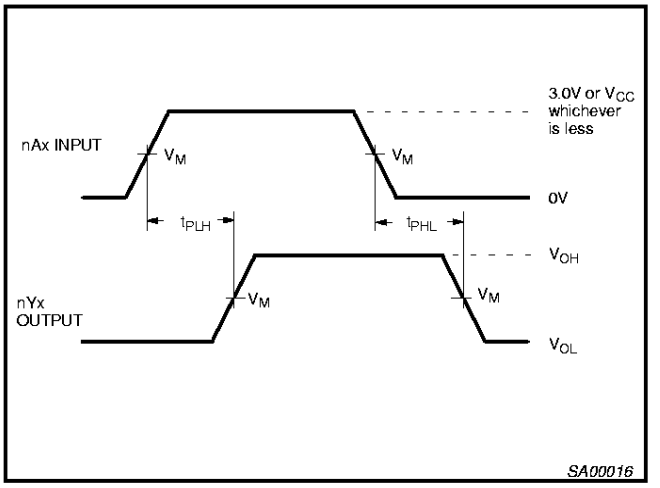
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
4. Unused pins at V_{CC} or GND.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

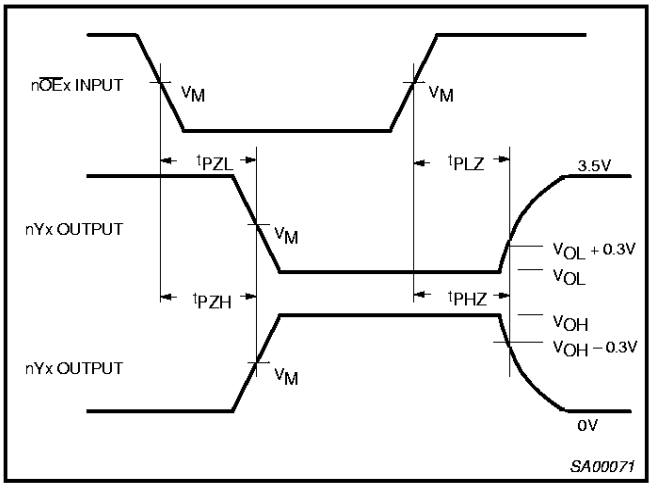
GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 0.6	1.8 1.4	2.5 2.0	1.0 0.6	2.8 2.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	2.9 2.9	3.8 3.8	1.0 1.0	4.8 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.0 1.6	3.3 2.5	4.5 3.4	2.0 1.6	5.2 3.7	ns

AC WAVEFORMS

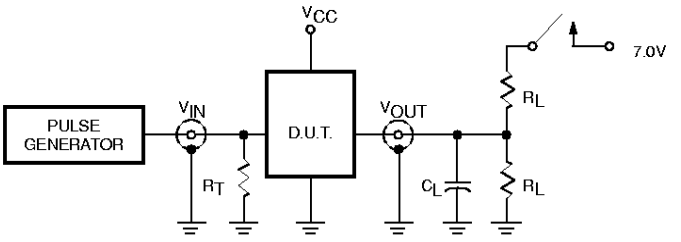


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

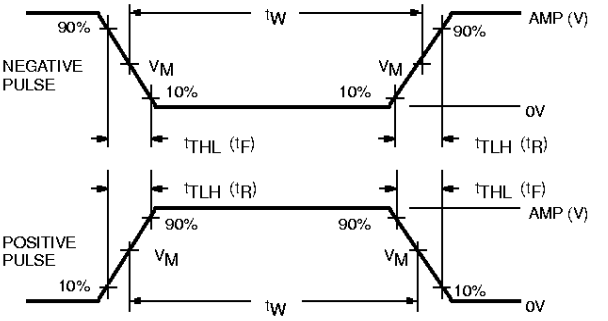


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

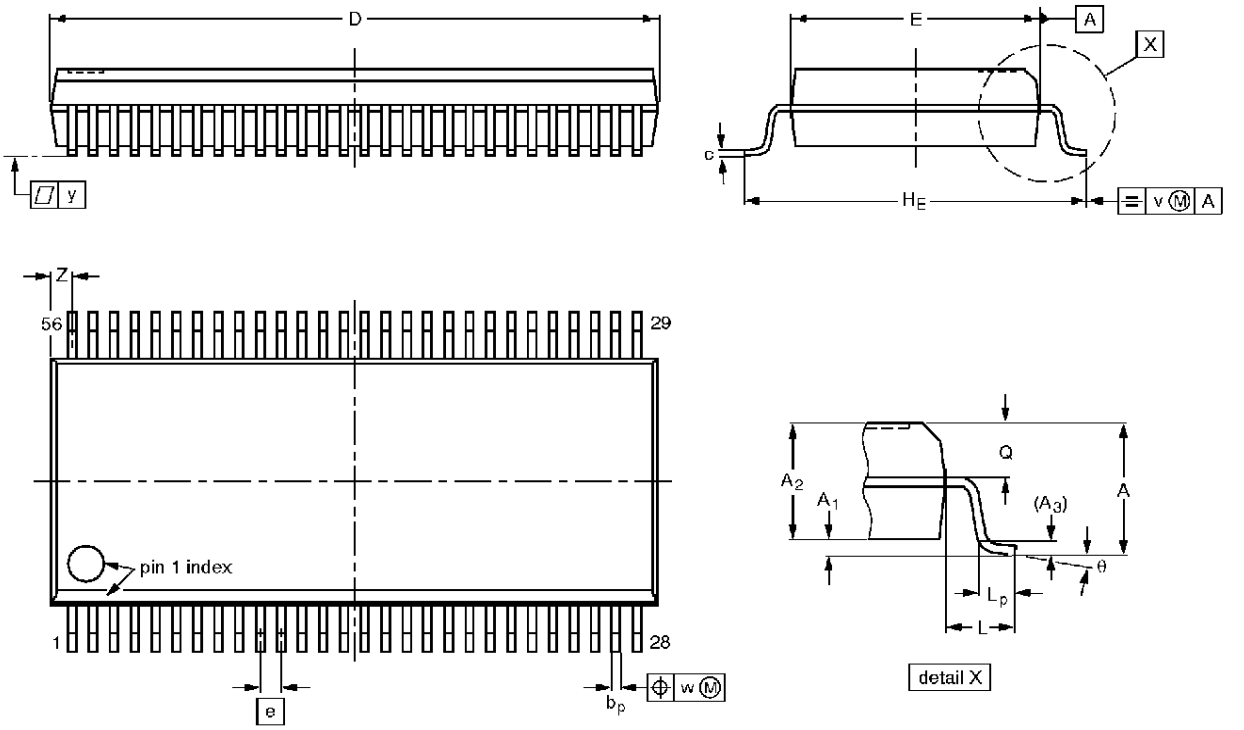
DEFINITIONS

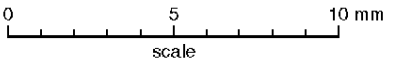
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**





DIMENSIONS (mm are the original dimensions)

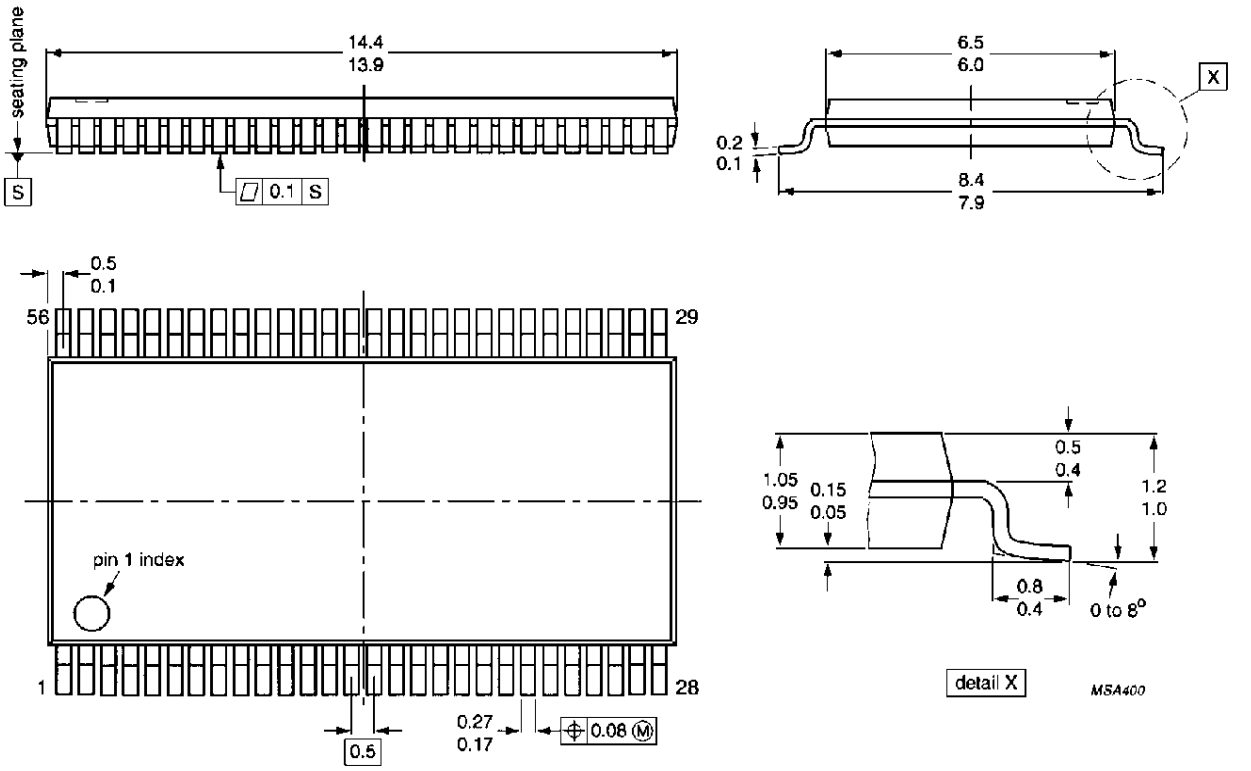
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



Dimensions in mm.

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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