

DATA SHEET

www.DataSheet4U.net

74ABT16821A

74ABTH16821A

20-bit bus-interface D-type flip-flop;
positive-edge trigger (3-State)

Product specification
Supersedes data of 1995 Sep 28
IC23 Data Handbook

1998 Feb 27

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

FEATURES

- 20-bit positive-edge triggered register
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- 74ABTH16821A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16821A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16821A has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable (nOE) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable (nOE) controls all ten 3-State buffers independent of the register operation. When nOE is Low, the data in the register appears at the outputs. When nOE is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

Two options are available, 74ABT16821A which does not have the bus-hold feature and 74ABTH16821A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	$C_L = 50\text{pF}$; $V_{CC} = 5\text{V}$	2.4 2.0	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	3	pF
C_{OUT}	Output capacitance	$V_O = 0\text{V}$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	μA
I_{CCL}		Outputs LOW; $V_{CC} = 5.5\text{V}$	10	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ABT16821A DL	BT16821A DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ABT16821A DGG	BT16821A DGG	SOT364-1
56-Pin Plastic SSOP Type III	-40°C to $+85^{\circ}\text{C}$	74ABTH16821A DL	BH16821A DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to $+85^{\circ}\text{C}$	74ABTH16821A DGG	BH16821A DGG	SOT364-1

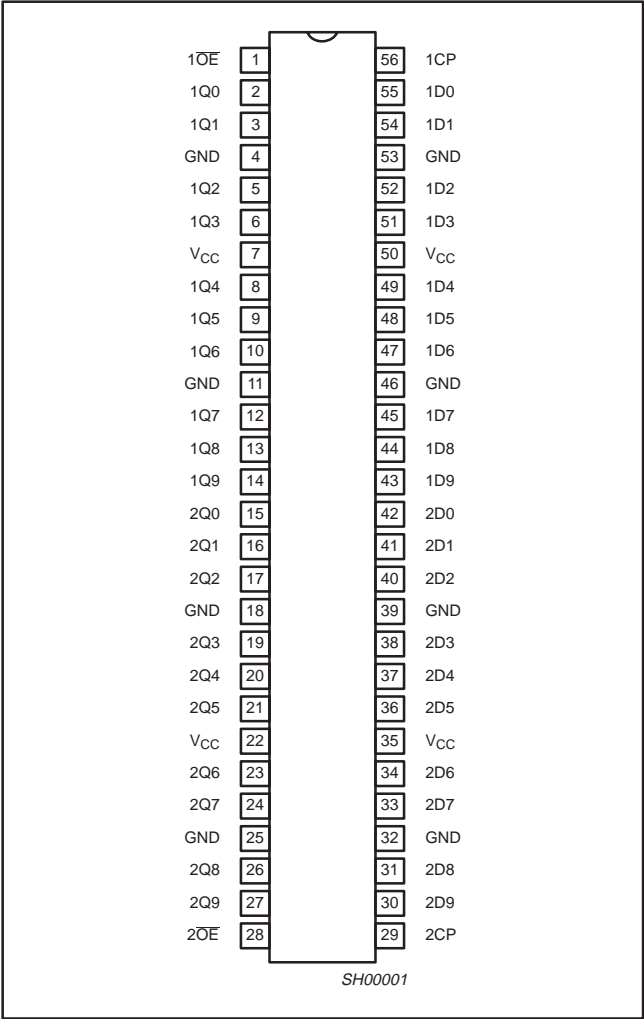
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1D0 - 1D9 2D0 - 2D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Q0 - 1Q9 2Q0 - 2Q9	Data outputs
1, 28	1OE, 2OE	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

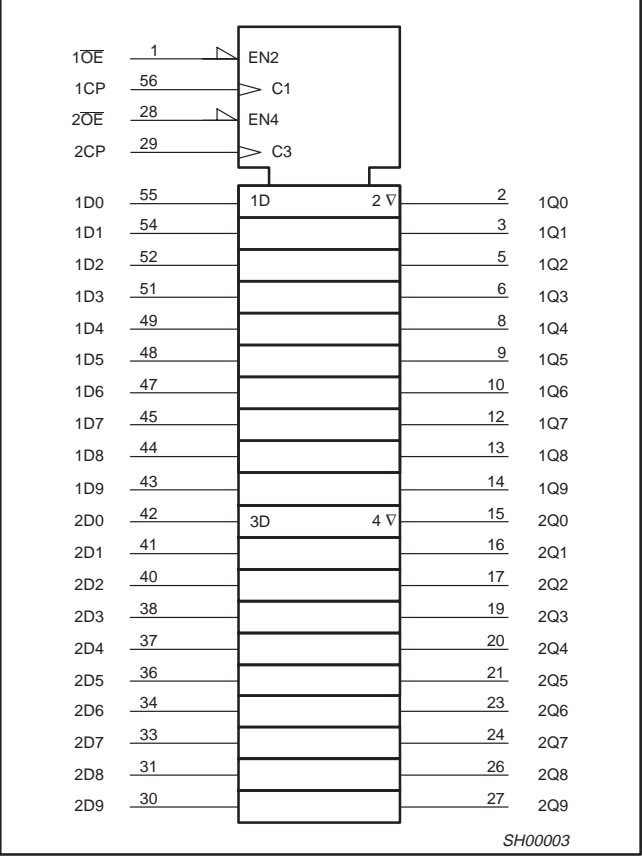
20-bit bus-interface D-type flip-flop;
positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

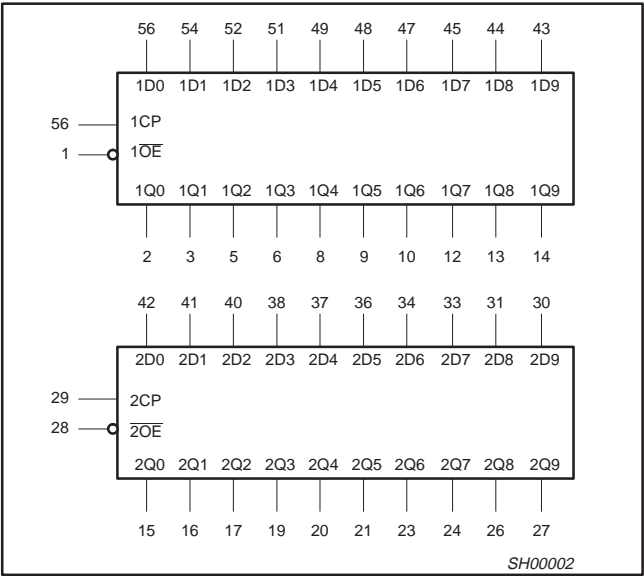
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL

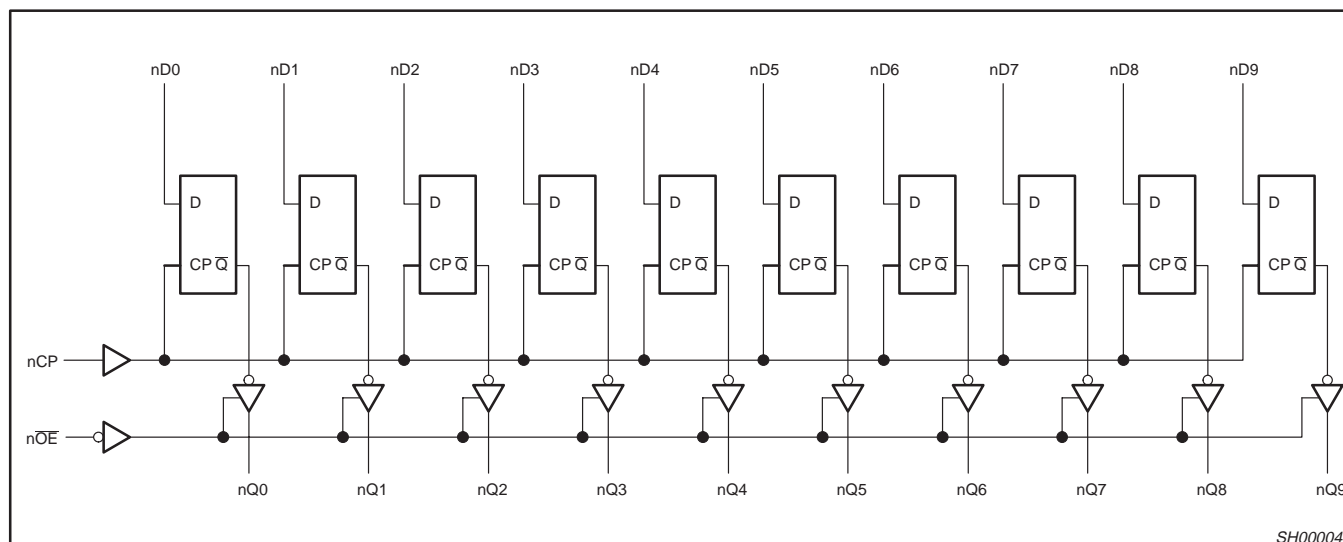


FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
nOE	nCP	nDx		nQ0 - nQ9	
L	↑	L	L	L	Load and read register
L	↑	X	NC	NC	Hold
H	↑	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low to High clock transition
↑ = Not a Low-to-High clock transition

74ABT16821A
74ABTH16821A



ABSOLUTE MAXIMUM RATINGS				
SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	−18	mA
V _I	DC input voltage ³		−1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	−50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	−0.5 to +5.5	V
I _{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T _{sta}	Storage temperature range		−65 to 150	°C

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level Input voltage		0.8	V
I _{OH}	High-level output current		−32	mA
I _{OL}	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	−40	+85	°C

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA			-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}		2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}		3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}		2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}			0.36	0.55		0.55	V
V _{RST}	Power-up output voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}			0.13	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = V _{CC} or GND			±0.01	±1.0		±1.0	μA
I _I	Input leakage current 74ABTH16821A	V _{CC} = 5.5V; V _I = V _{CC} or GND	Control pins		±0.01	±1		±1	μA
		V _{CC} = 5.5V; V _I = V _{CC}	Data pins		0.01	1		1	μA
		V _{CC} = 5.5V; V _I = 0			-1	-3		-5	μA
I _{HOLD}	Bus Hold current inputs ⁵ 74ABTH16821A	V _{CC} = 4.5V; V _I = 0.8V		35			35		μA
		V _{CC} = 4.5V; V _I = 2.0V		-75			-75		
		V _{CC} = 5.5V; V _I = 0 to 5.5V		±800					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V			±5.0	±100		±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care			±5.0	±50		±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}			1.0	10		10	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}			-1.0	-10		-10	μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}			5.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V		-50	-90	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}			0.5	1		1	mA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}			10	19		19	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}			0.5	1		1	mA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND			0.25	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V a transition time of up to 100μsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

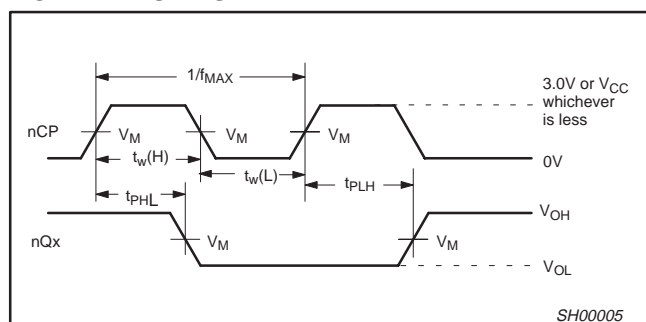
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	1	160	250		160		MHz
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	1	1.3 1.1	2.4 2.0	3.3 2.6	1.3 1.1	3.7 3.0	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	3 4	1.4 1.2	2.5 2.3	3.3 3.0	1.4 1.2	4.1 3.7	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	3 4	1.6 1.3	3.2 2.3	4.1 3.1	1.6 1.3	4.8 3.3	ns

AC SETUP REQUIREMENTS

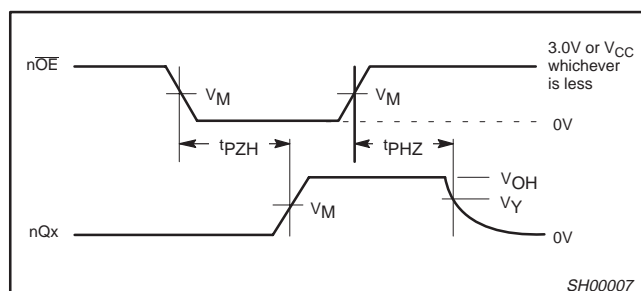
GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T _{amb} = +25°C V _{CC} = +5.0V		T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MIN	MAX	
t _s (H) t _s (L)	Setup time, High or Low nDx to nCP	2	1.8 1.8	1.2 −0.9	1.8 1.8		ns
t _h (H) t _h (L)	Hold time, High or Low nDx to nCP	2	1.0 1.0	0.8 −1.0	1.0 1.0		ns
t _w (H) t _w (L)	nCP pulse width High or Low	1	2.5 2.5	0.8 1.0	2.5 2.5		ns

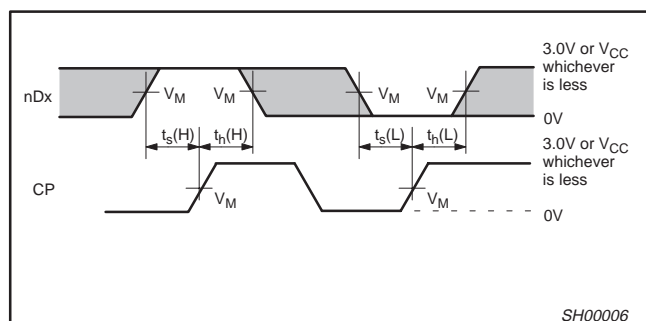
AC WAVEFORMS



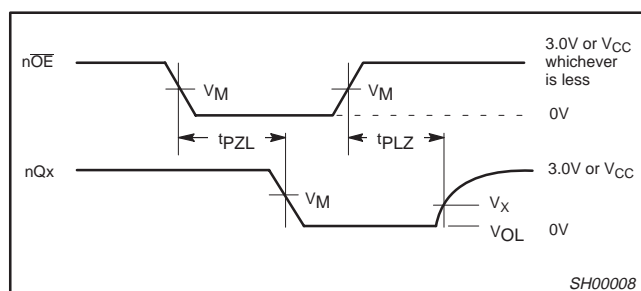
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Data Setup and Hold Times

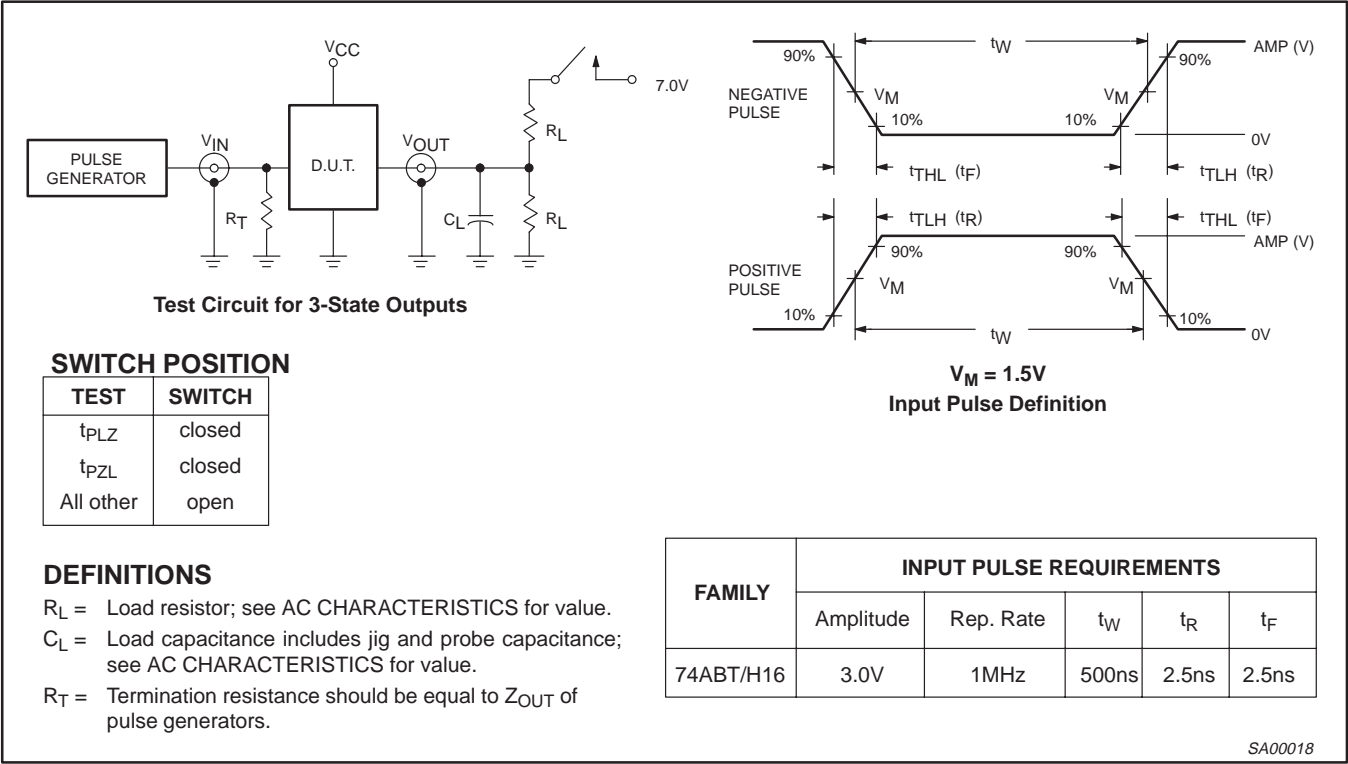


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

20-bit bus-interface D-type flip-flop;
positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

TEST CIRCUIT AND WAVEFORM

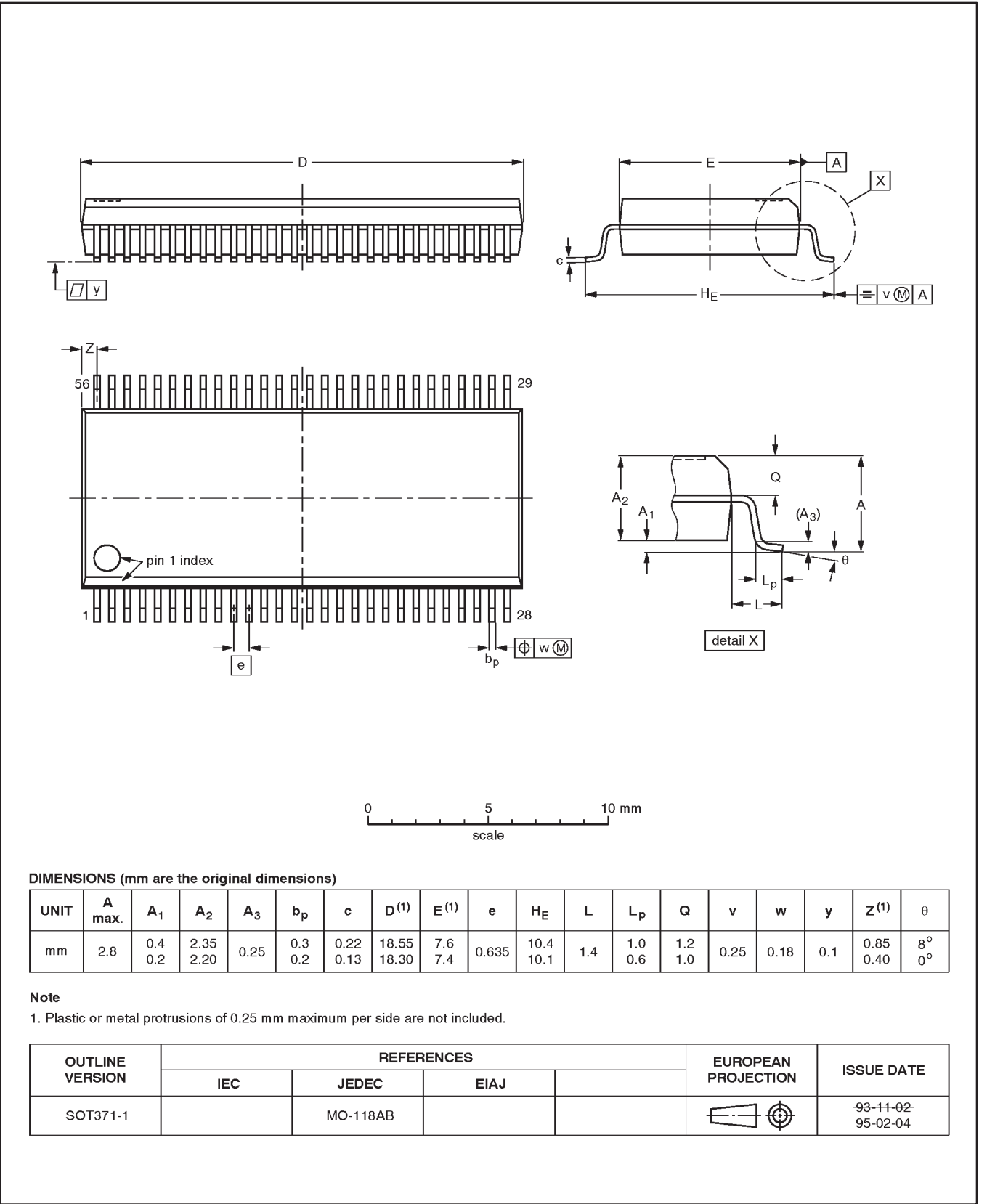


20-bit bus-interface D-type flip-flop;
positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



74ABT16821A
74ABTH16821A

SOT364-1



20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ABT16821A
74ABTH16821A

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1998
All rights reserved. Printed in U.S.A.

print code

Date of release: 05-96

Document order number:

9397-750-03501

Let's make things better.