8-bit transceiver with 9-bit parity checker/ generator and flag latch (3-State)

74ABT853

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector $\overline{\text{ERROR}}$ output
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT853 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT853 is an octal transceiver with a parity generator/checker and is intended for bus–oriented applications.

When Output Enable A ($\overline{\text{OEA}}$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{\text{OEB}}$) controls the B outputs in the same way.

The parity generator creates an odd parity output (PARITY) when $\overline{\text{OEB}}$ is Low. When $\overline{\text{OEA}}$ is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a latch. The error data can then be passed, stored, cleared, or sampled depending on the $\overline{\text{ENABLE}}$ and $\overline{\text{CLEAR}}$ control signals.

If both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

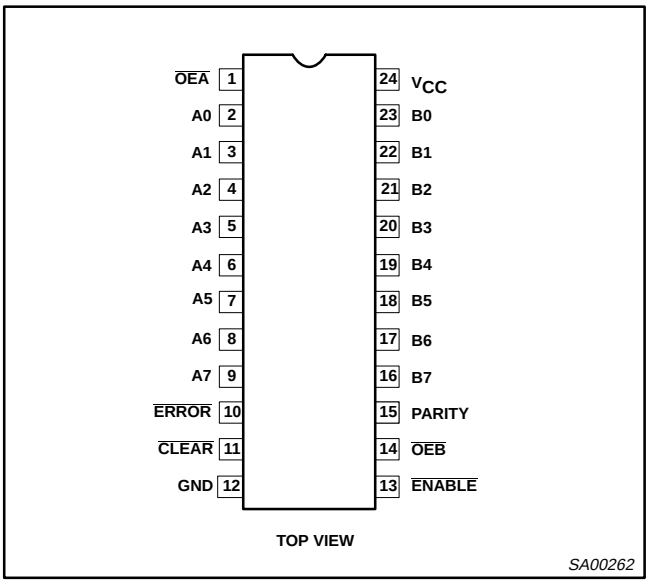
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.4	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	C_L = 50pF; V_{CC} = 5V	7.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	50	µA

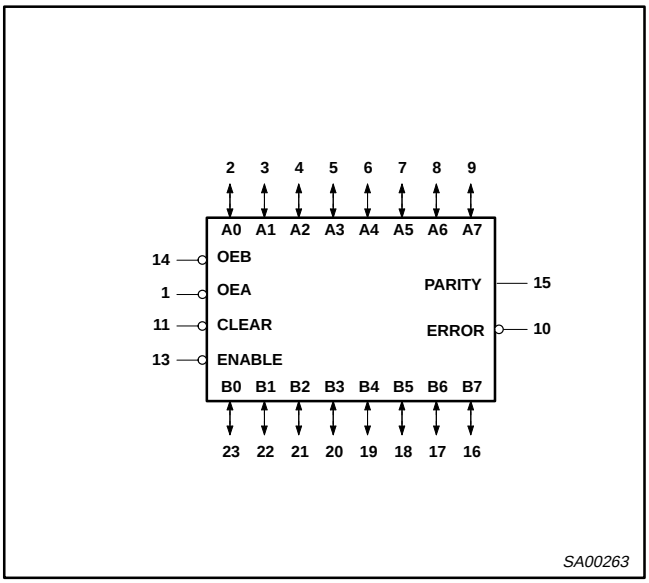
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT853 N	74ABT853 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT853 D	74ABT853 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT853 DB	74ABT853 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT853 PW	74ABT853PW DH	SOT355-1

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 – A7	2, 3, 4, 5, 6, 7, 8, 9	A port 3–State inputs/outputs
B0 – B7	23, 22, 21, 20, 19, 18, 17, 16	B port 3–State inputs/outputs
$\overline{OEA}$	1	Enables the A outputs when Low
$\overline{OEB}$	14	Enables the B outputs when Low
PARITY	15	Parity output/input
$\overline{ERROR}$	10	Error output (open collector)
$\overline{CLEAR}$	11	Clears the error flag register when Low
$\overline{ENABLE}$	13	Enable input (active-Low)
GND	12	Ground (0V)
V_{CC}	24	Positive supply voltage

FUNCTION TABLE

MODE	INPUTS				OUTPUTS		
	$\overline{OEB}$	$\overline{OEA}$	An Σ OF HIGHS	Bn + PARITY Σ OF HIGHS	An	Bn	PARITY
A data to B bus and generate odd parity output	L	H	Odd Even	(output)	(input)	An	L H
B data to A bus and check for parity error[1]	H	L	(output)	X	Bn	(input)	(input)
A bus and B bus disabled[2]	H	H	X	X	Z	Z	Z
A data to B bus and generate inverted parity output	L	L	Odd Even	(output)	(input)	An	H L

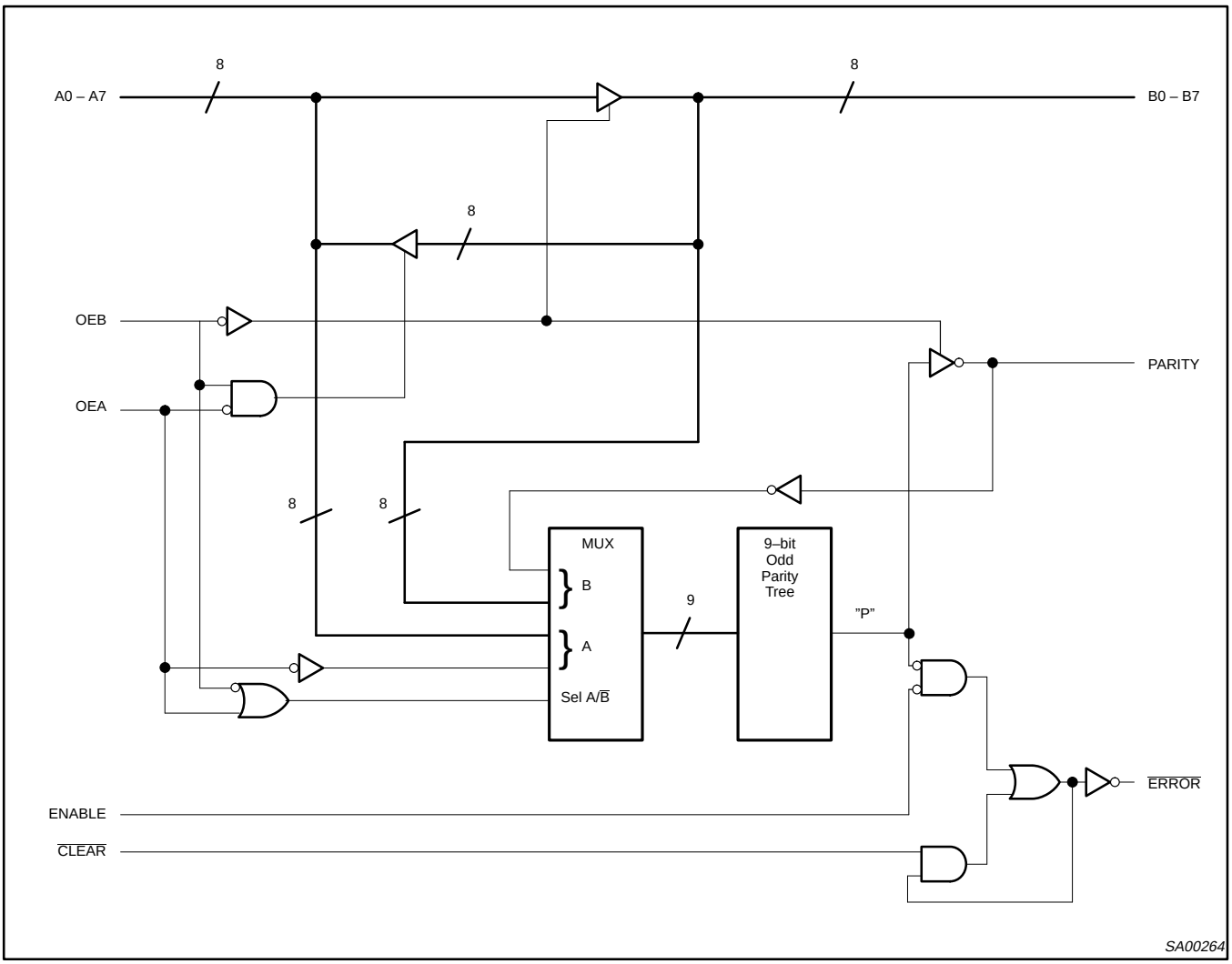
NOTES:
1. Error checking is detailed in the Error Flag Function Table below.
2. When $\overline{ENABLE}$ is Low, $\overline{ERROR}$ is Low if the sum of A inputs is even or $\overline{ERROR}$ is High if the sum of A inputs is odd.

ERROR FLAG FUNCTION TABLE

MODE	INPUTS			INTERNAL NODE	OUTPUT	
	$\overline{ENABLE}$	$\overline{CLEAR}$	Bn + PARITY Σ OF HIGHS	POINT "P"	PRE–STATE $\overline{ERROR}$n–1	$\overline{ERROR}$ OUTPUT
Pass	L	L	Odd Even	H L	X	H L
Sample	L	H	Odd Even X	H L X	H X L	H L L
Clear	H	L	X	X	X	H
Store	H	H	X	X	L H	L H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High–level output voltage All outputs except $\overline{ERROR}$		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[3]		V_{CC} = 2.1V; V_O = 0.5V; V_I = GND or V_{CC}; $V_{\overline{OE}}$ = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		25	38		38	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.01	50		50	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted. The $\overline{ERROR}$ output pin 10 is not included in this spec due to the open collector design.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORMS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±10%		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	4	1.2 1.0	3.4 2.6	4.8 4.0	1.2 1.0	5.3 4.5	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	1, 4	2.1 2.5	7.4 7.4	9.5 9.7	2.1 2.5	11.2 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEA}$ to PARITY	1, 4	1.8 2.3	6.6 6.7	8.5 8.6	1.8 2.3	10.5 10.0	ns
t_{PLH}	Propagation delay $\overline{CLEAR}$ to $\overline{ERROR}$	3	1.0	3.6	5.5	1.0	6.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{ENABLE}$ to $\overline{ERROR}$	4	1.8 1.8	3.8 4.5	5.1 5.8	1.8 1.8	6.0 6.6	ns
t_{PLH} t_{PHL}	Propagation delay Bn or PARITY to $\overline{ERROR}$	1, 4	2.0 3.0	7.9 9.0	10.1 11.5	2.0 3.0	11.7 12.8	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEA}$ to An or $\overline{OEB}$ to Bn, PARITY	2, 5	1.0 2.1	3.2 4.1	5.1 5.8	1.0 2.1	6.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEA}$ to An or $\overline{OEB}$ to Bn, PARITY	2, 5	3.1 3.2	5.1 5.6	7.3 7.2	3.1 3.2	7.9 8.1	ns

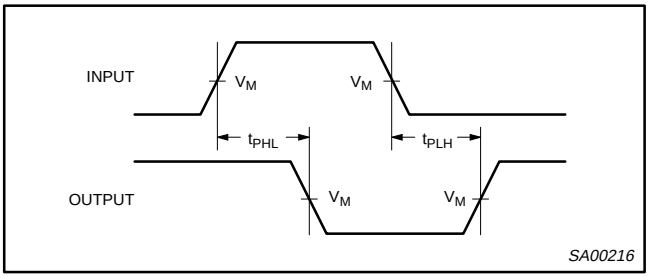
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

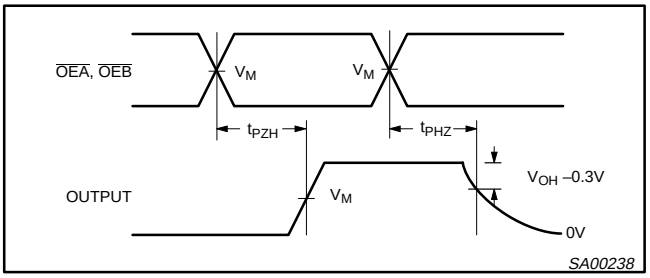
SYMBOL	PARAMETER	WAVEFORMS	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±10%	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Bn or PARITY to $\overline{ENABLE}$	6	8.5 8.5	6.5 3.6	8.5 8.5	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Bn or PARITY to $\overline{ENABLE}$	6	0.0 0.0	–3.4 –6.3	0.0 0.0	ns
$t_s(H)$	Setup time, High $\overline{CLEAR}$ to $\overline{ENABLE}$	6	2.0	–1.6	2.0	ns
$t_h(L)$	Hold time, Low $\overline{CLEAR}$ to $\overline{ENABLE}$	6	3.0	1.8	3.0	ns
$t_w(L)$	Pulse width, Low $\overline{CLEAR}$	3	3.5	1.0	3.5	ns
$t_w(L)$	Pulse width, Low $\overline{ENABLE}$	6	4.0	2.5	4.0	ns

AC WAVEFORMS

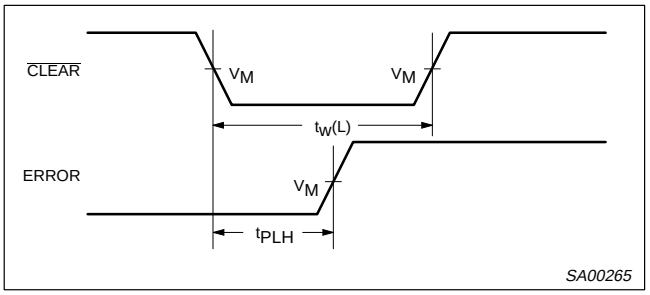
V_M = 1.5V, V_{IN} = GND to 3.0V



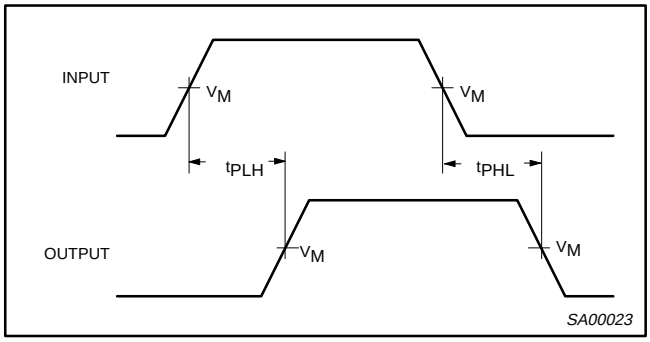
Waveform 1. Propagation Delay For Inverting Output



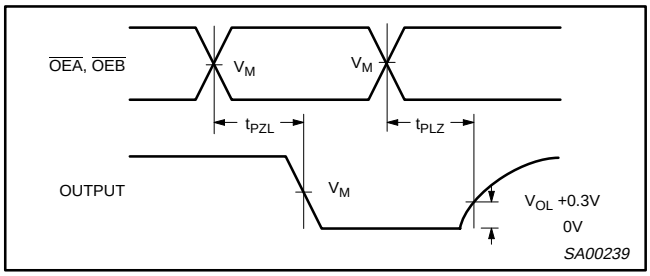
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



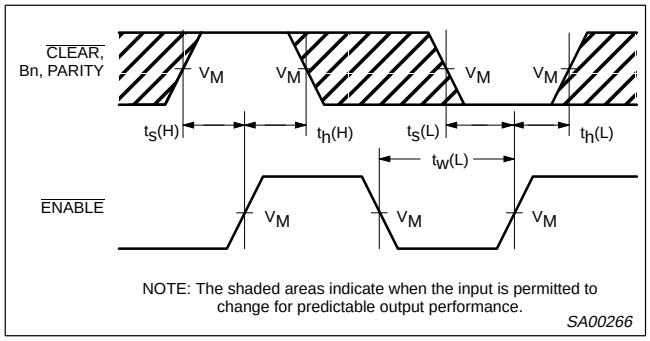
Waveform 3. $\overline{CLEAR}$ Pulse Width and $\overline{CLEAR}$ to $\overline{ERROR}$ Delay



Waveform 4. Propagation Delay For Non-Inverting Output

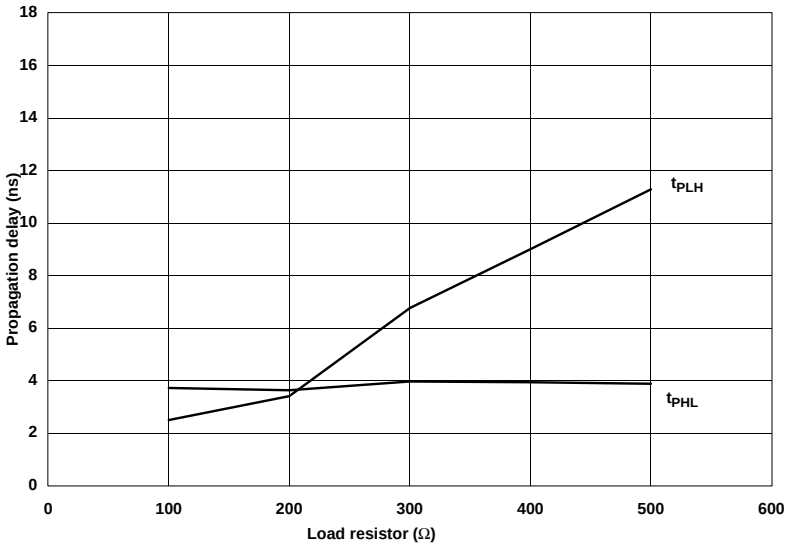


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 6. Data Setup and Hold Times and $\overline{ENABLE}$ Pulse Width

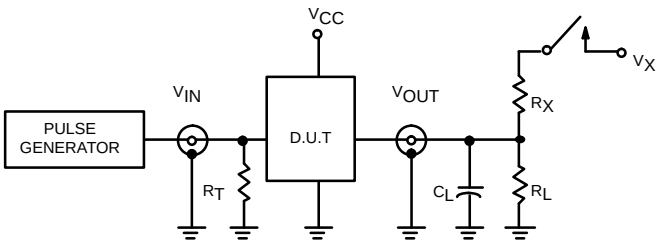
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



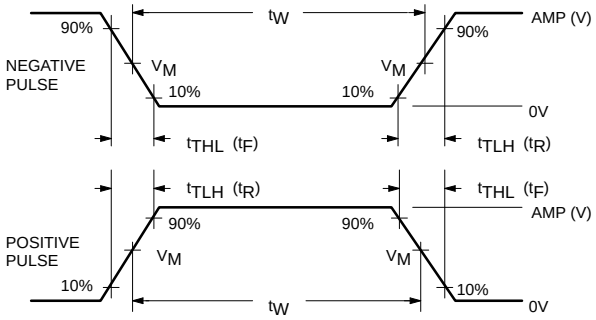
NOTE:
When using Open-Collector parts, the value of the pull–up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} over 300% with only a slight change in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

SA00241

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

LOAD VALUES

OUTPUT	R_X	V_X
$\overline{\text{ERROR}}$	100Ω	V_{CC}
All other	500Ω	7.0V

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00242