DATA SHEET

74ABT16273
16-bit D-type flip-flop

Product data
Replaces data sheet 74ABT/H16273 of 1998 Feb 27

2004 Feb 12

Philips
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16-bit D-type flip-flop 74ABT16273

FEATURES

- 16-bit D-type edge triggered flip-flops
- Output capability: +64 mA/–32 mA
- TTL input and output switching levels
- Live insertion/extraction permitted
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16273 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

This part is a 16-bit edge triggered D-type flip-flop with non-inverting high drive outputs. This device can be used as two 8-bit flip-flops or one 16-bit flip-flop. When the clock (CP) goes High, the data on the D inputs is stored and the Q outputs display the stored data.

This device also features a master reset ($\overline{MR}$) that resets all flip-flops to the Low state when $\overline{MR}$ is set to the Low state.

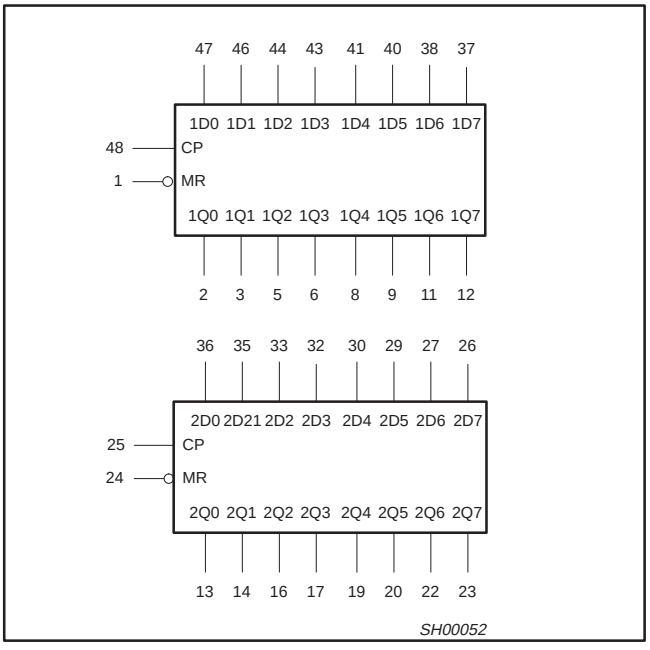
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5.0V	2.5 2.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
I_{CCH}	Quiescent supply current	Outputs High; V_{CC} = 5.5V	200	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16273 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16273 DGG	SOT362-1

LOGIC SYMBOL

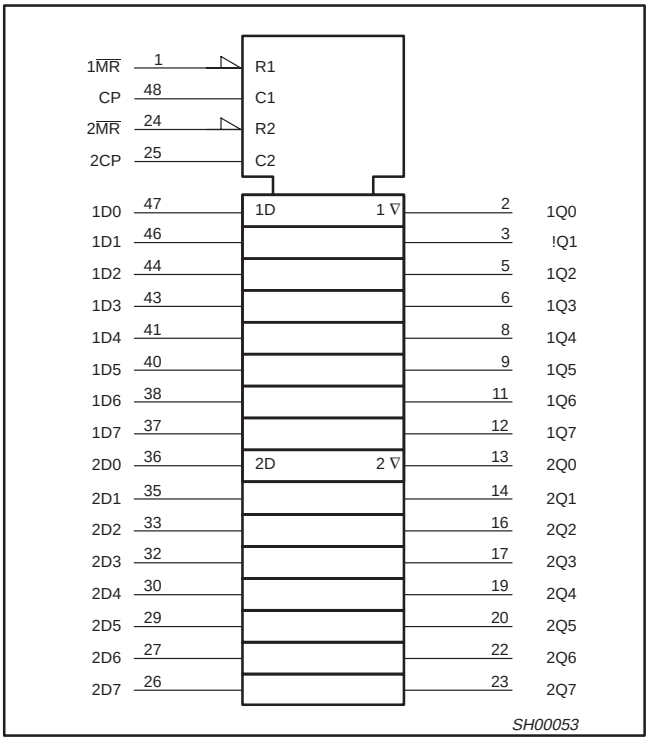


PIN DESCRIPTION

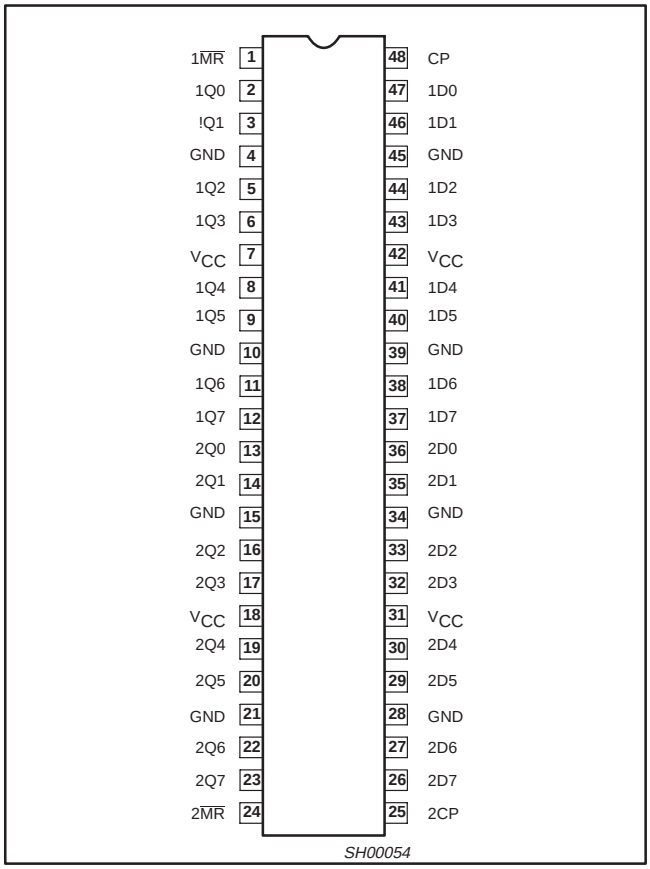
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	1$\overline{MR}$, 2$\overline{MR}$	Master reset input (active-Low)
2, 3, 5, 6, 8, 9, 11, 12,13, 14, 16, 17, 19, 20, 22, 23	1Q0-1Q7 2Q0-2Q7	Data outputs
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0-1D7 2D0-2D7	Data inputs
25, 48	1CP, 2CP	Clock pulse input (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

16-bit D-type flip-flop

LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION

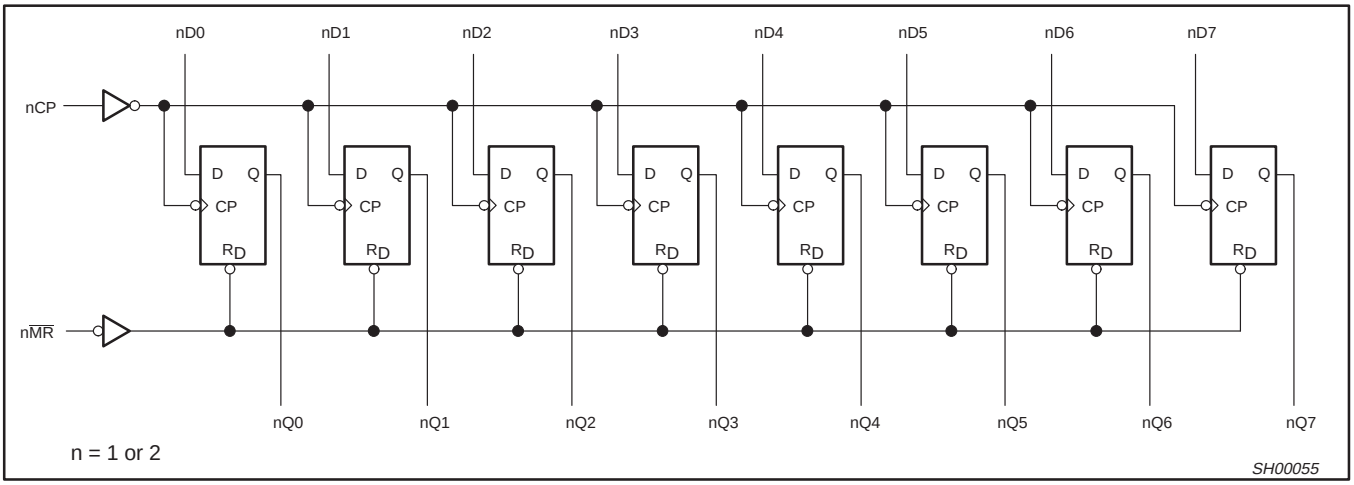


FUNCTION TABLE

Inputs			Output	operating mode
$n\overline{MR}$	nCP	nDX	nQ0-nQ7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load “1”
H	↑	I	L	Load “0”
H	L	X	Q_0	Retain state

H = High voltage level
h = high voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
I = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don’t care
↑ = Low-to-High clock transition
Q_0 = Output as it was

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to –7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			Temp = +25°C			Temp = -40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = –32mA; V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND		±0.1	±1		±1	µA
I_{OFF}	Power-off leakage current	V_{CC}= 0.0V; V_O or V_I < 4.5V		±5.0	±100		±100	µA
I_O	output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–70	–180	–50	–180	mA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.2	1		1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		8	19		19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V. Other inputs at V_{CC} or GND		5	100		100	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω;

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = –40 to +85 °C V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.5 1.2	2.5 2.0	3.4 2.7	1.5 1.2	4.0 3.0	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQx	2	1.9	3.7	4.3	1.9	5.3	ns
f_{MAX}	Maximum clock frequency	1	150	240		150		MHz

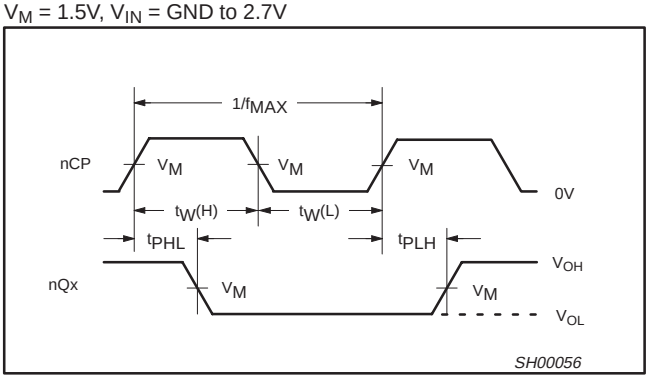
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω

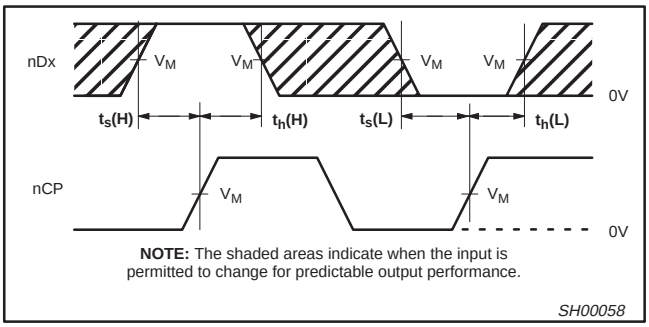
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = –40 to +85 °C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_S(H)$ $t_S(L)$	Setup time, High or Low nDx to nCP	3	2.0 2.0	1.0 1.0	2.0 2.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	3	0 0	–0.6 –0.6	0 0	ns
$t_W(H)$ $t_W(L)$	Clock pulse width High or Low	1	3.3 3.3	1.2 1.0	3.3 3.3	ns
$t_W(L)$	Master Reset pulse width, Low	2	3.3	1.1	3.3	ns
t_{REC}	Recovery time $n\overline{MR}$ + nCP	2	2.0	0.0	2.0	ns

AC WAVEFORMS

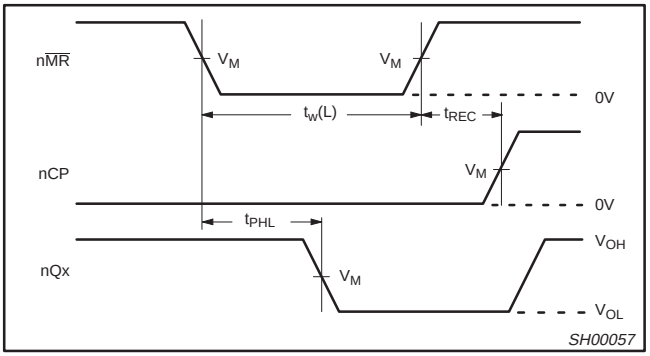
V_M = 1.5V, V_{IN} = GND to 2.7V



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

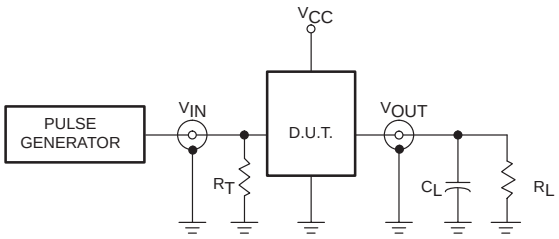


Waveform 3. Data Setup and Hold Times

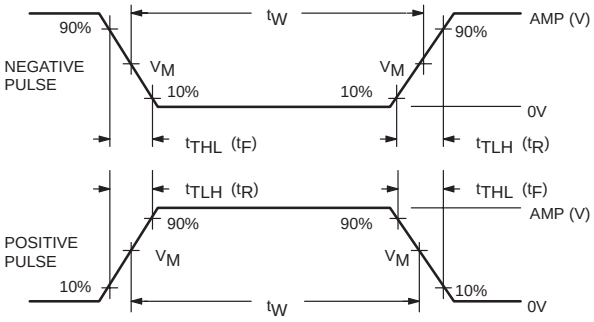


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

TEST CIRCUIT AND WAVEFORM



Test Circuit for Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

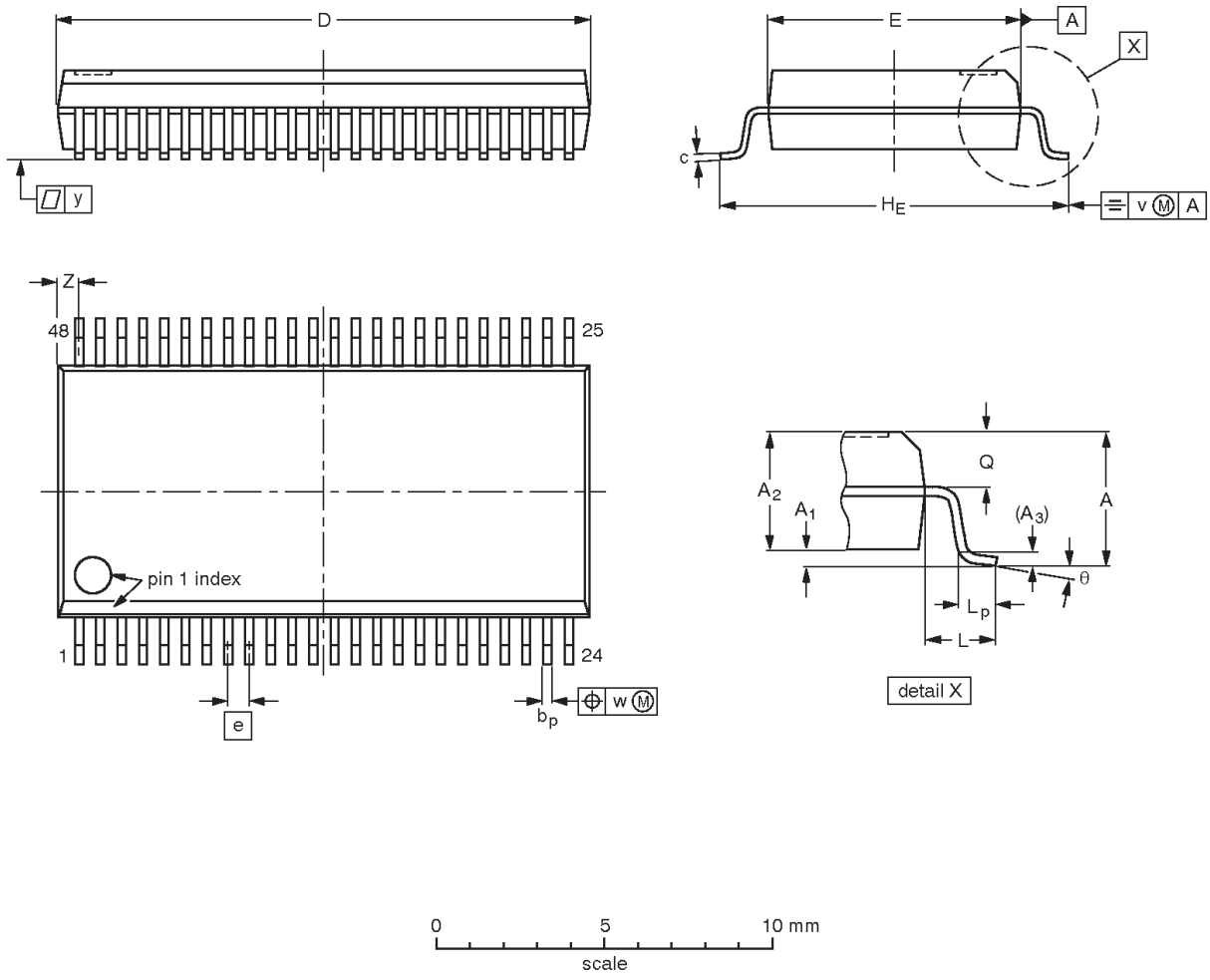
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00059

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

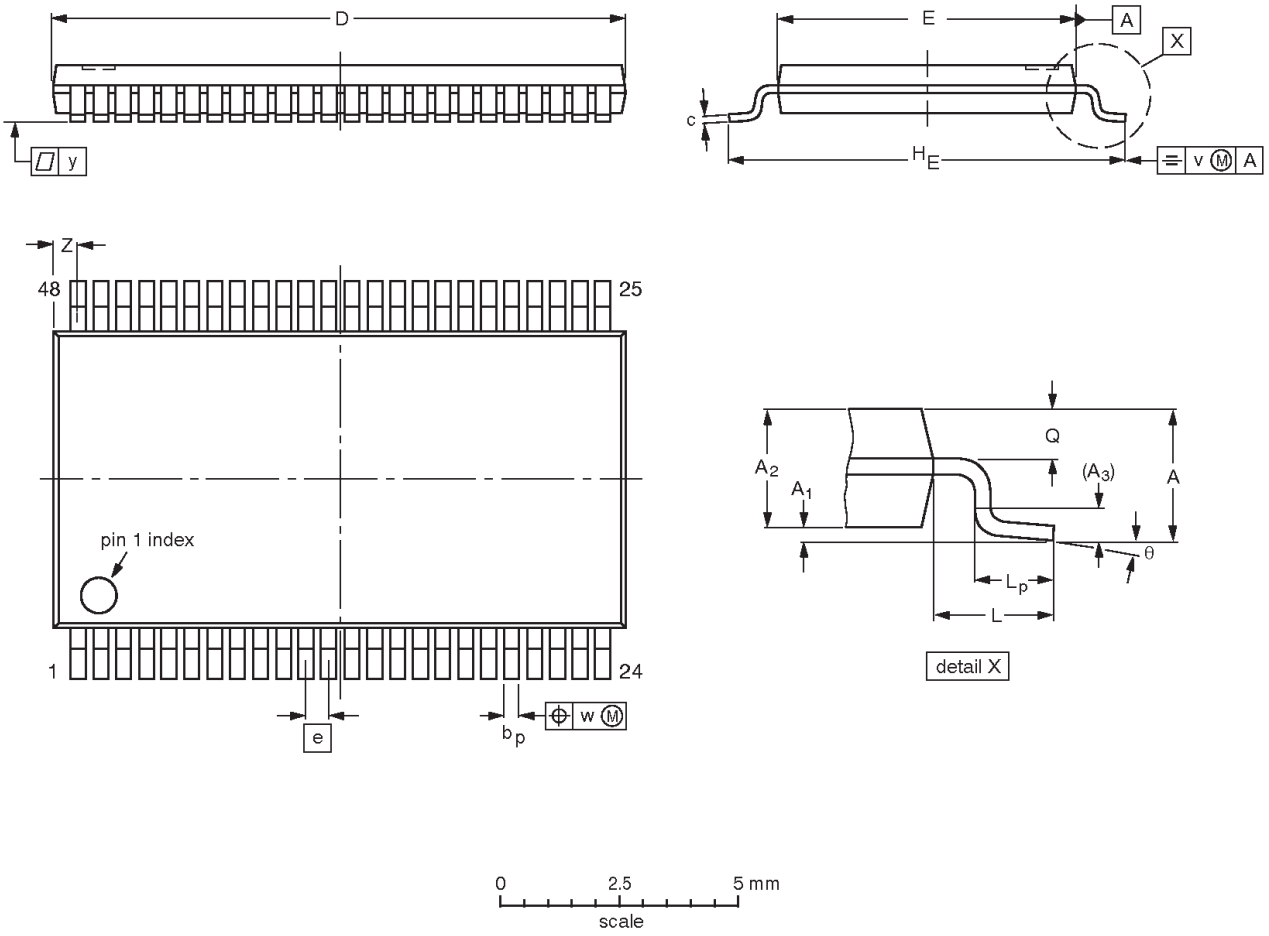
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_3	20040212	**Product data (9397 750 12892); 853-1793 ECN 01–A15421 of 26 January 2004. Replaces data sheet 74ABT_H16273_2 of 1998 Feb 27 (9397 750 03489).** Modifications: ● Delete all references to 74ABTH16273 (product discontinued).
_2	19980227	**Product data (9397 750 03489); ECN 853-1793 19027 of 27 February 1998. Supersedes initial version.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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