DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT7403

4-Bit x 64-word FIFO register; 3-state

Product specification
Supersedes data of October 1990
File under Integrated Circuits, IC06

September 1993

Philips Semiconductors

PHILIPS

4-Bit x 64-word FIFO register; 3-state 74HC/HCT7403

FEATURES

- Synchronous or asynchronous operation
- 3-state outputs
- 30 MHz (typical) shift-in and shift-out rates
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: driver (8 mA)
- I_{CC} category: LSI.

APPLICATIONS

- High-speed disc or tape controller
- Communications buffer.

GENERAL DESCRIPTION

The 74HC/HCT7403 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no.7A.

The “7403” is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 4 bits. A guaranteed 15 MHz data-rate makes it ideal for high-speed applications. A higher data-rate can be obtained in applications where the status flags are not used (burst-mode).

With separate controls for shift-in (SI) and shift-out ($\overline{SO}$), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input ($\overline{MR}$), an output enable input ($\overline{OE}$) and flags. The data-in-ready (DIR) and data-out-ready (DOR) flags indicate the status of the device.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$, SI to DIR and DOR	C_L = 15 pF; V_{CC} = 5 V	15	17	ns
f_{max}	maximum clock frequency		30	30	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	note 1	475	490	pF

Note

1. For HC the condition is V_I = GND to V_{CC}.
   For HCT the condition is V_I = GND to V_{CC} –1.5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7403N	16	DIL	plastic	SOT38Z
74HC/HCT7403D	16	SO16L	plastic	SOT162

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{OE}$	1	output enable input (active LOW)
DIR	2	data-in-ready output
SI	3	shift-in input (active HIGH)
D_O to D_3	4, 5, 6, 7	parallel data input
GND	8	ground
$\overline{MR}$	9	asynchronous master-reset input (active LOW)
Q_3 to Q_0	10, 11, 12, 13	data output
DOR	14	data-out-ready output
$\overline{SO}$	15	shift-out input (active LOW)
V_{CC}	16	positive supply voltage

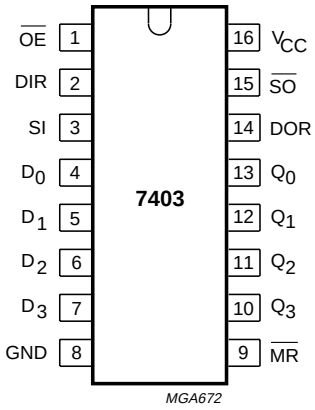


Fig.1 Pin configuration.

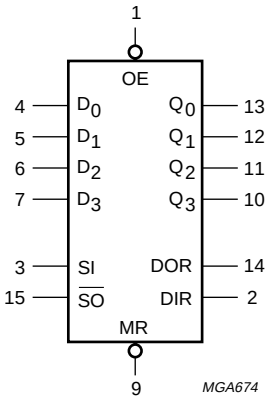


Fig.2 Logic symbol.

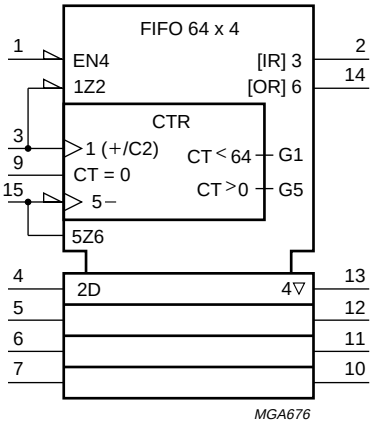


Fig.3 IEC logic symbol.

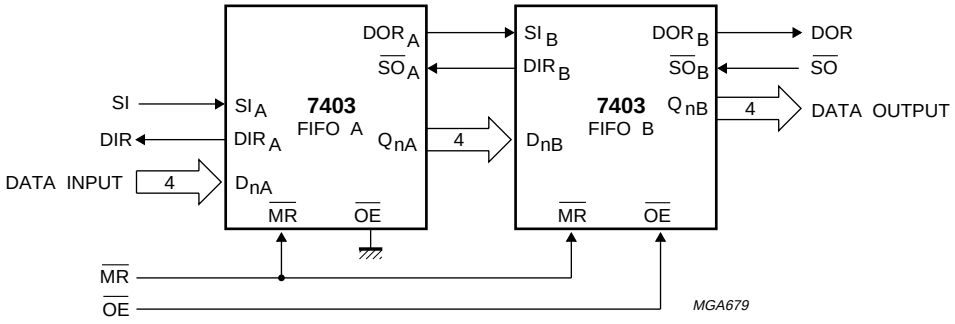


Fig.4 Functional diagram.

FUNCTIONAL DESCRIPTION

A DIR flag indicates the input stage status, either empty and ready to receive data (DIR = HIGH) or full and busy (DIR = LOW). When DIR and SI are HIGH, data present at D_0 to D_3 is shifted into the input stage; once complete DIR goes LOW. When SI is set LOW, data is automatically shifted to the output stage or to the last empty location. A FIFO which can receive data is indicated by DIR set HIGH.

A DOR flag indicates the output stage status, either data available (DOR = HIGH) or busy (DOR = LOW). When $\overline{SO}$ and DOR are HIGH, data is available at the outputs (Q_0 to Q_3). When $\overline{SO}$ is set LOW new data may be shifted into the output stage, once complete DOR is set HIGH.

Expanded format (see Fig.17)

The DOR and DIR signals are used to allow the “7403” to be cascaded. Both parallel and serial expansion is possible.

Serial expansion is only possible with typical devices.

Parallel expansion

Parallel expansion is accomplished by logically ANDing the DOR and DIR signals to form a composite signal.

Serial expansion

Serial expansion is accomplished by:

- tying the data outputs of the first device to the data inputs of the second device
- connecting the DOR pin of the first device to the SI pin of the second device
- connecting the $\overline{SO}$ pin of the first device to the DIR pin of the second device.

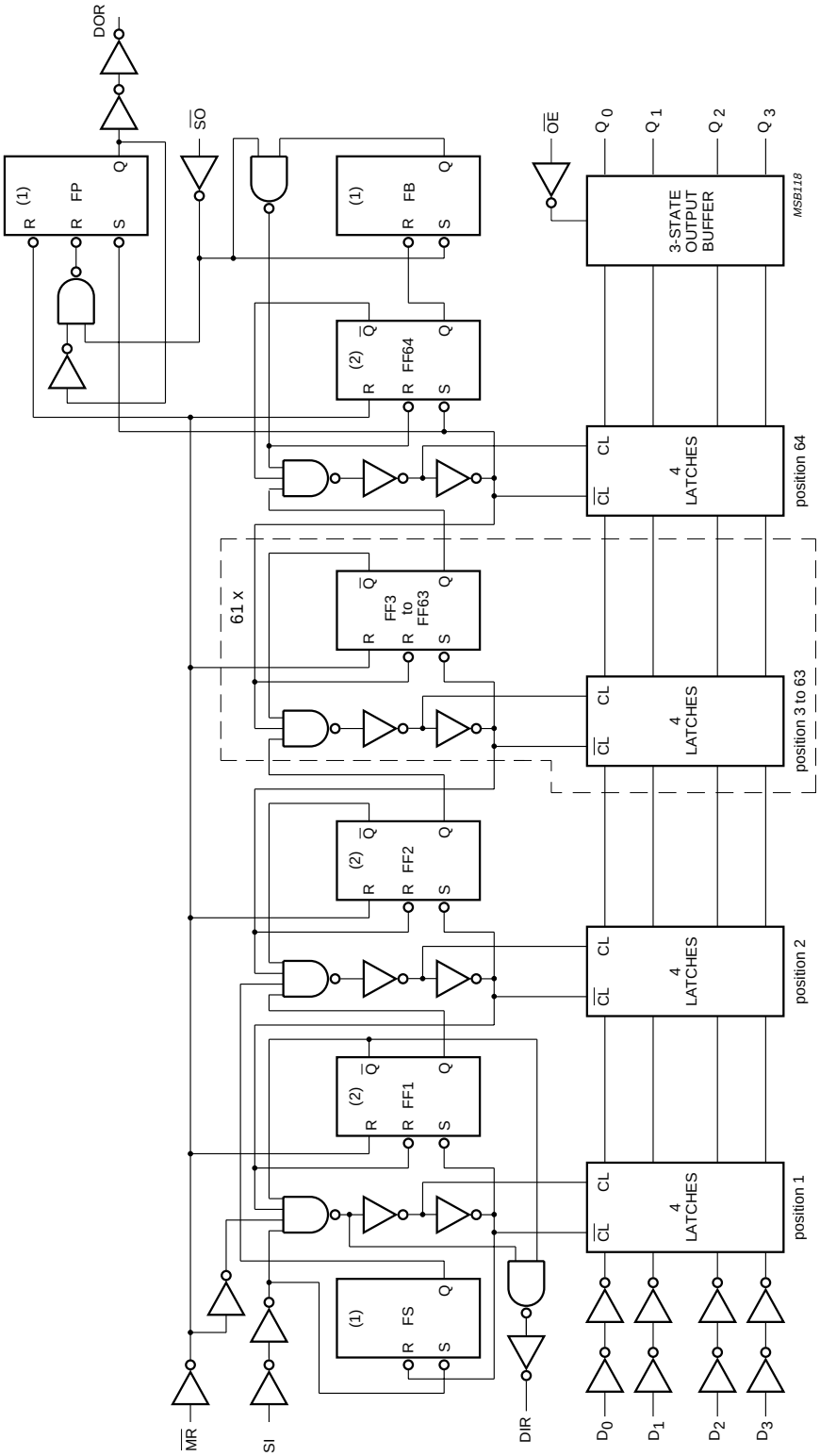


Fig.5 Logic diagram.

(see control flip-flops)
LOW on $\overline{S}$ input of flip-flops FS, FB and FP will set Q output to HIGH independent of state on $\overline{R}$ input.
LOW on $\overline{R}$ input of FF1 to FF64 will set Q output to LOW independent of state on $\overline{S}$ input.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*, except that V_{OH} and V_{OL} are not valid for driver output.

They are replaced by the values given below.

Output capability: driver 8 mA
I_{CC} category: LSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HC

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			–40 to +85		–40 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = –20 µA
V_{OH}	HIGH level output voltage driver outputs	3.98 5.48	4.32 5.81	– –	3.84 5.34	– –	3.70 5.20	– –	V V	4.5 6.0	V_{IH} or V_{IL}	I_O = –8 mA I_O = –10 mA
V_{OL}	LOW level output voltage all outputs	– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V V V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 µA
V_{OL}	LOW level output voltage driver outputs	– –	0.15 0.15	0.26 0.26	– –	0.33 0.33	– –	0.40 0.40	V V	4.5 6.0	V_{IH} or V_{IL}	I_O = 8 mA I_O = 10 mA

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to DIR, DOR	– – –	69 25 20	210 42 36	– – –	265 53 45	– – –	315 63 54	ns ns ns	2.0 4.5 6.0	Fig.8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	– – –	52 19 15	160 32 27	– – –	200 40 34	– – –	240 48 41	ns ns ns	2.0 4.5 6.0	Fig.8
t_{PHL}/t_{PLH}	propagation delay SI to DIR	– – –	66 24 19	205 41 35	– – –	255 51 43	– – –	310 62 53	ns ns ns	2.0 4.5 6.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to DOR	– – –	94 34 27	290 58 49	– – –	365 73 62	– – –	435 87 74	ns ns ns	2.0 4.5 6.0	Fig.9
t_{PHL}/t_{PLH}	propagation delay DOR to Q_n	– – –	11 4 3	35 7 6.0	– – –	45 9 8	– – –	55 11 9	ns ns ns	2.0 4.5 6.0	Fig.10
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n	– – –	105 38 30	325 65 55	– – –	406 81 69	– – –	488 98 83	ns ns ns	2.0 4.5 6.0	Fig.14
t_{PLH}	propagation delay/ripple through delay SI to DOR	– – –	2.2 0.8 0.6	7 1.4 1.2	– – –	8.8 1.8 1.5	– – –	10.5 2.1 1.8	µs µs µs	2.0 4.5 6.0	Fig.10
t_{PLH}	propagation delay/bubble-up delay $\overline{SO}$ to DIR	– – –	2.8 1.0 0.8	9 1.8 1.5	– – –	11.2 2.2 1.9	– – –	13.5 2.7 2.3	µs µs µs	2.0 4.5 6.0	Fig.7
t_{PZH}/t_{PZL}	3-state output enable $\overline{OE}$ to Q_n	– – –	44 16 13	150 30 26	– – –	190 38 32	– – –	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.16
t_{PHZ}/t_{PLZ}	3-state output disable $\overline{OE}$ to Q_n	– – –	50 18 14	150 30 26	– – –	190 38 33	– – –	225 45 38	ns ns ns	2.0 4.5 6.0	Fig.16
t_{THL}/t_{TLH}	output transition time	– – –	14 5 4	60 12 10	– – –	75 15 13	– – –	90 18 15	ns ns ns	2.0 4.5 6.0	Fig.16
t_W	SI pulse width HIGH or LOW	35 7 6.0	11 4 3	– – –	45 9 8	– – –	55 11 9	– – –	ns ns ns	2.0 4.5 6.0	Fig.6
t_W	$\overline{SO}$ pulse width HIGH or LOW	70 14 12	22 8 6.0	– – –	90 18 15	– – –	105 21 18	– – –	ns ns ns	2.0 4.5 6.0	Fig.9

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			–40 to +85		–40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_W	DIR pulse width HIGH	10 5 4	41 15 12	130 26 22	8 4 3	165 33 28	8 4 3	195 39 33	ns ns ns	2.0 4.5 6.0	Fig.7
t_W	DOR pulse width HIGH	14 7 6.0	52 19 15	160 32 27	12 6 5	200 40 34	12 6.0 5.0	240 48 41	ns ns ns	2.0 4.5 6.0	Fig.10
t_W	$\overline{MR}$ pulse width LOW	120 24 20	39 14 11	– – –	150 30 26	– – –	180 36 31	– – –	ns ns ns	2.0 4.5 6.0	Fig.8
t_{rem}	removal time $\overline{MR}$ to SI	80 16 14	24 8 7	– – –	100 20 17	– – –	120 24 20	– – –	ns ns ns	2.0 4.5 6.0	Fig.15
t_{su}	set-up time D_n to SI	–8 –4 –3	–36 –13 –10	– – –	–6 –3 –3	– – –	–6 –3 –3	– – –	ns ns ns	2.0 4.5 6.0	Fig.13
t_h	hold time D_n to SI	135 27 23	44 16 13	– – –	170 34 29	– – –	205 41 35	– – –	ns ns ns	2.0 4.5 6.0	Fig.13
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ burst mode	3.6 18 21	9.9 30 36	– – –	2.8 14 16	– – –	2.4 12 14	– – –	MHz MHz MHz	2.0 4.5 6.0	Figs 11 and 12
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ using flags	3.6 18 21	9.9 30 36	– – –	2.8 14 16	– – –	2.4 12 14	– – –	MHz MHz MHz	2.0 4.5 6.0	Figs 6 and 9
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ cascaded	– – –	7.6 23 27	– – –	– – –	– – –	– – –	– – –	MHz MHz MHz	2.0 4.5 6.0	Figs 6 and 9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*, except that V_{OH} and V_{OL} are not valid for driver output.
They are replaced by the values given below.

Output capability: driver 8 mA.
I_{CC} category: LSI.

Voltages are referenced to GND (ground = 0 V).

DC CHARACTERISTICS FOR 74HCT

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage all outputs	4.4	4.5	–	4.4	–	4.4	–	V	4.5	V_{IH} or V_{IL}	I_O = –20 µA
V_{OH}	HIGH level output voltage driver outputs	3.98	4.32	–	3.84	–	3.7	–	V	4.5	V_{IH} or V_{IL}	I_O = –8 mA
V_{OL}	LOW level output voltage all outputs	–	0	0.1	–	0.1	–	0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 µA
V_{OL}	LOW level output voltage driver outputs	–	0.15	0.26	–	0.33	–	0.4	V	4.5	V_{IH} or V_{IL}	I_O = 8 mA

Notes to the HCT DC Characteristics

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
2. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	1
SI	1.5
D_n	0.75
$\overline{MR}$	1.5
$\overline{SO}$	1.5

AC CHARACTERISTICS FOR 74HCT

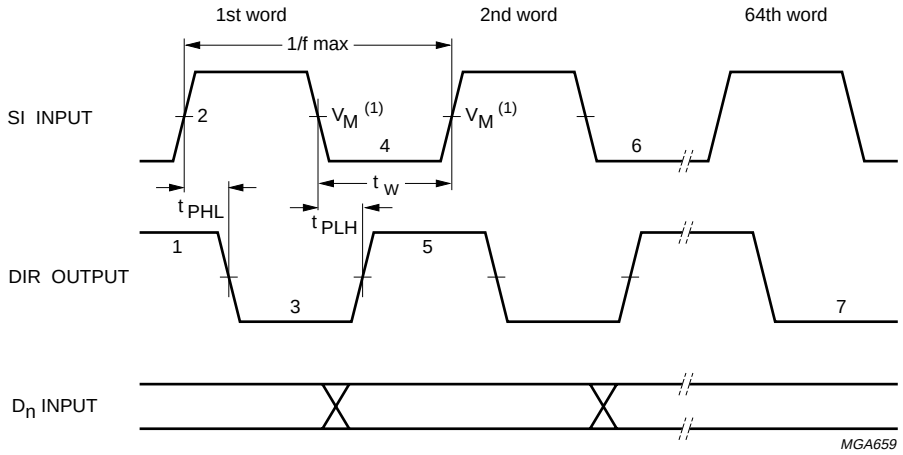
GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		−25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay $\overline{MR}$ to DIR, DOR	–	30	51	–	53	–	63	ns	4.5	Fig.8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	–	22	38	–	48	–	57	ns	4.5	Fig.8
t_{PHL}/t_{PLH}	propagation delay SI to DIR	–	25	43	–	54	–	65	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to DOR	–	36	61	–	76	–	92	ns	4.5	Fig.9
t_{PHL}/t_{PLH}	propagation delay $\overline{SO}$ to Q_n	–	42	72	–	90	–	108	ns	4.5	Fig.14
t_{PHL}/t_{PLH}	propagation delay DOR to Q_n	–	7	12	–	15	–	18	ns	4.5	Fig.10
t_{PLH}	propagation delay/ripple through delay SI to DOR	–	0.8	1.4	–	1.75	–	2.1	µs	4.5	Fig.10
t_{PLH}	propagation delay/bubble-up delay $\overline{SO}$ to DIR	–	1	1.8	–	2.25	–	2.7	µs	4.5	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	16	30	–	38	–	45	ns	4.5	Fig.16
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	19	30	–	38	–	45	ns	4.5	Fig.16
t_{THL}/t_{TLH}	output transition time	–	5	12	–	15	–	18	ns	4.5	Fig.16
t_W	SI pulse width HIGH or LOW	9	5	–	6	–	8	–	ns	4.5	Fig.6
t_W	$\overline{SO}$ pulse width HIGH or LOW	14	8	–	18	–	21	–	ns	4.5	Fig.9
t_W	DIR pulse width HIGH	5	17	29	4	36	4	44	ns	4.5	Fig.7

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		–25			–40 to +85		–40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_W	DOR pulse width HIGH	7	21	36	6.0	45	6.0	54	ns	4.5	Fig.10
t_W	$\overline{MR}$ pulse width LOW	26	15	–	33	–	39	–	ns	4.5	Fig.8
t_{rem}	removal time $\overline{MR}$ to SI	18	10	–	23	–	27	–	ns	4.5	Fig.15
t_{su}	set-up time D_n to SI	–5	–16	–	–4	–	–4	–	ns	4.5	Fig.13
t_h	hold time D_n to SI	30	18	–	38	–	45	–	ns	4.5	Fig.13
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ burst mode	18	30	–	14	–	12	–	MHz	4.5	Figs 11 and 12
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ using flags	18	30	–	14	–	12	–	MHz	4.5	Figs 6 and 9
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ cascaded	–	23	–	–	–	–	–	MHz	4.5	Figs 6 and 9

AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full



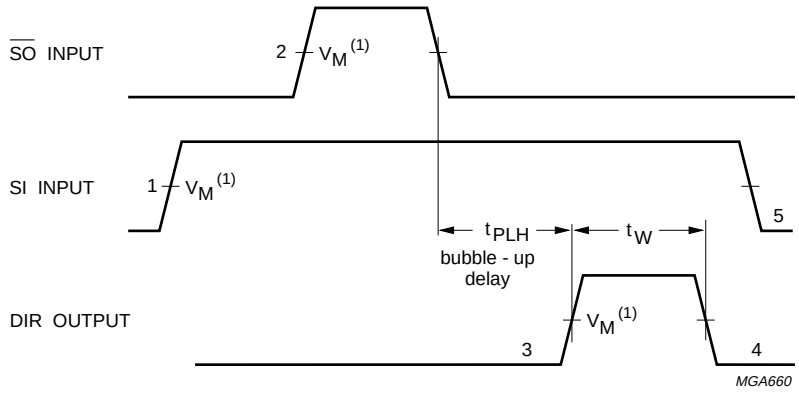
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the SI input to DIR output propagation delay, the SI pulse width and SI maximum pulse frequency.

Notes to Fig.6

1. DIR initially HIGH; FIFO is prepared for valid data
2. SI set HIGH; data loaded into input stage
3. DIR goes LOW, input stage “busy”
4. SI set LOW; data from first location “ripple through”
5. DIR goes HIGH, status flag indicates FIFO prepared for additional data
6. Repeat process to load 2nd word through to 64th word into FIFO
   DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

With FIFO full; SI held HIGH in anticipation of empty location



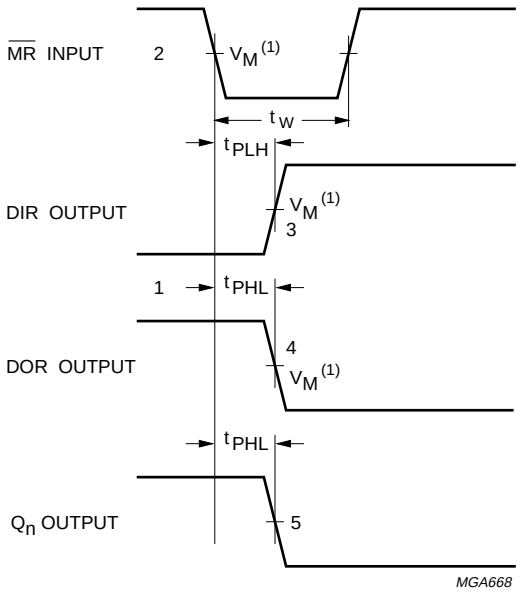
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing bubble-up delay, $\overline{SO}$ input to DIR output and DIR output pulse width.

Notes to Fig.7

1. FIFO is initially full, shift-in is held HIGH
2. $\overline{SO}$ pulse; data in the output stage is unloaded, “bubble-up” process of empty location begins
3. DIR HIGH; when empty location reaches input stage, flag indicates FIFO is prepared for data input
4. DIR returns to LOW; data shift-in to empty location is complete, FIFO is full again
5. SI set LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

Master reset applied with FIFO full

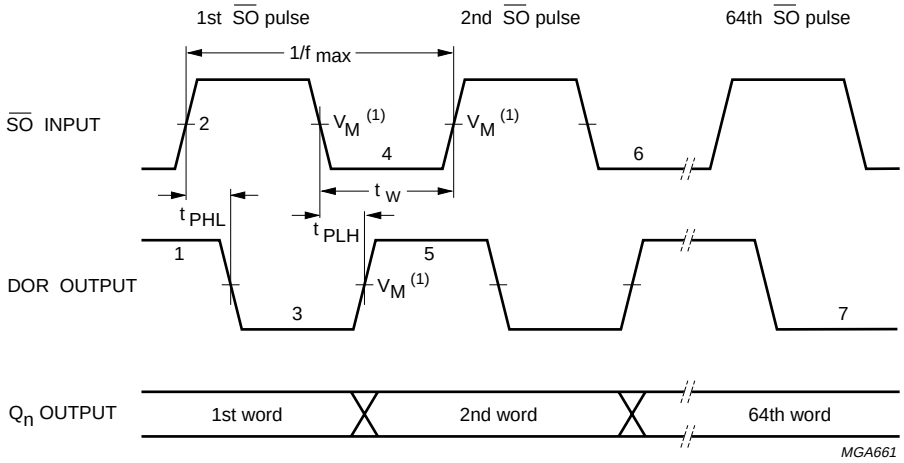


(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the $\overline{MR}$ input to DIR, DOR and Q_n output propagation delays and the $\overline{MR}$ pulse width.

Notes to Fig.8

1. DIR LOW, output ready HIGH; assume FIFO is full
2. $\overline{MR}$ pulse LOW; clears FIFO
3. DIR goes HIGH; flag indicates input prepared for valid data
4. DOR goes LOW; flag indicates FIFO empty
5. Q_n outputs go LOW (only last bit will be reset).



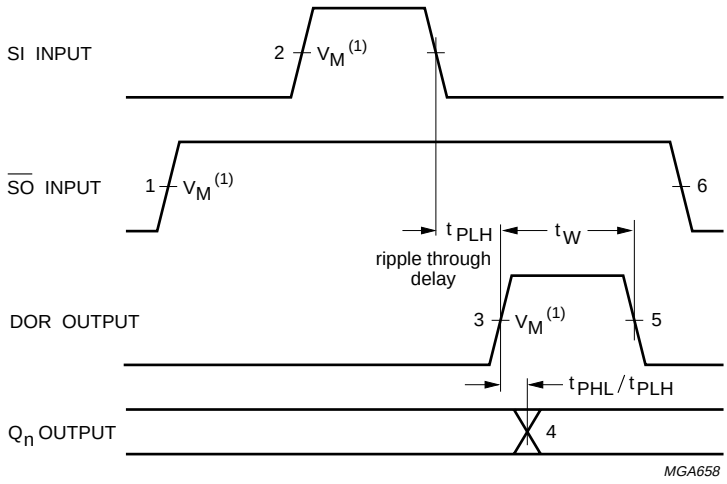
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the $\overline{SO}$ input to DOR output propagation delay. The $\overline{SO}$ pulse widths and maximum pulse frequency.

Notes to Fig.9

1. DOR HIGH; no data transfer in progress, valid data is present at output stage
2. $\overline{SO}$ set HIGH; results in DOR going LOW
3. DOR goes LOW; output stage “busy”
4. $\overline{SO}$ set LOW; data in the input stage is unloaded, and new data replaces it as empty location “bubbles-up” to input stage
5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay
6. Repeat process to unload the 3rd through to the 64th word from FIFO
7. DOR remains LOW; FIFO is empty.

With FIFO empty; $\overline{SO}$ is held HIGH in anticipation



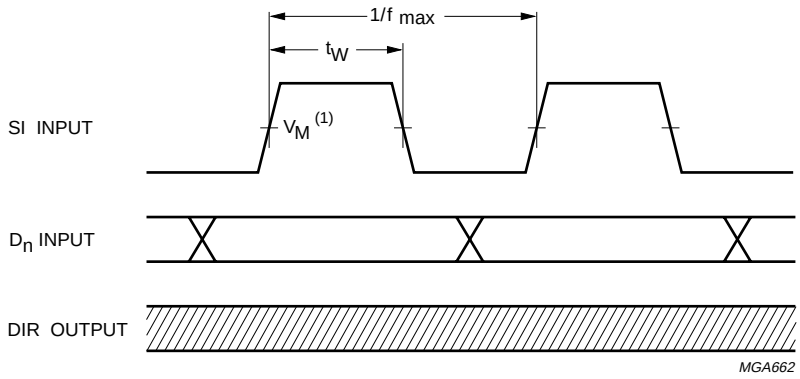
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.10 Waveforms showing ripple through delay SI input to DOR output, DOR output pulse width and propagation delay from the DOR pulse to the Q_n output.

Notes to Fig.10

1. FIFO is initially empty, $\overline{SO}$ is held HIGH
2. SI pulse; loads data into FIFO and initiates ripple through process
3. DOR flag signals the arrival of valid data at the output stage
4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output
5. DOR goes LOW; data shift-out is complete, FIFO is empty again
6. $\overline{SO}$ set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.

Shift-in operation; high-speed burst mode



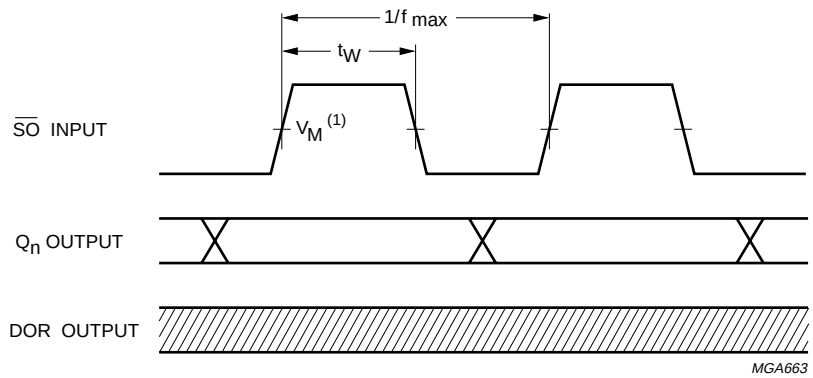
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.11 Waveforms showing SI minimum pulse width and maximum pulse frequency, in high-speed shift-in burst mode.

Note to Fig.11

In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

Shift-out operation; high-speed burst mode

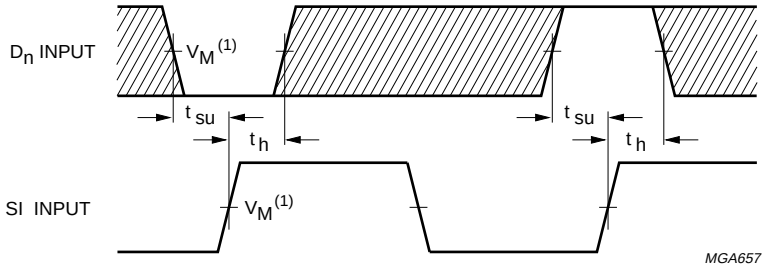


(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.12 Waveforms showing $\overline{SO}$ minimum pulse width and maximum pulse frequency, in high-speed shift-out burst mode.

Note to Fig.12

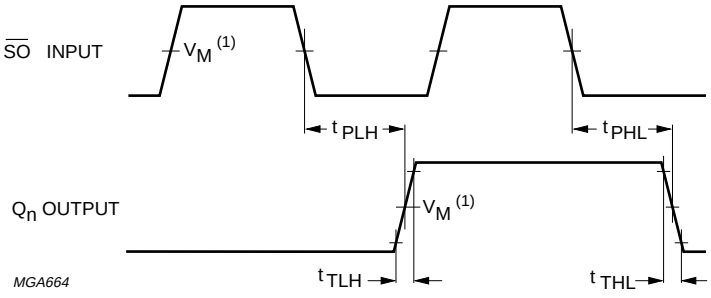
In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and an $\overline{SO}$ pulse can be applied without regard to the flag.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

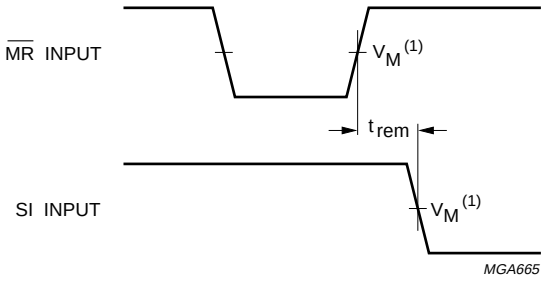
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.13 Waveforms showing hold and set-up times for D_n input to SI input.



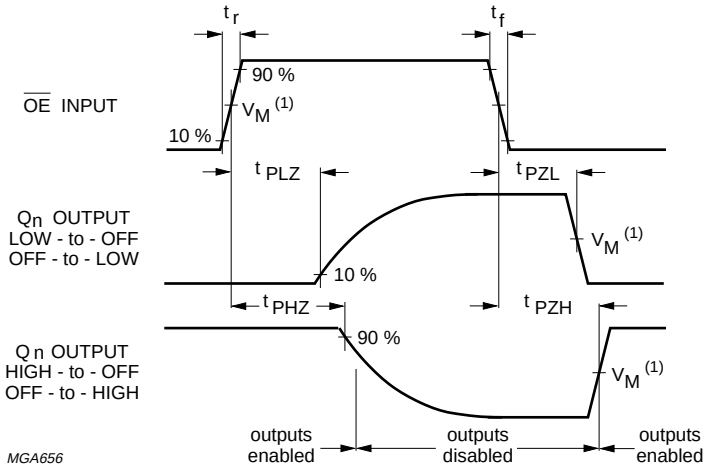
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.14 Waveforms showing $\overline{SO}$ input to Q_n output propagation delays and output transition time.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.15 Waveform showing the $\overline{MR}$ input to SI input removal time.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.16 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

APPLICATION INFORMATION

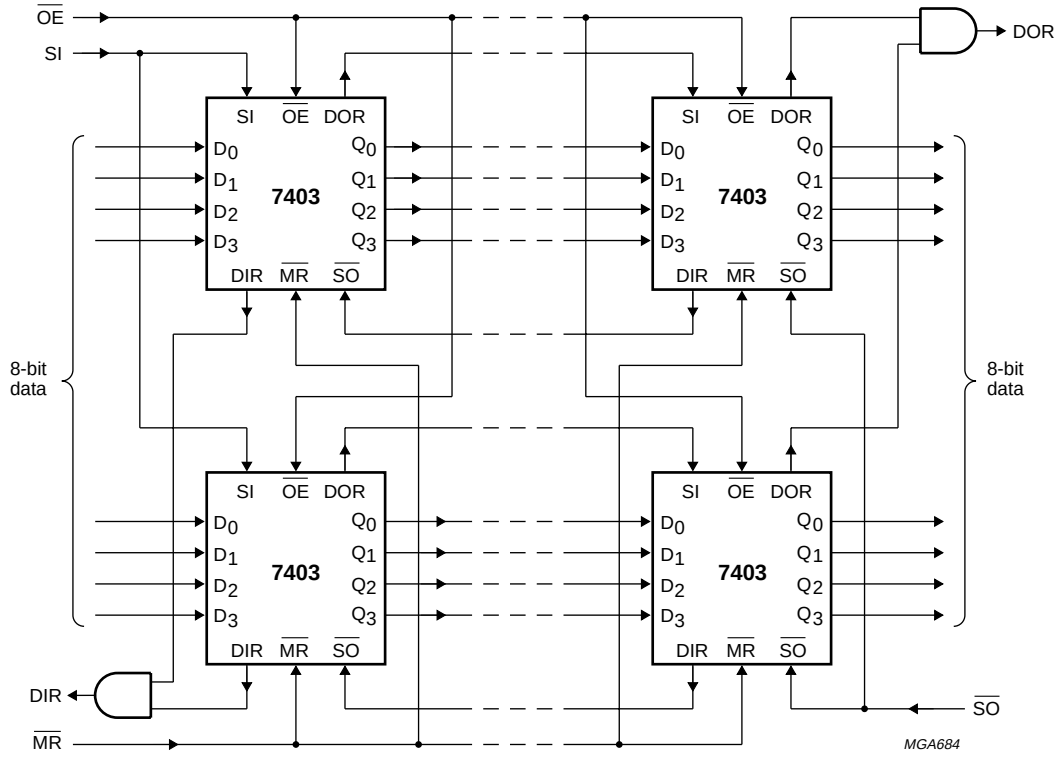


Fig.17 Expanded FIFO (parallel and serial) for increased word length; 8 bits wide x 64 n-bits.

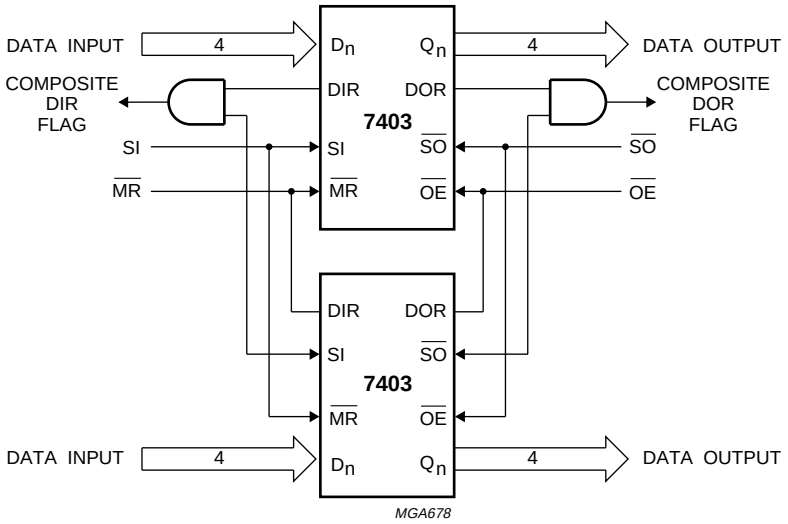


Fig.18 Expanded FIFO for increased word length; 64 words x 10 bits.

Note to Fig.18

The “7403” is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

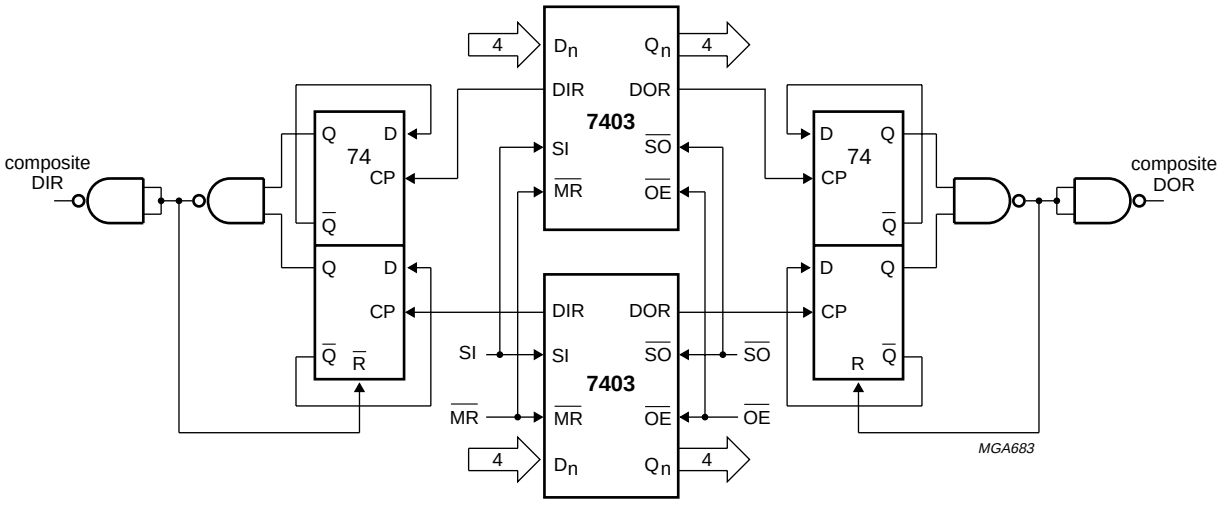


Fig.19 Expanded FIFO for increased word length.

Note to Fig.19

This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started or if $\overline{SO}$ output is constantly held HIGH, when the FIFO is full and the automatic shift-out cycles are started (see Figs 7 and 10).

Expanded format

Figure 20 shows two cascaded FIFOs providing a capacity of 128 words x 4 bits. Figure 21 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a ripple through delay, data arrives at the output of $FIFO_A$. Due to $\overline{SO}_A$ being HIGH, a DOR_A pulse is generated. The requirements of SI_B and D_{nB} are satisfied by the DOR_A pulse width and the timing between the rising edge of DOR_A and Q_{nA}. After a second ripple through delay, data arrives at the output of $FIFO_B$.

Figure 22 shows the signals on the nodes of both FIFOs after the application of a $\overline{SO}_B$ pulse, when both FIFOs are initially full. After a bubble-up delay a DIR_B pulse is generated, which acts as a $\overline{SO}_A$ pulse for $FIFO_A$. One word is transferred from the output of $FIFO_A$ to the input of $FIFO_B$. The requirements of the $\overline{SO}_A$ pulse for $FIFO_A$ is satisfied by the pulse width of DOR_B. After a second bubble-up delay an empty space arrives at D_{nA}, at which time DIR_A goes HIGH. Figure 23 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.

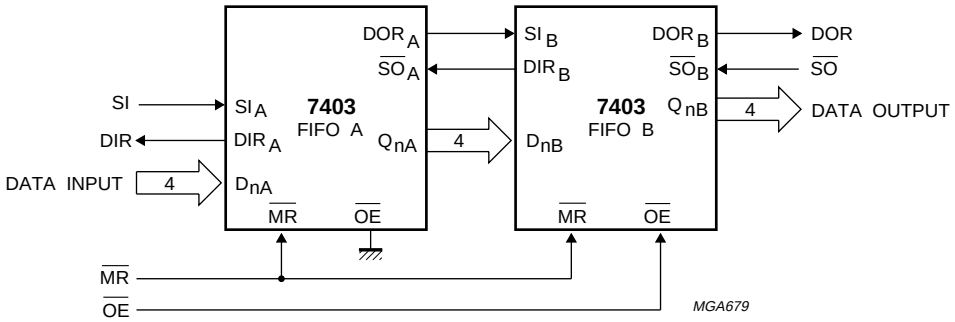


Fig.20 Cascading for increased word capacity; 128 words x 4 bits.

Note to Fig.20

The “7403” is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figures 21 and 22 demonstrate the intercommunication timing between $FIFO_A$ and $FIFO_B$. Figure 23 provides an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

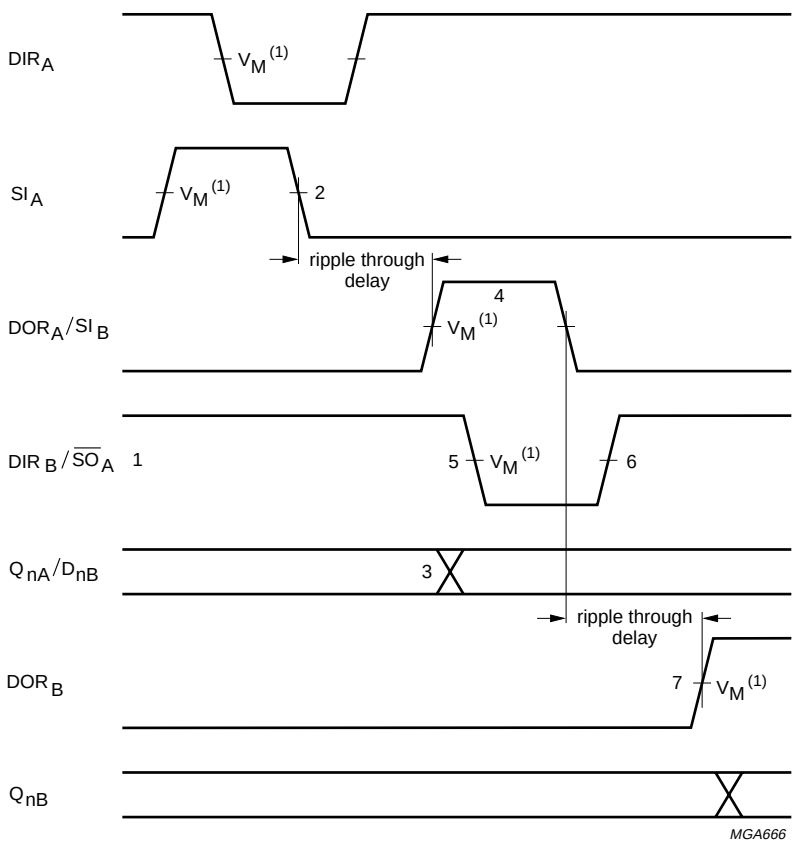


Fig.21 FIFO to FIFO communication; input timing under empty condition.

Notes to Fig.21

1. $FIFO_A$ and $FIFO_B$ initially empty, $\overline{SO}_A$ held HIGH in anticipation of data
2. Load one word into $FIFO_A$; SI pulse applied, results in DIR pulse
3. Data-out $_A$/data-in $_B$ transition; valid data arrives at $FIFO_A$ output stage after a specified delay of the DOR flag, meeting data input set-up requirements of $FIFO_B$
4. DOR_A and SI_B pulse HIGH; (ripple through delay after SI_A LOW) data is unloaded from $FIFO_A$ as a result of the data output ready pulse, data is shifted into $FIFO_B$
5. DIR_B and $\overline{SO}_A$ go LOW; flag indicates input stage of $FIFO_B$ is busy, shift-out of $FIFO_A$ is complete
6. DIR_B and $\overline{SO}_A$ go HIGH automatically; the input stage of $FIFO_B$ is again able to receive data, $\overline{SO}$ is held HIGH in anticipation of additional data
7. DOR_B goes HIGH; (ripple through delay after SI_B LOW) valid data is present one propagation delay later at the $FIFO_B$ output stage.

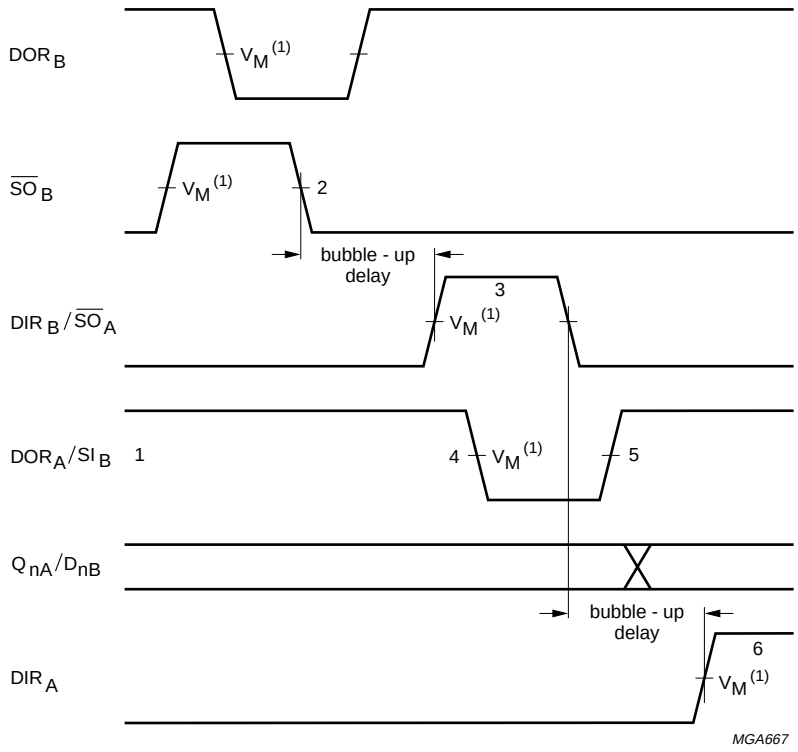


Fig.22 FIFO to FIFO communication; output timing under full condition.

Notes to Fig.22

1. $FIFO_A$ and $FIFO_B$ initially full, SI_B held HIGH in anticipation of shifting in new data as an empty location bubbles-up
2. Unload one word from $FIFO_B$; $\overline{SO}$ pulse applied, results in DOR pulse
3. DIR_B and $\overline{SO}_A$ pulse HIGH; (bubble-up delay after $\overline{SO}_B$ LOW) data is loaded into $FIFO_B$ as a result of the DIR pulse, data is shifted out of $FIFO_A$
4. DOR_A and SI_B go LOW; flag indicates the output stage of $FIFO_A$ is busy, shift-in to $FIFO_B$ is complete
5. DOR_A and SI_B go HIGH; flag indicates valid data is again available at $FIFO_A$ output stage, SI_B is held HIGH, awaiting bubble-up of empty location
6. DIR_A goes HIGH; (bubble-up delay after $\overline{SO}_A$ LOW) an empty location is present at input stage of $FIFO_A$.

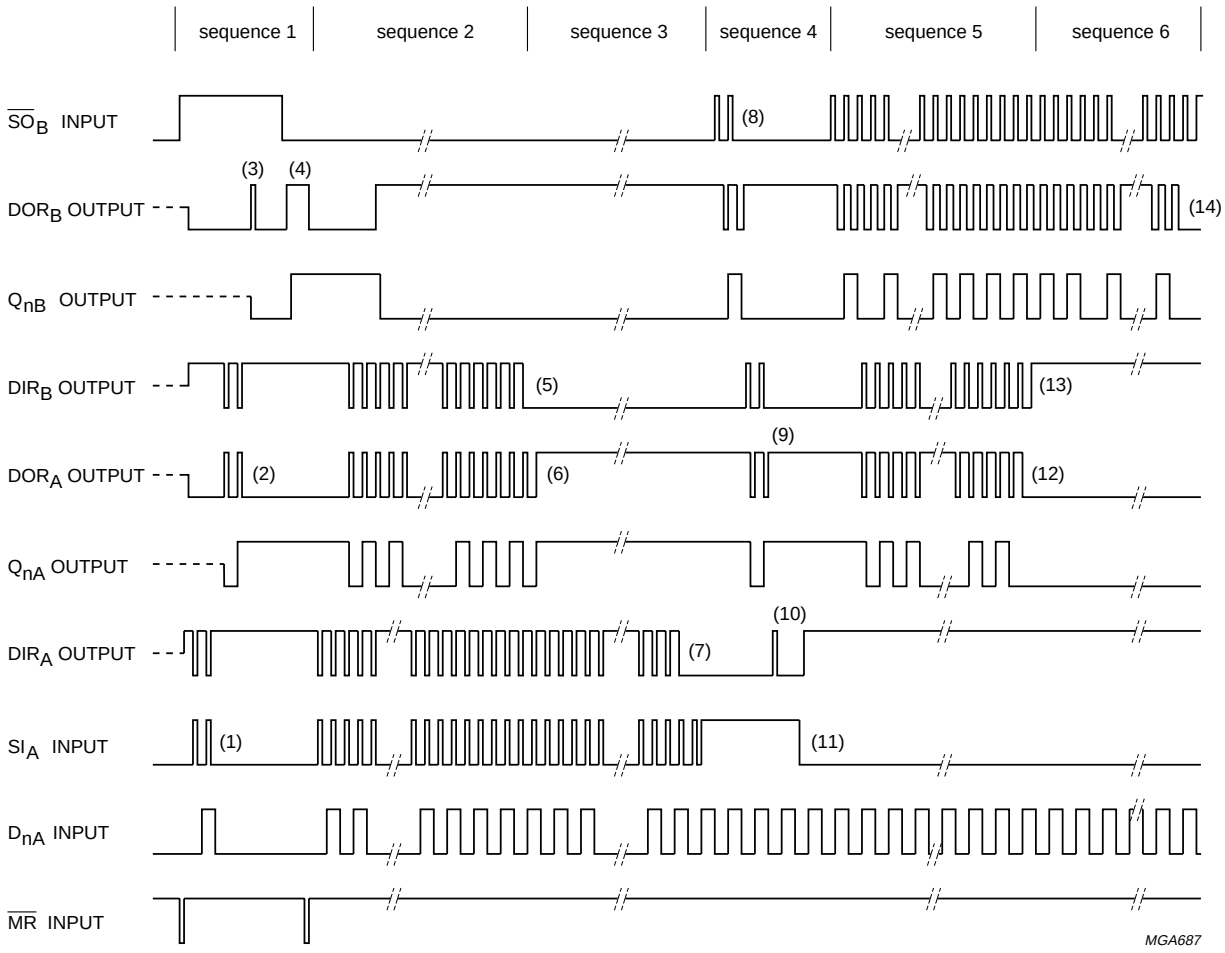


Fig.23 Waveforms showing the functionality and intercommunication between two FIFOs (refer to Fig.18).

Note to Fig.23

Sequence 1 (both FIFOS empty, starting SHIFT-IN process)

After a $\overline{MR}$ pulse has been applied FIFO$_A$ and FIFO$_B$ are empty. The DOR flags of FIFO$_A$ and FIFO$_B$ go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. $\overline{SO}_B$ is held HIGH and two SI$_A$ pulses are applied (1). These pulses allow two data words to ripple through to the output stage of FIFO$_A$ and to the input stage of FIFO$_B$ (2). When data arrives at the output of FIFO$_B$, a DOR$_B$ pulse is generated (3). When $\overline{SO}_B$ goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR$_B$ goes HIGH (4).

Sequence 2 ($FIFO_B$ runs full)

After the $\overline{MR}$ pulse, a series of 64 SI pulses are applied. When 64 words are shifted in, DIR_B remains LOW due to $FIFO_B$ being full (5). DOR_A goes LOW due to $FIFO_A$ being empty.

Sequence 3 ($FIFO_A$ runs full)

When 65 words are shifted in, DOR_A remains HIGH due to valid data remaining at the output of $FIFO_A$. Q_{nA} remains HIGH, being the polarity of the 65th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Sequence 4 (both FIFOs full, starting SHIFT-OUT process)

SI_A is held HIGH and two $\overline{SO}_B$ pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of $FIFO_B$, and proceed to $FIFO_A$ (9). When the first empty location arrives at the input of $FIFO_A$, a DIR_A pulse is generated (10) and a new word is shifted into $FIFO_A$. SI_A is made LOW and now the second empty location reaches the input stage of $FIFO_A$, after which DIR_A remains HIGH (11).

Sequence 5 ($FIFO_A$ runs empty)

At the start of sequence 5 $FIFO_A$ contains 63 valid words due to two words being shifted out and one word being shifted in, in sequence 4. An additional series of $\overline{SO}_B$ pulses are applied. After 63 $\overline{SO}_B$ pulses, all words from $FIFO_A$ are shifted into $FIFO_B$. DOR_A remains LOW (12).

Sequence 6 ($FIFO_B$ runs empty)

After the next $\overline{SO}_B$ pulse, DIR_B remains HIGH due to the input stage of $FIFO_B$ being empty. After another 63 $\overline{SO}_B$ pulses, DOR_B remains LOW due to both FIFOs being empty (14). Additional $\overline{SO}_B$ pulses have no effect. The last word remains available at the output Q_n.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.