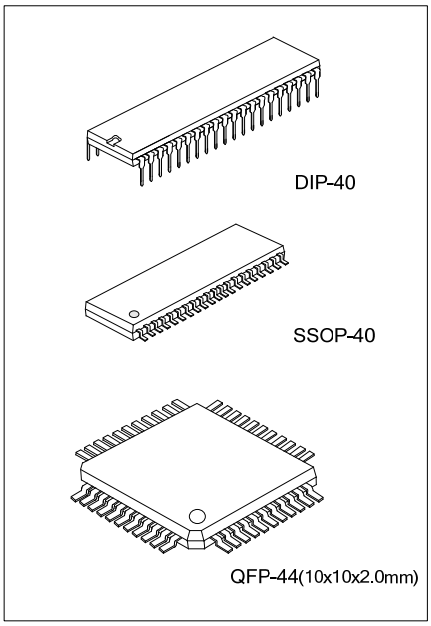
3½ DIGIT, LCD DISPLAY, A/D CONVERTERS



■ DESCRIPTION

The UTC **7106** is a high performance, low power,3½ digits A/D converter. Included are seven segment decoders, display drivers, a reference, and a clock.

The UTC **7106** is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive.

The UTC **7106** bring together a combination of high accuracy, versatility, and true economy. It features auto zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA (Max), and rollover error of less than one count. True differential inputs and reference are useful in all system, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge type transducers. Finally, the true economy of single power supply operation, enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

■ FEATURES

*Guaranteed Zero Reading for 0V Input On All Scales
*True Polarity At Zero for Precise Null Detection
*1pA Typical Input Current
*True Differential Input And Reference, Direct Drive LCD Display
*Low Noise-Less than 15μVp-p
*On chip Clock and Reference
*Low Power Dissipation-Typically Less than 10mW
*No Additional Active Circuits Required
*Enhanced Display Stability

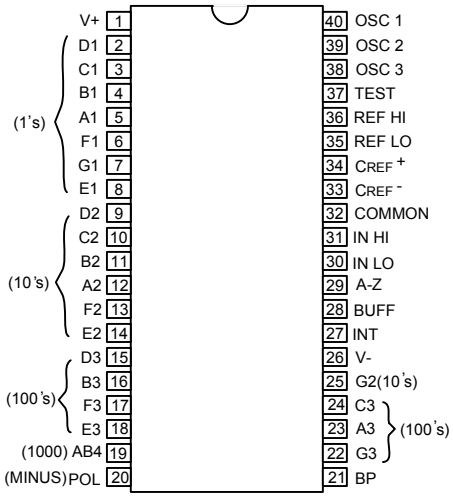
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
7106L-D40-T	7106G-D40-T	DIP-40	Tube
7106L-R40-R	7106G-R40-R	SSOP-40	Tape Reel
7106L-R40-T	7106G-R40-T	SSOP-40	Tube
7106L-QM1-Y	7106G-QM1-Y	QFP-44	Tray

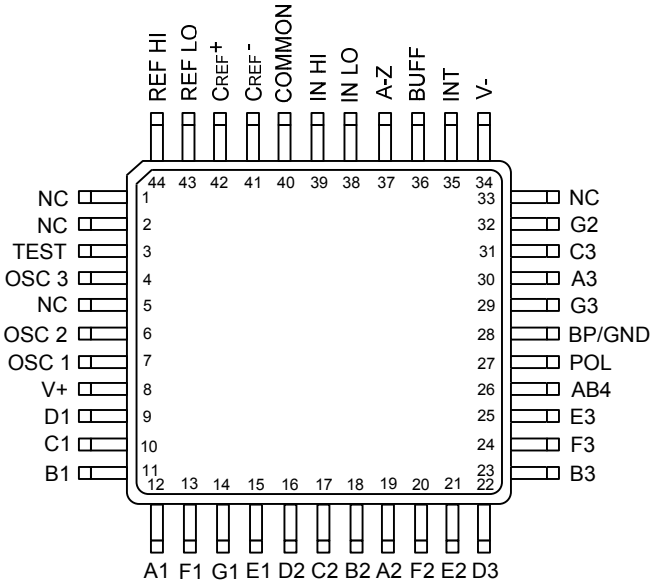
7106L-D40-T (1)Packing Type (2)Package Type (3)Lead Free	(1) T: Tube, R: Tape Reel, Y: Tray (2) D40: DIP-40, R40: SSOP-40, QM1: QFP-44 (3) G: Halogen Free, L: Lead Free

■ PIN CONFIGURATION

DIP- 40/SSOP-40



MQFP - 44



■ ABSOLUTE MAXIMUM RATINGS(T_A=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (V+ ~ V-)	V_{DD}	15	V
Analog Input Voltage (Either Input) (Note 1)	$V_{I,ANG}$	V+ ~ V-	V
Reference Input Voltage (Either Input)	$V_{I,REF}$	V+ ~ V-	V
Junction Temperature	T_J	150	°C
Operating Temperature	T_{OPR}	0 ~ +70	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: 1. Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-40	θ_{JA}	50	°C/W
	SSOP-40		70	
	QFP-44		75	

■ ELECTRICAL CHARACTERISTICS (T_A=25℃, f_{CLOCK}=48kHz, measured by the circuit of Fig.1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE						
Zero Input Reading	R_Z	V_{IN}=0.0V, Full Scale=200mV	-000.0	±000.0	+000.0	Digital Reading
Ratio metric Reading	R_R	V_{IN}=V_{REF}, V_{REF}=100mV	999	999/1000	1000	Digital Reading
Rollover Error	E_R	-V_{IN}=+V_{IN}≒200mV Difference in Reading for Equal Positive and Negative Inputs Near Full Scale		±0.2	±1	Counts
Linearity	L	Full Scale=200mV or Full Scale=2V Maximum Deviation from Best Straight Line Fit (Note 2)		±0.2	±1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM}=1V,V_{IN}=0V, Full Scale=200mV(Note 2)		50		μV/V
Noise	V_N	V_{IN}=0V,Full Scale=200mV (Peak-To-Peak Value Not Exceeded 95% of Time)		15		μV
Leakage Current Input	IL	V_{IN}=0(Note 2)		1	10	pA
Zero Reading Drift	D_{ZR}	V_{IN}=0, 0℃ ~ 70℃ (Note 2)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	$\Phi_{T,S}$	V_{IN}=199mV, 0℃ ~ 70℃, (Ext.Ref.0ppm/℃) (Note 2)		1	5	ppm/°C
End Power Supply Character V+ Supply Current	I_{EP}	V_{IN}=0		1.0	1.8	mA
COMMON Pin Analog Common Voltage	V_{COM}	25kΩ Between Common and Positive Supply (With Respect to +Supply)	2.7	3.05	3.3	V
Temperature Coefficient of Analog Common	$\Phi_{T,A}$	25kΩ Between Common and Positive Supply (With Respect to +Supply)		80		ppm/°C

■ ELECTRICAL CHARACTERISTICS(Cont.)

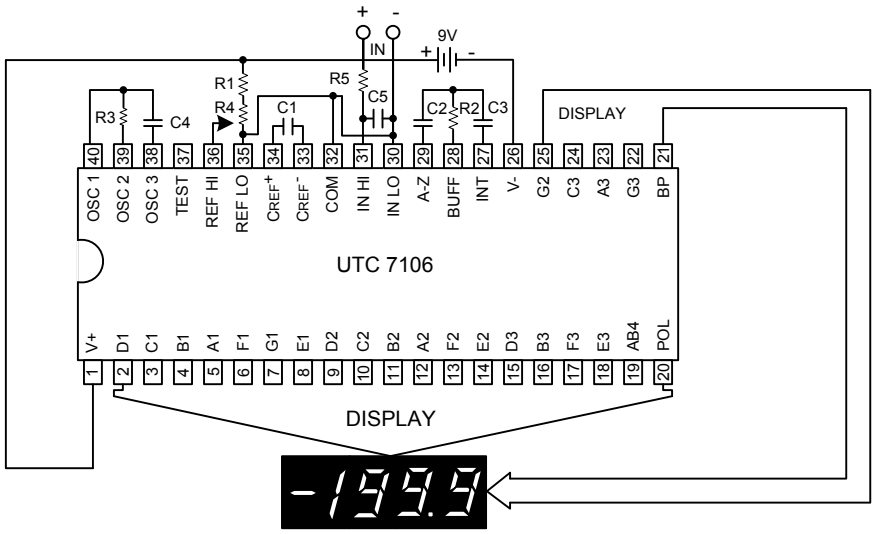
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DISPLAY DRIVER						
Peak-to-Peak Segment Drive Voltage Peak-to-Peak Backplane Drive Voltage	$V_{D,PP}$	V+ ~ V-=9V(Note 1)	4	5.5	6	V

Note: 1. Back plane drive is in phase with segment drive for"off"segment,180 degrees out of phase for "on" segment . Frequency is 20 times conversion rate. Average DC component is less than 50mV.

2. Not tested, guaranteed by design.

■ TYPICAL APPLICATIONS AND TEST CIRCUIT

(LCD DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE)



C1=0.1 μF
C2=0.47 μF
C3=0.22 μF
C4=100pF
C5=0.02 μF
R1=24kΩ
R2=47kΩ
R3=91kΩR
4=1kΩ
R5=1MΩ

■ DESIGN INFORMATION SUMMARY SHEET

*OSCILLATOR FREQUENCY
fosc=0.45/RC
C_{OSC}>50pF, R_{OSC}>50kΩ
f_{OSC} (Typ)=48kHz

*OSCILLATOR PERIOD
t_{OSC}=RC/0.45
*INTEGRATION CLOCK FREQUENCY
$f_{CLOCK}=f_{OSC}/4$

*INTEGRATION PERIOD
$t_{INT}=1000\times(4/f_{OSC})$

*60/50Hz REJECTION CRITERION
t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz}=Integer

*OPTIMUM INTEGRATION CURRENT
I_{INT}=4μA

*FULL SCALE ANALOG INPUT VOLTAGE
V_{INFS} (Typ)=200mV or 2V

*INTEGRATE ESISTOR
$R_{INT}= V_{INFS}/ I_{INT}$

*INTEGRATE CAPACITOR
$C_{INT}=(t_{INT})(I_{INT})/ V_{INT}$

*INTEGRATOR OUTPUT VOLTAGE SWING
$V_{INT}=(t_{INT})(I_{INT})/ C_{INT}$

*V_{INT} MAXIMUM SWING
(V- + 0.5V)<V_{INT}<(V+ - 0.5V), V_{INT} (Typ)=2V

*DISPLAY COUNT
$COUNT=1000\times V_{IN}/V_{REF}$

*CONVERSION CYCLE
$t_{CYC}=t_{CLOCK}\times4000$
$t_{CYC}=t_{OSC}\times16,000$
When f_{OSC}=48kHz, t_{CYC}=333ms

*COMMON MODE INPUT VOLTAGE
(V- + 1V)<V_{IN}<(V+ - 0.5V)

*AUTO-ZERO CAPACITOR
0.01μF<C_{AZ}<1μF

*REFERENCE CAPACITOR
0.1μF<C_{REF}<1μF

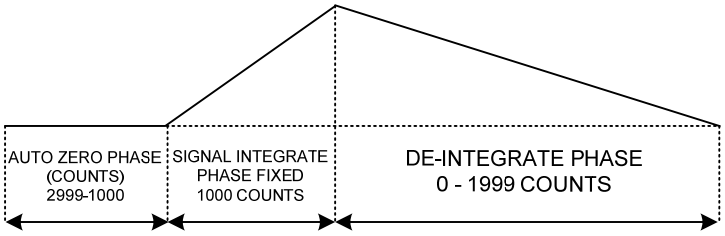
*V_{COM}
Biased between Vi and V-

*$V_{COM}\fallingdotseq$V+ - 2.8V
Regulation lost when V+ to V- <$\fallingdotseq$6.8V
If V_{COM} is externally pulled down to (V+ to V-)/2, the V_{COM} circuit will turn off.

*POWER SUPPLY: SINGLE 9V
V+ - V- =9V
$V_{GND}\fallingdotseq$V+ - 4.5V
Digital supply is generated by internal parts.

*DISPLAY: LCD
Type: Direct drive with digital logic supply amplitude.

■ TYPICAL INTEGRATOR AMPLIFIER OUTPUT WAVEFORM (INT PIN)



TOTAL CONVERSION TIME=4000 × t_{CLOCK}=16,000 × tosc

■ DETAILED DESCRIPTION

ANALOG SECTION

Fig.1 shows the Analog Section for the UTC **7106**. Each measurement cycle is divided into three phases. They are(1) auto-zero(A-Z), (2)signal integrate (INT)and (3)de-integrate(DE).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. if, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

DE-INTEGRATE PHASE

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

DISPLAY COUNT=1000(V_{IN}/ V_{REF}).

DIFFERENTIAL INPUT

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

■ DETAILED DESCRIPTION(Cont.)

DIFFERENTIAL REFERENCE

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection)

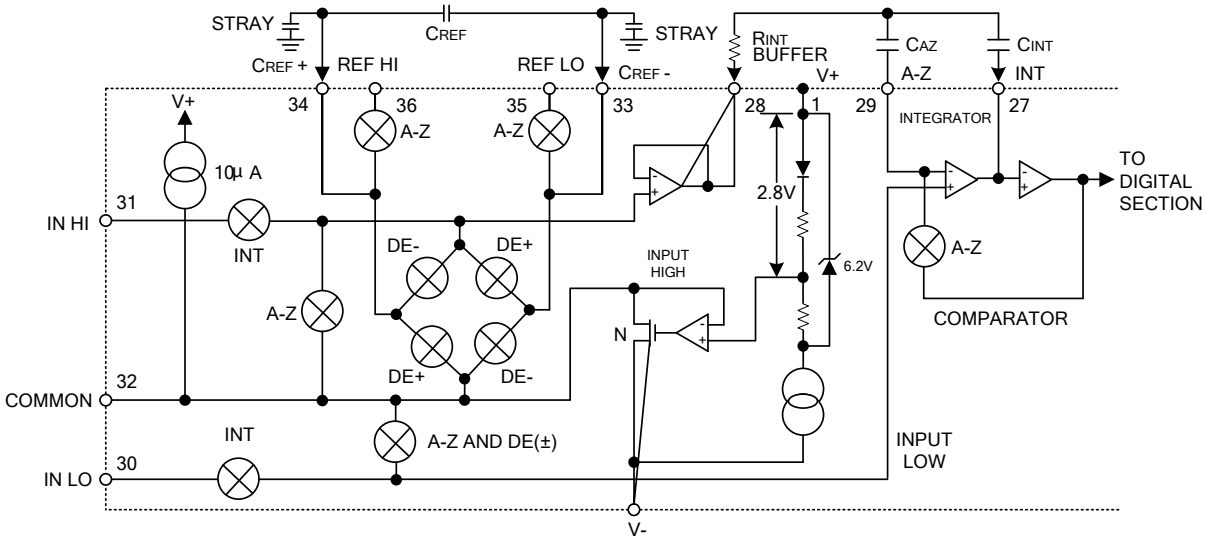


Fig.1 Analog Section

■ DETAILED DESCRIPTION(Cont.)

ANALOG COMMON

This pin is included primarily to set the common mode voltage for battery operation (UTC **7106**) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate(>7V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance (≒15Ω), and a temperature coefficient typically less than 80ppm/℃.

The UTC **7106**, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig.2

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage(power supply common for instance).In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N-Channel FET that can sink approximately 30mA of current to hold the voltage 2.8V below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

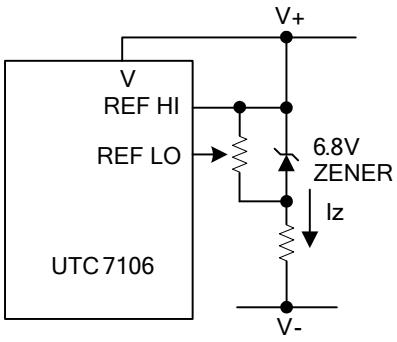


FIGURE 2A.

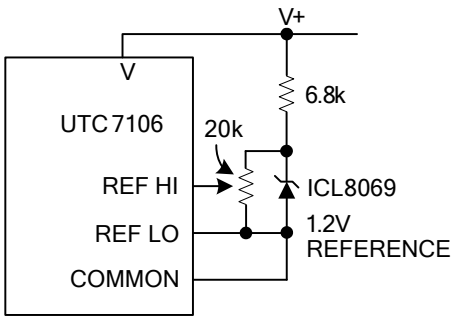


FIGURE 2B.

Fig.2 Using an External Reference

■ DETAILED DESCRIPTION(Cont.)

TEST

The TEST pin serves two function. On the UTC **7106** it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Fig.3 and 4 show such an application. No more than a 1mA load should be applied.

The second function is a “lamp test”. When TEST is pulled high (to V+) all segments will be turned on and the display should read ”1888”. The TEST pin will sink about 15mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant DC voltage (no square-wave) . This may burn the LCD display if maintained for extended periods.

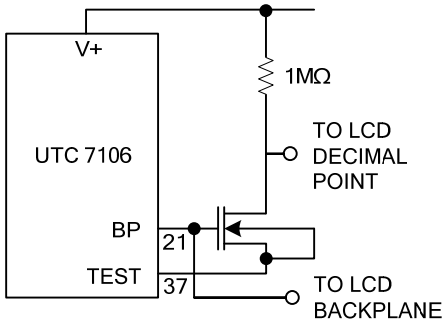


Fig.3 Simple Inverter for Fixed Decimal Point

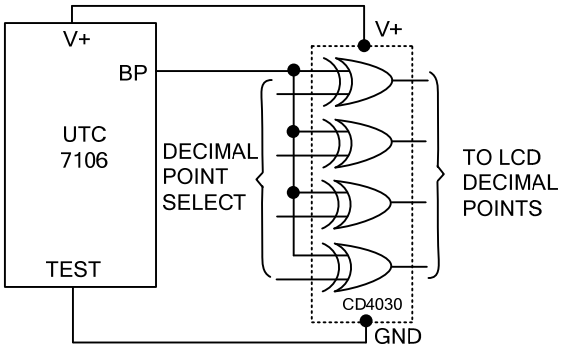


Fig.4 Exclusive "OR" Gate For Decimal Point Drive

■ DETAILED DESCRIPTION(Cont.)

DIGITAL SECTION

Fig.5 show the digital section for the UTC **7106**, respectively. In the UTC **7106**, an internal digital ground is generated from a 6V Zener diode and a large P-Channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane(BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/sec, this is a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

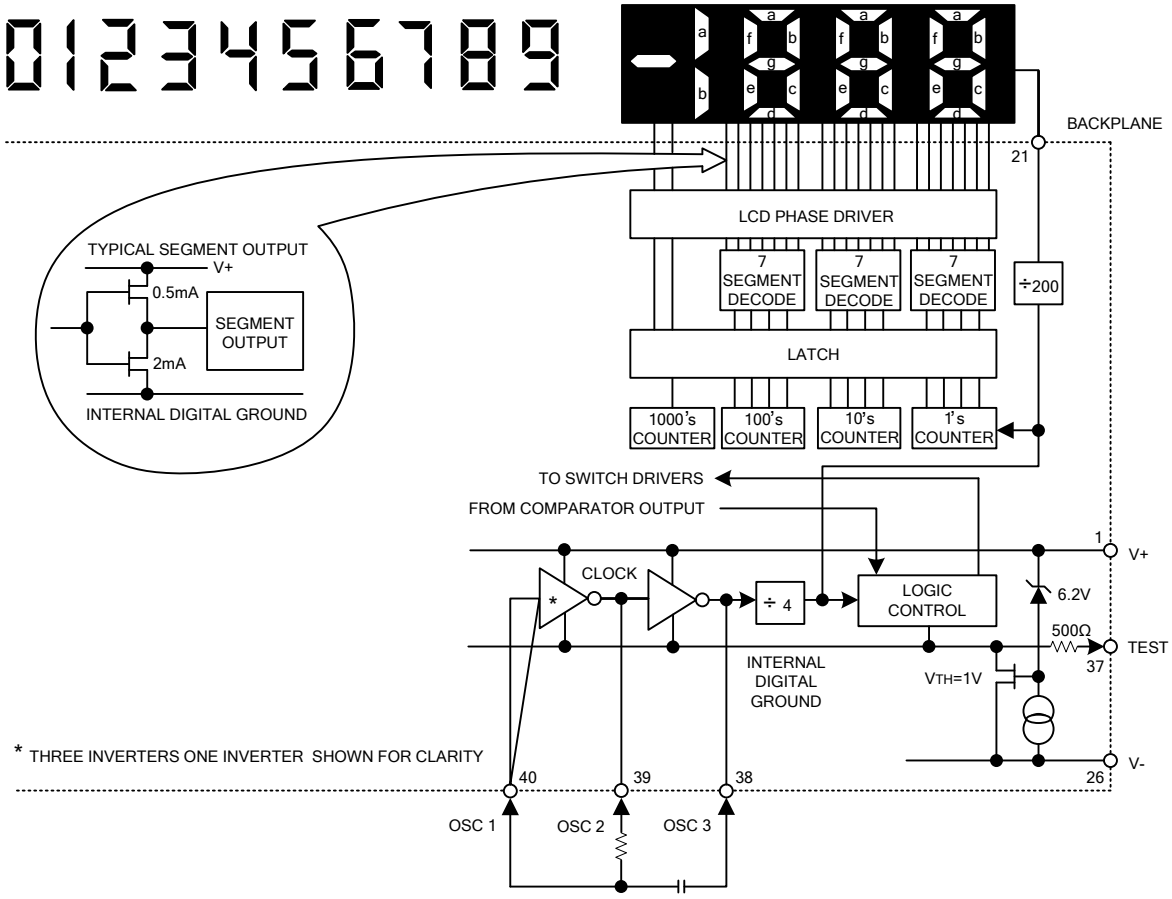


Fig.5 Digital Section

■ DETAILED DESCRIPTION(Cont.)

SYSTEM TIMING

Fig.6 shows the clocking arrangement used in the UTC **7106**. Two basic clocking arrangements can be used:

1. Fig.6A. An external oscillator connected to pin 40.
2. Fig.6B. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero(1000 ~ 3000 counts). For signals less than full scale. auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

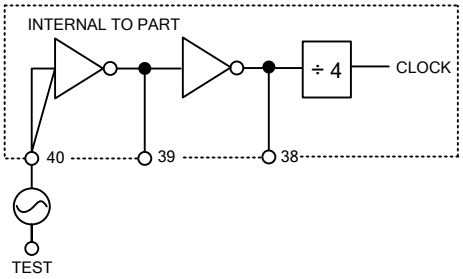


FIGURE 6A

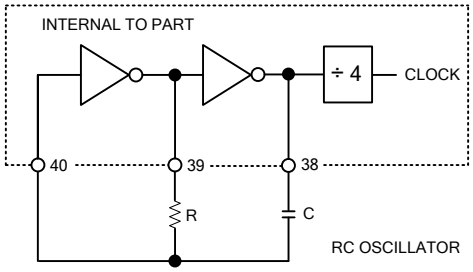


FIGURE 6B

Fig.6 Clock Circuits

COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 4μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing(approximately. 0.3V from either supply).In the UTC **7106**, when the analog COMMON is used as a reference, a nominaul+2V full scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47μF capacitor is recommended. On the 2V scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

■ DETAILED DESCRIPTION(Cont.)

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e., the REF LO pin is not at analog COMMON)and a 200mV scale is used, a larger value is required to prevent roll-ovre error. Generally 1μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

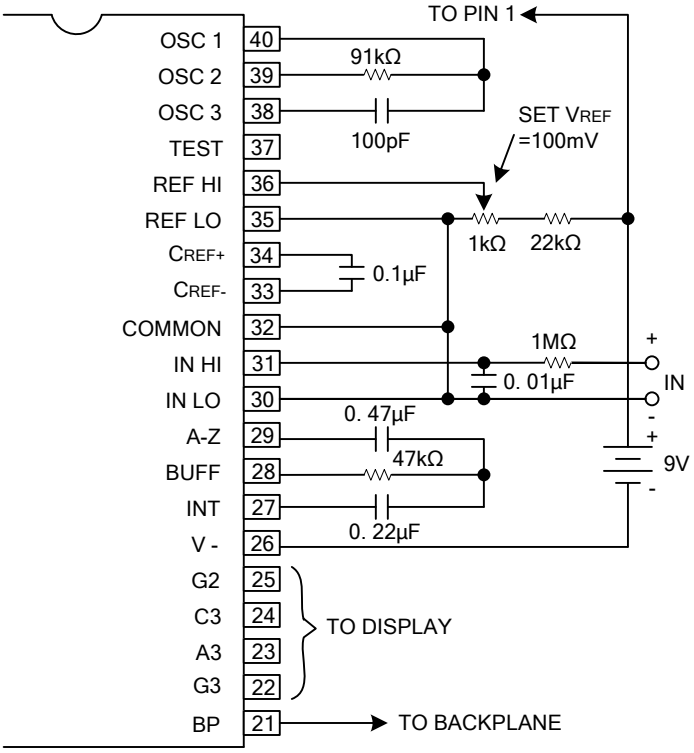
For all ranges of frequency a 91kΩ resistor is recommended and the capacitor is selected from the equation: f= 0.45/RC for 48kHz Clock (3 Readings/sec), C=100pF.

Reference Voltage

The analog input required to generate full scale output (2000 counts) is: $V_{IN}=2V_{REF}$.Thus, for the 200mV and 2V scale, V_{REF} should equal 100mV and 1V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.662V. Instead of dividing the input down to 200mV, the designer should use the input voltage directly and select V_{REF}=0.341V. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input.

■ TYPICAL APPLICATIONS

The UTC **7106** may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.



Values shown are for 200mV full scale,3 readings/sec.,floating supply voltage(9V battery).

Fig.7 Using The Internal Reference

■ TYPICAL APPLICATIONS(Cont.)

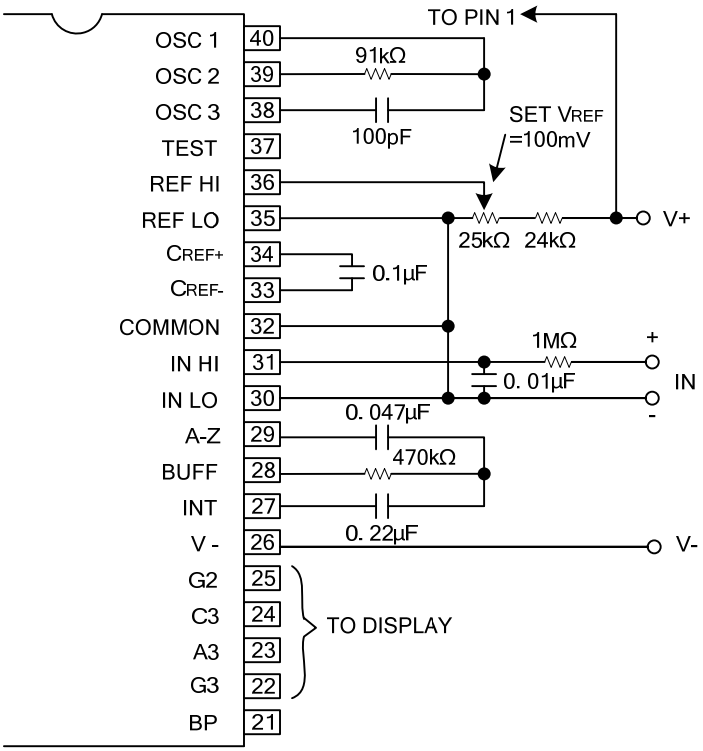
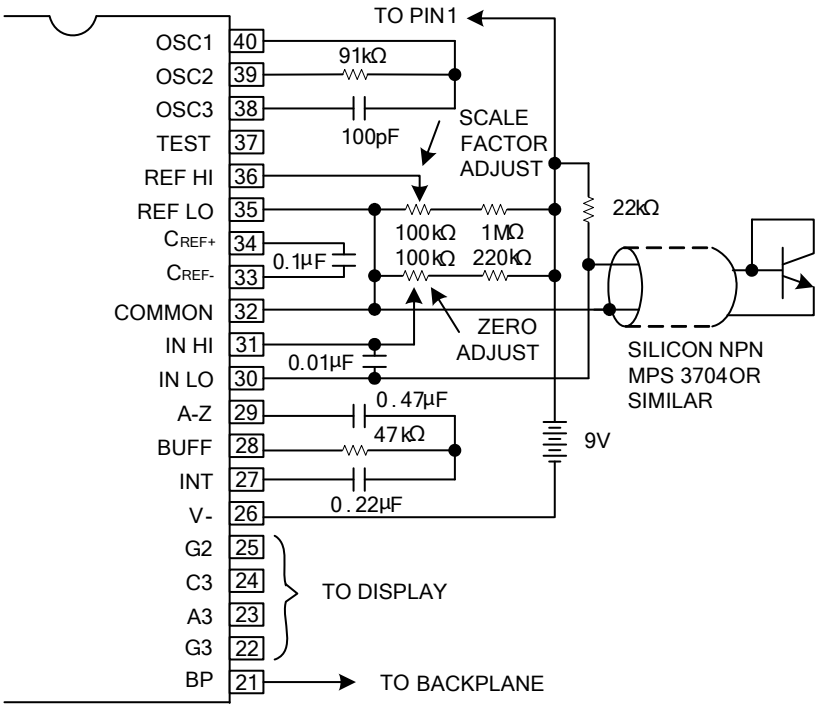


Fig.8 Recommended Component Values For 2V Full Scale

■ TYPICAL APPLICATIONS(Cont.)



A sillicon diode-connected transistor has a temperature coefficient of about -2 mV/℃. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading

Fig.9 Used as A Digital Centigrade Thermometer

■ TYPICAL APPLICATIONS(Cont.)

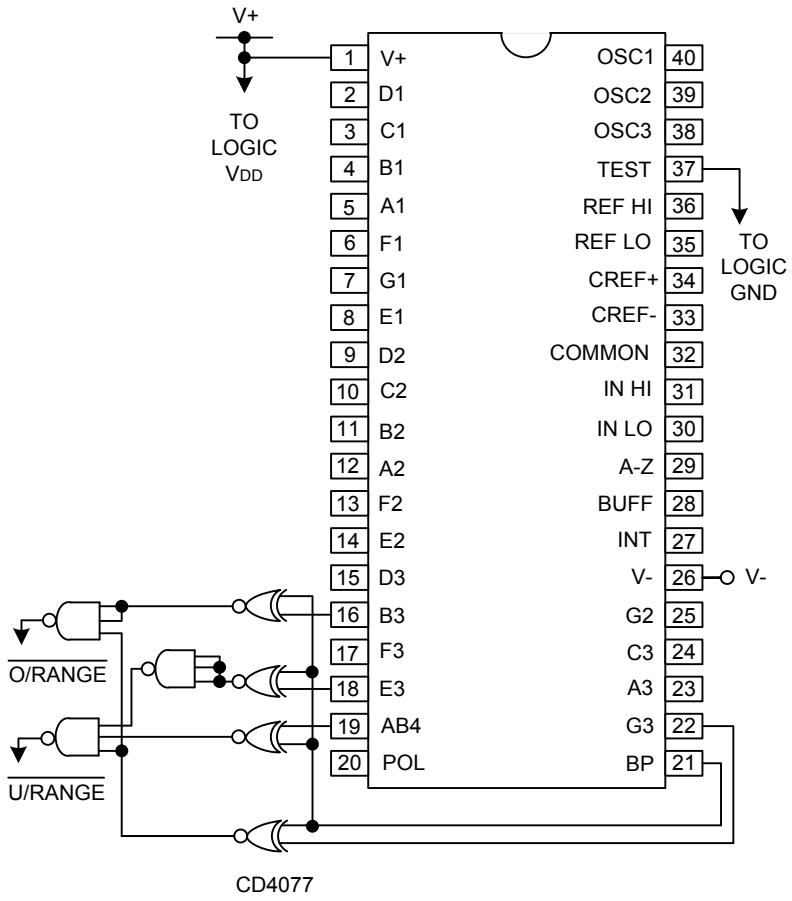
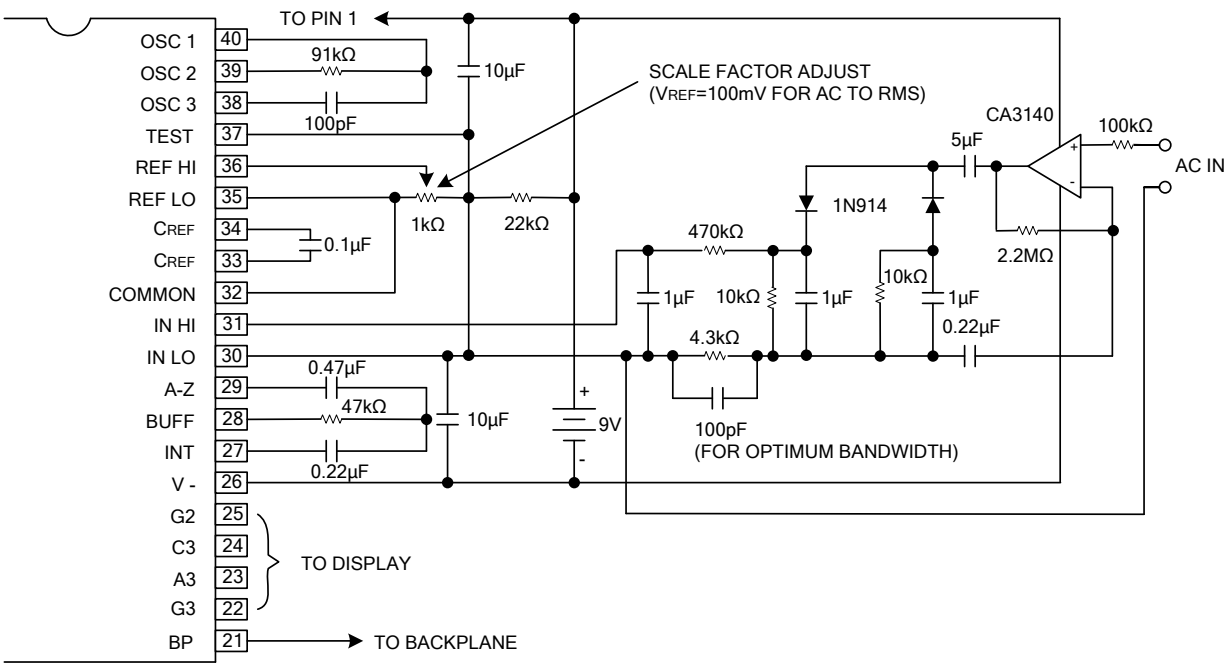


Fig.10 Circuit for Developing Underrange and Overrange from UTC 7106 Outputs

■ TYPICAL APPLICATIONS(Cont.)



Test is used as a common-mode reference level to ensure compatiblity with most op amps.

Fig. 11 AC to DC Converter with UTC 7106