commodore semiconductor group

CMOS

MPS

65C23

TRI-PORT INTERFACE

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CONCEPT . . .

The 65C23 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. It has three dedicated 8-bit I/O ports which provide 24 individually programmable I/O lines.

FEATURES:

- 24 individually programmable I/O lines
- Completely static operation
- Two TTL Drive Capability
- 6 directly addressable registers
- 1 MHz operation

65C23 Addressing

65C23 REGISTERS (Direct Addressing)

*000	R0	PRA — Port Register A
001	R1	PRB — Port Register B
010	R2	PRC — Port Register C
011	R3	DDRA — Data Direction Register A
100	R4	DDRB — Data Direction Register B
101	R5	DDRC — Data Direction Register C
110	}	Illegal States
111	}	Illegal States

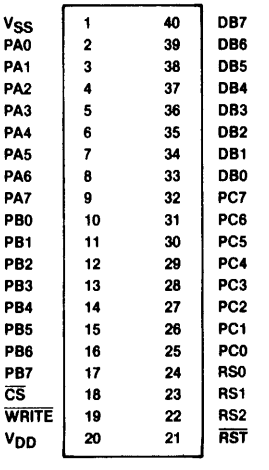
*NOTE: RS2, RS1, RS0 respectively

ORDER NUMBER:

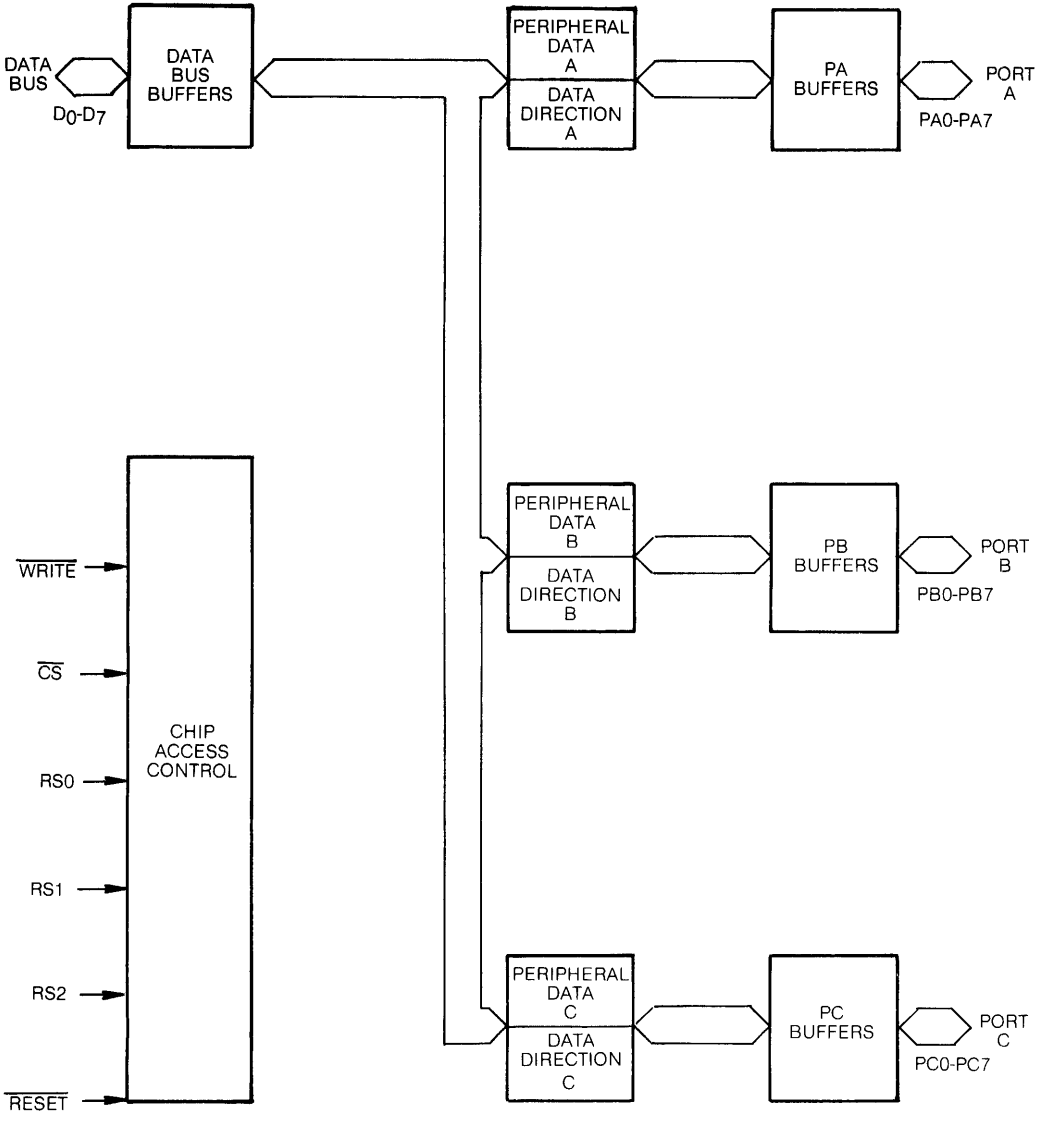
MXS 65C23

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

65C23 PIN CONFIGURATION



65C23 INTERNAL ARCHITECTURE



MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{CC}	−0.3 to +7.0	V_{dc}
INPUT VOLTAGE	V_{in}	−0.3 to +7.0	V_{dc}
OPERATING TEMPERATURE RANGE	T_A	0 to +70	°C
STORAGE TEMPERATURE RANGE	T_{stg}	−55 to +150	°C

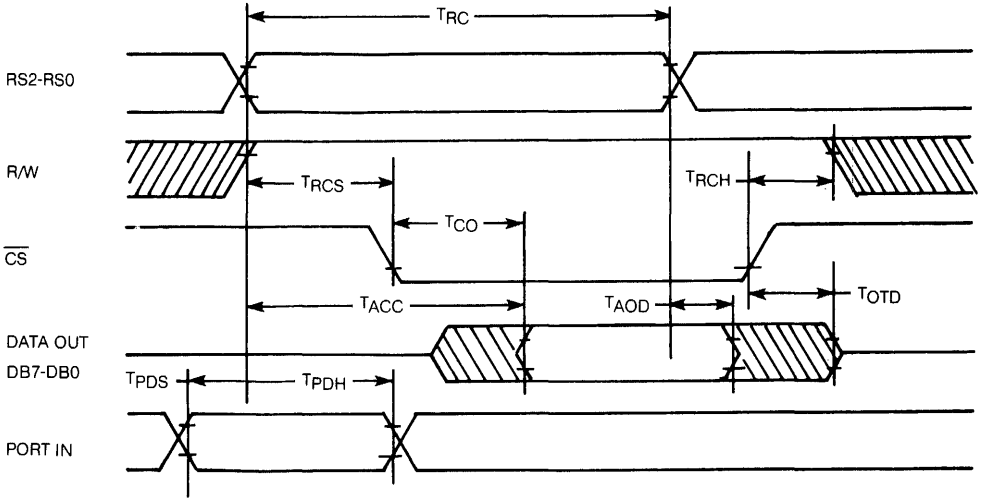
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0V, T_A = 0° to 70°C)

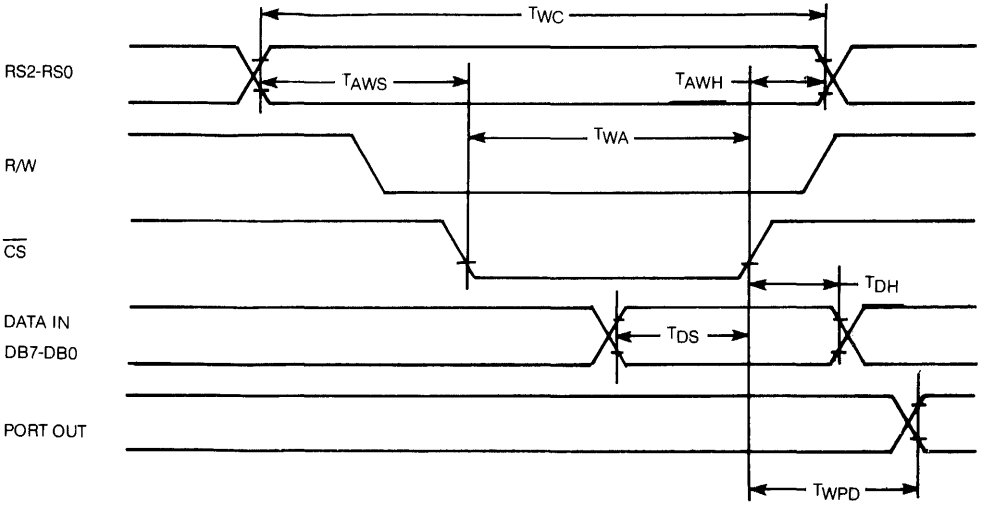
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	—	+.8	Vdc
Input Leakage Current V_{in} = 0 to 5.0 Vdc $\overline{WRITE}$ $\overline{RST}$, $\overline{CS}$, RS_0-RS_2	I_{IN}	0	±1.0	±2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) D0-D7, PA0-PA7, PB0-PB7, PC0-PC7	I_{TSI}	0	±2.0	±10	μAdc
Output High Voltage (V_{CC} = min, Load = 200 μAdc)	V_{OH}	2.4	3.5	V_{CC}	Vdc
Output Low Voltage (V_{CC} = min, Load = 3.2 mAdc)	V_{OL}	V_{SS}	0.2	+0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 Vdc)	I_{OH}	−200	−1000	—	μAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	3.2	—	—	mAdc
Supply Current	I_{CC}	—		10	mA
Input Capacitance (V_{in} = 0V, T_A = 25°C, f = 1.0 MHz) D0-D7, PA0-PA7, PB0-PB7, PC0-PC7 $\overline{WRITE}$ $\overline{RST}$, RS_0-RS_2, $\overline{CS}$	C_{in}	—	7	10	pF
Output Capacitance (V_{in} − 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	—	7	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

READ CYCLE



WRITE CYCLE



Note: All timings referenced to V_{IL}max, V_{IH} min on inputs and V_{OL} max, V_{OH} min on outputs.

READ CYCLE

Symbol	Parameter	MIN	MAX	UNITS
T_{RC}	Read Cycle	450	—	nS
T_{ACC}	Access Time[1]	—	450	nS
T_{CO}	$\overline{CS}$ to Output Valid	—	270	nS
T_{RCS}	R/W high to $\overline{CS}$ Setup	0	—	nS
T_{RCH}	R/W high to $\overline{CS}$ Hold	0	—	nS
T_{OTD}	$\overline{CS}$ to Output Off Delay	20	120	nS
T_{AOD}	Address to Output Delay	50	—	nS
T_{PDS}	Port Input Setup	120	—	nS
T_{PDH}	Port Input Hold	150	—	nS

Note 1: Access Time measured from later of $\overline{WRITE}$ high or RS stable.

WRITE CYCLE

Symbol	Parameter	MIN	MAX	UNITS
T_{WC}	Write Cycle	450	—	nS
T_{WA}	Write Active Time[2]	420	—	nS
T_{AWS}	Address to R/W low Setup	0	—	nS
T_{AWH}	Address to R/W low Hold	0	—	nS
T_{DS}	Data bus in Setup	150	—	nS
T_{DH}	Data bus in Hold	0	—	nS
T_{WPD}	Write active to Port out Delay	—	1000	nS

Note 2: T_{WA} is the time while both $\overline{CS}$ and R/W are low.