RS data

Universal asynchronous receiver transmitter 6402 and 6402-1

Stock numbers 309-284 and 304-144

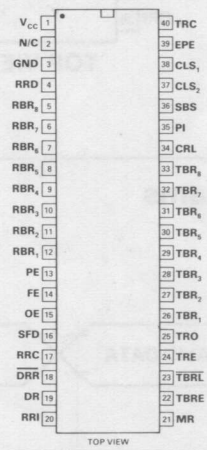
The RS Universal asynchronous receiver transmitters, UARTS are designed for interfacing an asynchronous serial data channel and a parallel data channel. The devices can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems.

The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. The receiver converts serial start, data parity and stop bits to parallel data verifying proper code transmission, parity and stop bits. Utilising CMOS – LSI technology the devices operate at low power levels and can be clocked at frequencies up to 1 MHz (6402) or 2 MHz (6402-1). Several status output flags are provided thereby increasing flexibility and simplifying the user interface.

Features

- Two speed options up to 1 MHz 6402 or 2 MHz 6402-1
- Low power – less than 10 mW at 2 MHz
- Programmable word length, stop bits and parity
- Automatic data formatting and status generation
- CMOS and LS TTL compatible.

PIN CONNECTIONS



Absolute maximum ratings

Operating temperature range ——— −40°C to +85°C
Storage temperature ——— −65°C to +150°C
Supply voltage ——— +7.0 V d.c.
Voltage on any input or output pin ——— −0.3 V to V_{CC}+0.3 V

d.c. characteristics

Test conditions: V_{CC} = 5 V d.c. ±5%, T_{amb} = 25°C 6402-1 characteristics in ( ) where different.

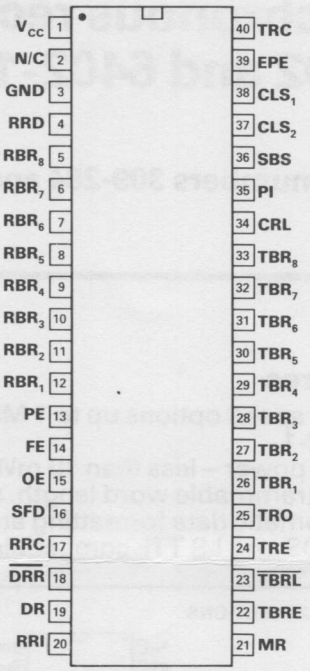
Parameter	Condition	Min.	Typ.	Max.	Unit
Input voltage High V_{IH}		V_{CC} − 2.0			V
Input voltage Low V_{IL}				0.8	V
Input leakage I_{IL}	$G_{nd} \leq V_{IN} \leq V_{CC}$	−5.0 (−1)		5.0 (1)	μA
Output voltage High V_{OH}	I_{OH} = −0.2 mA	2.4			V
Output voltage Low V_{OL}	I_{OL} = 1.6 mA			0.45	V
Output leakage I_{OL}	$G_{nd} \leq V_{OUT} \leq V_{CC}$	−5.0 (−1)		5.0 (1)	μA
Power supply current I_{CC}	$V_{IN} = G_{nd}$ or V_{CC}		1.0	800 (100)	μA
Input capacitance C_{IN}			7.0	8.0	pF
Output capacitance C_O			8.0	10.0	pF

a.c. characteristics

Test conditions : V_{CC} = 5 V d.c. ±5%, T_{amb} = 25°C 6402-1 characteristics in ( ) where different.

Parameter	Condition	Min.	Typ.	Max.	Unit
Clock frequency f_c		d.c.		1.0 (2.0)	MHz
Power supply current I_{CC}	f_c = 500 kHz			1.2 (1.9)	mA
Pulse widths t_{pw}	see timing diagrams	225 (150)	50		ns
Pulse width t_{MR}	see timing diagrams	600 (400)	200		ns
Input data setup time t_{DS}	see timing diagrams	75 (50)	20		ns
Input data hold time t_{DH}	see timing diagrams	90 (60)	40		ns
Output enable time t_{EN}	see timing diagrams		80	190 (160)	ns

Pin connections



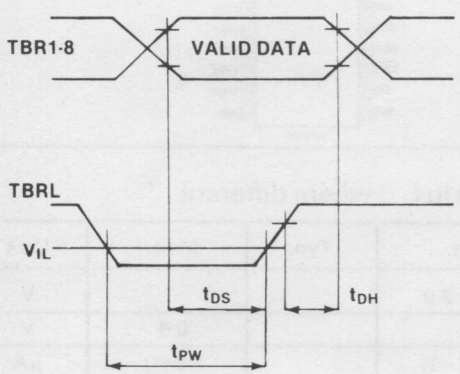
TOP VIEW

Pin definition

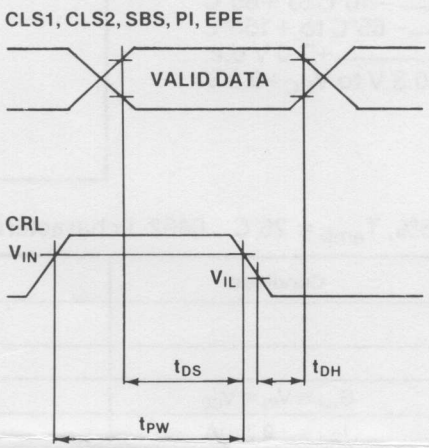
V_{CC}	+V supply
N/C	No Connection
GND	GROUND
RRD	RECEIVER REGISTER DISABLE
$RBR_{1.8}$	RECEIVER BUFFER REGISTER OUTPUTS
PE	PARITY ERROR
FE	FRAMING ERROR
OE	OVERRUN ERROR
SFD	STATUS FLAGS DISABLE
RRC	RECEIVER REGISTER CLOCK
$\overline{DRR}$	DATA RECEIVED RESET
DR	DATA RECEIVED
RRI	RECEIVER REGISTER INPUT
MR	MASTER RESET
$\overline{TBRE}$	TRANSMITTER BUFFER REGISTER EMPTY
$\overline{TBRL}$	TRANSMITTER BUFFER REGISTER LOAD
TRE	TRANSMITTER REGISTER EMPTY
TRO	TRANSMITTER REGISTER OUTPUT
$TBR_{1.8}$	TRANSMITTER BUFFER REGISTER INPUTS
CRL	CONTROL REGISTER LOAD
PI	PARITY INHIBIT
SBS	STOP BIT SELECT
$CLS_{1.2}$	CHARACTER LENGTH SELECT
EPE	EVEN PARITY ENABLE
TRC	TRANSMITTER REGISTER CLOCK

Timing diagrams

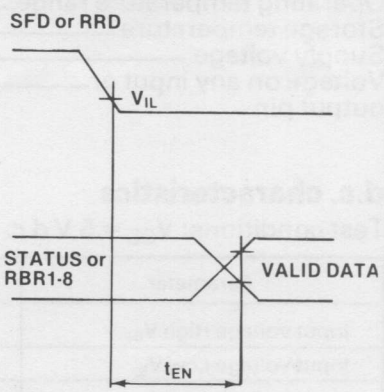
Data input cycle



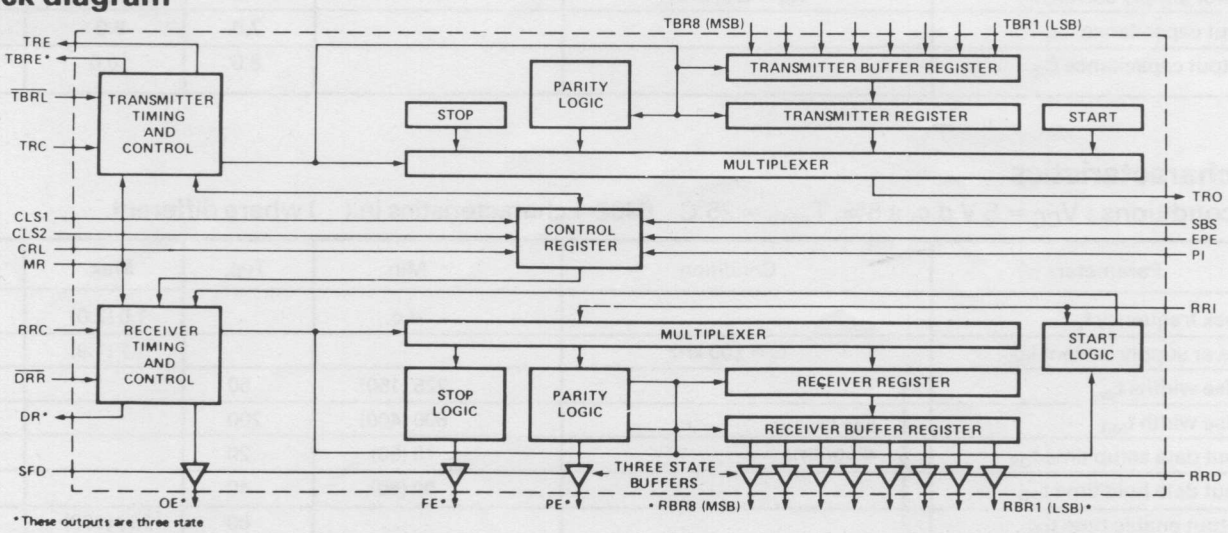
Control register load cycle



Status flag enable time or Data Output enable time



Block diagram



Control inputs

RRD – Receiver register disable – a high level on this input forces the receiver holding register outputs RBR1 – RBR8 to a high impedance state thus allowing direct connection in data bus applications.

SFD – Status flag disable – a high level forces the outputs PE, FE, OE, DR, and TBRE (see status flag description) to a high impedance state.

$\overline{\text{DRR}}$ – Data received reset – a low level on this input clears Data received output (DR) to a low level thereby permitting the next character to be received without an overrun error.

MR – Master reset – a high level clears the PE, FE, OE, DR, and TRE status flags and sets the TBRE and TRO outputs high. Eighteen clock periods after MR goes low, TRE returns high. Note: MR does not clear the receiver buffer register.

CRL – Control register load – a high level loads the control register with the character length, parity and stop bit length. See control register description below.

$\overline{\text{TBRL}}$ – Transmitter buffer register load – a low level transfers data from the inputs TBR1 to TBR8 into the transmitter buffer register. A low to high transition on this input requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed until the current transmission is completed at this point the next character is loaded and transmission of that character commences so that the two characters are transmitted end to end.

Control register – The following inputs are used to set the control register status when the CRL input goes high.

CLS1, CLS2 – Character length select – these two inputs select the character length according to the following table.

Character length (bits)	5	6	7	8
CLS1	L	H	L	H
CLS2	L	L	H	H

PI – Parity inhibit – a high level inhibits parity generation, parity checking and forces the PE status flag output low. This input overrides the EPE input.

EPE – Even parity enable – when the PI is set low a high level on the EPE input generates and checks even parity conversely a low level selects odd parity.

SBS – Stop bit select – this input selects the number of stop bits. The number of stop bits added to the transmitted character also depends on the character length selected by the CLS1 and CLS2 inputs. The following table lists the number of stop bits selected versus the character length and state of the SBS input.

	Character length selected		
SBS input	5 bits	6, 7 or 8 bits	
L	1	1	Stop bits
H	1½	2	

Status flags

TBRE* – Transmitter buffer register empty – a high level on this output indicates that the transmitter buffer register has transferred its contents to the transmitter register and is ready to accept new data.

TRE – Transmitter register empty – a logic high level indicates the transmission is completed including stop bits.

PE* – Parity error – a high level on parity error indicates that the received parity does not match the parity programmed by the control register bits. When parity is inhibited (refer to PI control input) the output is forced low.

FE* – Framing error – a high level indicates the first stop bit is invalid.

OE* – Overrun error – a high level indicates the data received flag was not cleared before the last character was transferred to the receiver register buffer.

DR* – Data received – a high level indicates a character has been correctly received and transferred to the receiver buffer register – this output must be reset before a new character can be received (refer to $\overline{\text{DRR}}$ control input).

* Status flags are three state and can be disabled (high impedance state) by using the status flags disable input (SFD) – refer to control input description.

Data inputs and outputs

RBR1 to RBR8 – The contents of the receiver buffer register appears on these outputs. Word formats less than 8 bits are right justified to RBR1. The outputs are forced to a high impedance state by applying a logic high to the RRD input.

RRI – Receiver register input – serial data on this input is clocked into the receiver register.

TBR1 to TBR8 – Character data is loaded into the transmitter buffer register via these inputs in conjunction with the $\overline{\text{TBRL}}$ input. For character formats of less than 8 bits, the TBR8, 7 or 6 inputs are ignored corresponding to the programmed character length.

TRO – Transmitter register output – character data, start, stop and parity bits appear serially at this output.

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Clock inputs

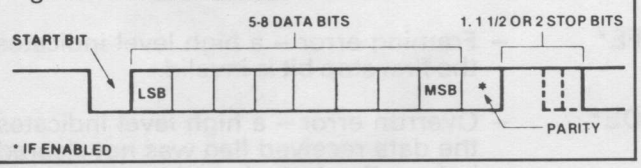
RRC – Receiver register clock – this input determines the rate at which the received data is clocked into the receiver register. The actual clock frequency should be 16 times the required data rate.

TRC – Transmitter register clock – this input sets the transmitted data rate. The frequency of the clock should be 16 times the required data rate.

Transmitter operation

The transmitter section accepts parallel data, formats and transmits in serial form adding start, parity (if selected) and stop bits as shown in Fig. 1.

Figure 1: **Word format**



The sequence of events prior to and following the transmission of the data is described below together with the aid of the timing diagram shown in Fig. 2.

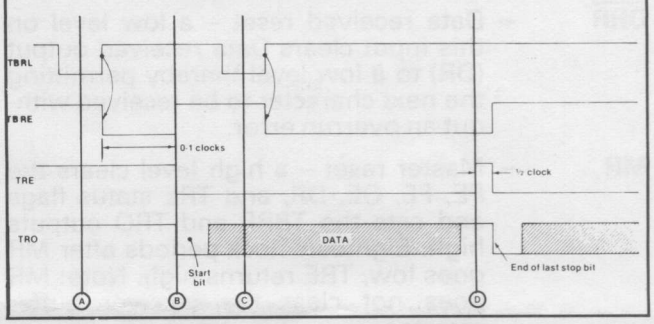
Ⓐ Data is loaded into the TBR from the inputs TR1 to TBR8 by a logic low on $\overline{TBRL}$. Valid data must be present t_{DS} prior to the low to high transition of $\overline{TBRL}$ and remain valid at t_{DH} after this transition. If the data is less than 8 bits only the least significant bits are accepted. Following the transition of $\overline{TBRL}$ from low to high TBRE goes low indicating the TRB is not empty. If the transmitter register TR, is empty indicated by the TRE status output being high the data is transferred to the TR and transmission commences Ⓑ between 0 to 1 clock periods later. Should $\overline{TBRL}$ go low again during the transmission shown at Ⓒ in Fig. 2 the data is loaded into the TBR as before and the TBRE status goes low following the $\overline{TBRL}$ low to high transition however the data is not immediately loaded into the TR, due to the transmission in progress, instead the data remains in the TBR until the last stop bit of the current transmission has been transmitted.

At Ⓓ the data-in the TBR is automatically transferred into the TR and transmission of that character commences.

Receiver operation – refer to Fig. 3.

Data is received in serial form at the RR1 input, when no data is being received this input must remain high, the data is clocked into the RR at the clock rate which should be 16 times the required data rate. A low level on the $\overline{DRR}$ clears the DR line and during the first stop bit data is transferred from the RR to the RBR. If the word length is less than 8 bits the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1.

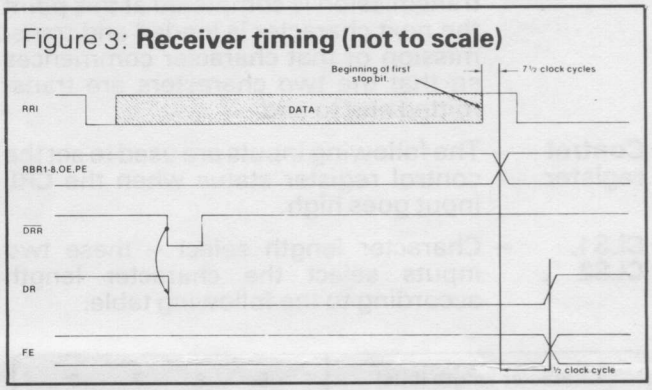
Figure 2: **Transmitter timing**



A logic high on the OE status output indicates an overrun which occurs when the DR line has not been cleared before the present character was transferred to the RBR. A logic high on PE indicates a parity error.

One half clock cycle after the data is transferred to the RBR the DR line is set high and FE is evaluated. A logic high on the FE output indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a correct stop bit is received.

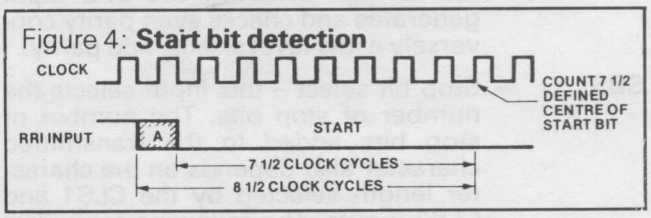
Figure 3: **Receiver timing (not to scale)**



Start bit detection

The receiver uses a 16 times clock for timing. The start bit Ⓐ in Fig. 4 could have occurred as much as one clock cycle before it was detected, as indicated by the crosshatched section. The centre of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the centre of the start bit will be located within ±½ clock cycles, ±1/32 bit or 3.125%. The receiver begins searching for the next start bit at the centre of the first stop bit.

Figure 4: **Start bit detection**



R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company
Telephone: 0536 201234