National Semiconductor

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54LVXC3245
8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs

General Description

The LVXC3245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for real time configurable I/O applications. The V_{CCA} pin accepts a 3V supply level. The A port is a dedicated 3V port. The V_{CCB} pin accepts a 3V-to-5V supply level. The B port is configured to track the V_{CCB} supply level respectively. A 5V level on the V_{CC} pin will configure the I/O pins at a 5V level and a 3V V_{CC} will configure the I/O pins at a 3V level. This device will allow the V_{CCB} voltage source pin and I/O pins on the B port to float when $\overline{OE}$ is HIGH. This feature is necessary to buffer data to and from sockets that require live insertion and removal during normal operation.

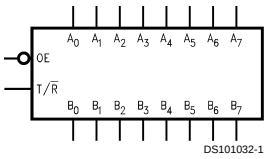
Features

- Bidirectional interface between 3V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Available in Cerpack and CDIP package
- Implements patented EMI reduction circuitry
- Flexible V_{CCB} operating range
- Allows B port and V_{CCB} to float simultaneously when $\overline{OE}$ is HIGH
- Functionally compatible with the 54 series 245
- Standard Microcircuit Drawing (SMD) 5962-9861901

Ordering Code

Order Number	Package Number	Package Description
54LVXC3245W-QML	W24A	24-Lead (0.300" Wide) Ceramic Flatpack
54LVXC3245J-QML	J24F	24-Lead Ceramic Dual-in-line

Logic Symbol



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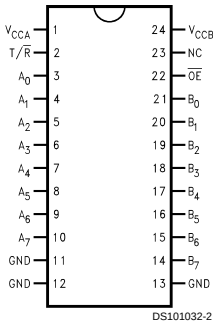
Connection Diagram

Pin Assignment for CDIP and Cerpack



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Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

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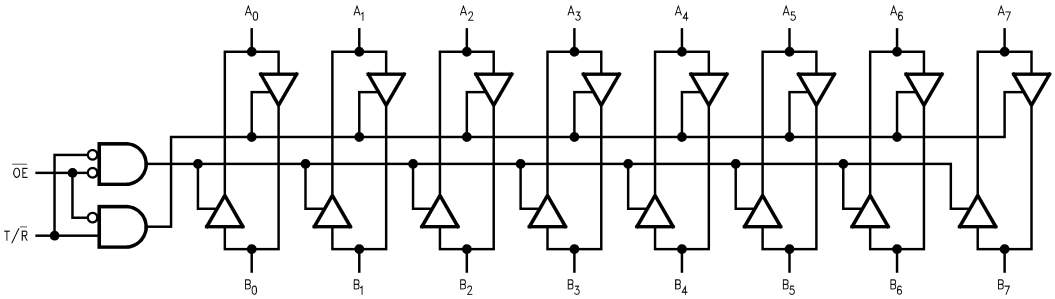
Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CCA}, V_{CCB})	−0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	−0.5V to V_{CCA} +0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A_n	−0.5V to V_{CCA} +0.5V
@ B_n	−0.5V to V_{CCB} +0.5V
DC Input Diode Curr. (I_{IK}) @ $\overline{OE}$, T/$\overline{R}$	±20 mA
DC Output Diode (I_{OK})Current	±50 mA
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
and Max Current	±200 mA
Storage Temperature Range (T_{STG})	−65˚C to +150˚C

Recommended Operating Conditions (Note 2)

Supply Voltage	
V_{CCA}	2.7V to 3.6V
V_{CCB}	3.0V to 5.5V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCA}
Input Output Voltage ($V_{I/O}$)	
@ A_n	0V to V_{CCA}
@ B_n	0V to V_{CCB}
Free Air Operating Temperature (T_A)	−55˚C to +125˚C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The A port unused pins (inputs or I/Os) must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IHA}	Minimum High Level Input Voltage	A_n, $\overline{OE}$, T/$\overline{R}$	2.7	3.0	2.0	V	$V_{OUT} \le 0.1V$ or $\ge V_{CC} - 0.1V$
			3.0	3.6	2.0		
			3.6	5.5	2.0		
V_{IHB}		B_n	2.7	3.0	2.0		
			3.0	3.6	2.0		
			3.6	5.5	3.85		
V_{ILA}	Maximum Low Level Input Voltage	A_n, $\overline{OE}$, T/$\overline{R}$	2.7	3.0	0.8	V	$V_{OUT} \le 0.1V$ or $\ge V_{CC} - 0.1V$
			3.0	3.6	0.8		
			3.6	5.5	0.8		
V_{ILB}		B_n	2.7	3.0	0.8		
			3.0	3.6	0.8		
			3.6	5.5	1.65		
V_{OHA}	Minimum High Level Output Voltage		2.7	3.0	2.6	V	I_{OH} = −100 µA
			3.6	5.5	3.5		I_{OH} = −100 µA
			2.7	3.0	2.2		I_{OH} = −12 mA
			3.0	3.0	2.4		I_{OH} = −12 mA
			3.0	3.0	2.2		I_{OH} = −24 mA
V_{OHB}			2.7	3.0	2.9	V	I_{OH} = −100 µA
			3.6	5.5	5.4		I_{OH} = −100 µA
			2.7	3.0	2.4		I_{OH} = −12 mA
			3.0	3.0	2.2		I_{OH} = −24 mA
			3.0	4.5	3.7		I_{OH} = −24 mA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{OLA}	Maximum Low Level Output Voltage		2.7	3.0	0.1	V	I_{OL} = 100 µA
			3.6	5.5	0.1		I_{OL} = 100 µA
			2.7	3.0	0.3		I_{OL} = 12 mA
			3.0	3.0	0.3		I_{OL} = 12 mA
			3.0	3.0	0.4		I_{OL} = 24 mA
V_{OLB}			2.7	3.0	0.1	V	I_{OL} = 100 µA
			3.6	5.5	0.1		I_{OL} = 100 µA
			2.7	3.0	0.3		I_{OL} = 12 mA
			3.0	3.0	0.4		I_{OL} = 24 mA
			3.0	4.5	0.4		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		3.6	3.6	±1.0	µA	V_I = V_{CCA}, GND
			3.6	5.5	±1.0		
I_{OZA}	Maximum 3-STATE Output Leakage @ A_n		3.6	3.6	±5.0	µA	V_I = V_{IL}, V_{IH}, $\overline{OE}$ = V_{CCA}
			3.6	5.5	±5.0		V_O = V_{CCA}, GND
I_{OZB}	Maximum 3-STATE Output Leakage @ B_n		3.6	3.6	±5.0	µA	V_I = V_{IL}, V_{IH}, $\overline{OE}$ = V_{CCA}
			3.6	5.5	±5.0		V_O = V_{CCB}, GND
ΔI_{CC}	Maximum I_{CC}/Input	B_n	3.6	5.5	1.5	mA	V_I = V_{CCB}–2.1V
		All Inputs	3.6	3.6	0.5		V_I = V_{CC}–0.6V
I_{CCA1}	Quiescent V_{CCA} Supply Current as B Port Floats		3.6	Open	10	µA	A_n = V_{CCA} or GND, B_n = Open, $\overline{OE}$ = V_{CCA}, T/$\overline{R}$ = V_{CCA}, V_{CCB} = Open
I_{CCA2}	Quiescent V_{CCA} Supply Current		3.6	3.6	10	µA	A_n = V_{CCA} or GND, B_n = V_{CCB} or GND, $\overline{OE}$ = GND, T/$\overline{R}$ = GND
			3.6	5.5	10		
I_{CCB}	Quiescent V_{CCB} Supply Current		3.6	3.6	10	µA	A_n = V_{CCA} or GND, B_n = V_{CCB} or GND, $\overline{OE}$ = GND, T/$\overline{R}$ = V_{CCA}
			3.6	5.5	40		
V_{OLPA}	Quiet Output Maximum Dynamic V_{OL}		3.3	3.3	1.0	V	(Note 3)
			3.3	5.0	1.1		
V_{OLPB}			3.3	3.3	0.9	V	(Note 3)
			3.3	5.0	1.6		
V_{OLVA}	Quiet Output Minimum Dynamic V_{OL}		3.3	3.3	-0.7	V	(Note 3)
			3.3	5.0	-0.8		
V_{OLVB}			3.3	3.3	-0.6	V	(Note 3)
			3.3	5.0	-1.1		

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n–1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	T_A = −55°C to +125°C C_L = 50 pF V_{CCA} = 2.7V–3.6V V_{CCB} = 4.5V–5.5V		T_A = −55°C to +125°C C_L = 50 pF V_{CCA} = 2.7V–3.6V V_{CCB} = 3.0V–3.6V		Units
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	9.0	1.0	9.5	ns
t_{PLH}	A to B	1.0	9.0	1.0	9.5	
t_{PHL}	Propagation Delay	1.0	9.0	1.0	9.0	ns
t_{PLH}	B to A	1.0	9.0	1.0	9.0	
t_{PZL}	Output Enable Time	1.0	9.0	1.0	10.0	ns
t_{PZH}	$\overline{OE}$ to B	1.0	9.0	1.0	10.0	
t_{PZL}	Output Enable Time	1.0	11.0	1.0	11.0	ns
t_{PZH}	$\overline{OE}$ to A	1.0	11.0	1.0	11.0	
t_{PHZ}	Output Disable Time	1.0	7.5	1.0	8.0	ns
t_{PLZ}	$\overline{OE}$ to B	1.0	7.5	1.0	8.0	
t_{PHZ}	Output Disable Time	1.0	7.0	1.0	7.0	ns
t_{PLZ}	$\overline{OE}$ to A	1.0	7.0	1.0	7.0	
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 5) Data to Output		1.5		1.5	ns

Note 5: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	10.0	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance	12.0	pF	V_{CCA} = 3.3V V_{CCB} = 5.0V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CCB} = 5.0V V_{CCA} = 3.3V

Note 6: C_{PD} is measured at 10 MHz.

Configurable I/O Application for mixed or unknown Voltages

LVXC3245 is designed to solve 3V/5V interfacing issues when CMOS devices cannot tolerate I/O levels above their applied V_{CC}. If an I/O pin of 3V ICs is driven by 5V ICs, the P-Channel transistor in 3V ICs will conduct causing current flow from I/O bus to the 3V power supply. The resulting high current flow can cause destruction of 3V ICs through latchup effects. To prevent this problem, a current limiting resistor is used typically under direct connection of 3V ICs and 5V ICs, but it causes speed degradation.

In a better solution, the LVXC3245 configures two different output levels to handle the dual supply interface issues. The "A" port is a dedicated 3V port to interface 3V ICs. The "B" port is configurable and accepts a 3V-to-5V supply level. This configurable ″B″ port provides maximum flexibility for interfacing to unknown supply voltages, for interfacing to supply voltages which may change in the future, or for providing flexibility when supplying systems to multiple customers with varying power supply requirements. *Figure 1* shows how the LVXC3245 fits into a system with a 3V subsystem and a 5V subsystem.

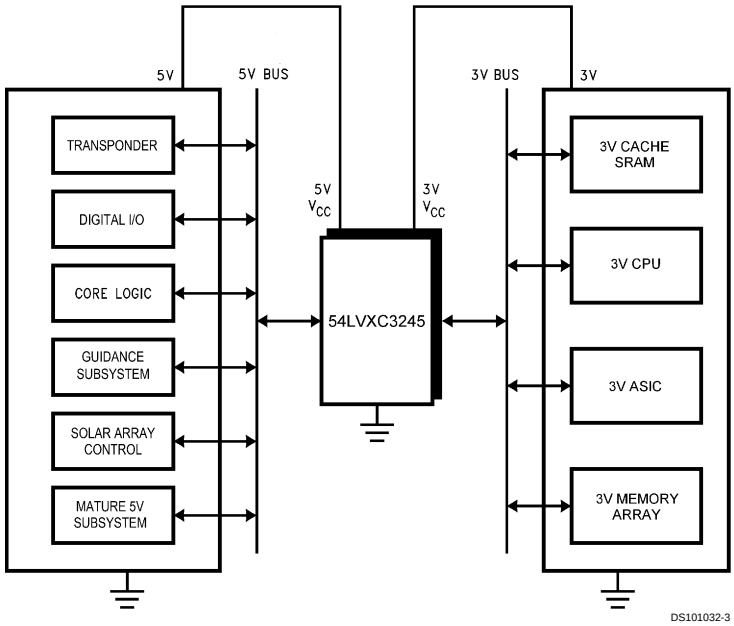


FIGURE 1. LVXC3245 Fits into a System with 3V Subsystem and 5V Subsystem

Configurable I/O Application for mixed or unknown Voltages

(Continued)

Additionally, the LVXC3245 solves two other unique problems: when interfacing to non-TTL compatible signals or when interfacing to components or busses which are pulled up to 5V.

In the first case, when interfacing to non-TTL inputs such as ACMOS or HCMOS where full 5V signal swings are needed, the LVXC3245 can act as an amplifier to translate 0 volt to 3 volt signals up to 0 volt to 5 volt levels as shown in *Figure 2*.

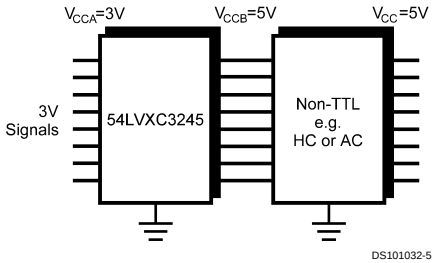


FIGURE 2. LVXC3245 amplifies 3V signals for interfacing to non-TTL inputs.

In the second case, when interfacing to busses which use resistive pull-ups to 5V, it is desirable to avoid connecting 3V devices directly to the bus to avoid excessive power consumption. The LVXC3245 can be used to translate the 3 volt signals to 5 volt levels and eliminate the power consumed by the pull-up resistors.

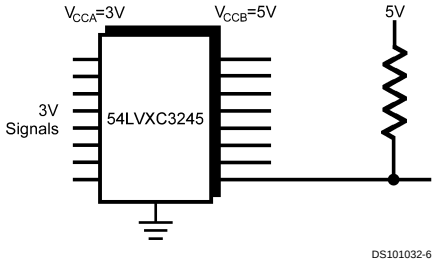
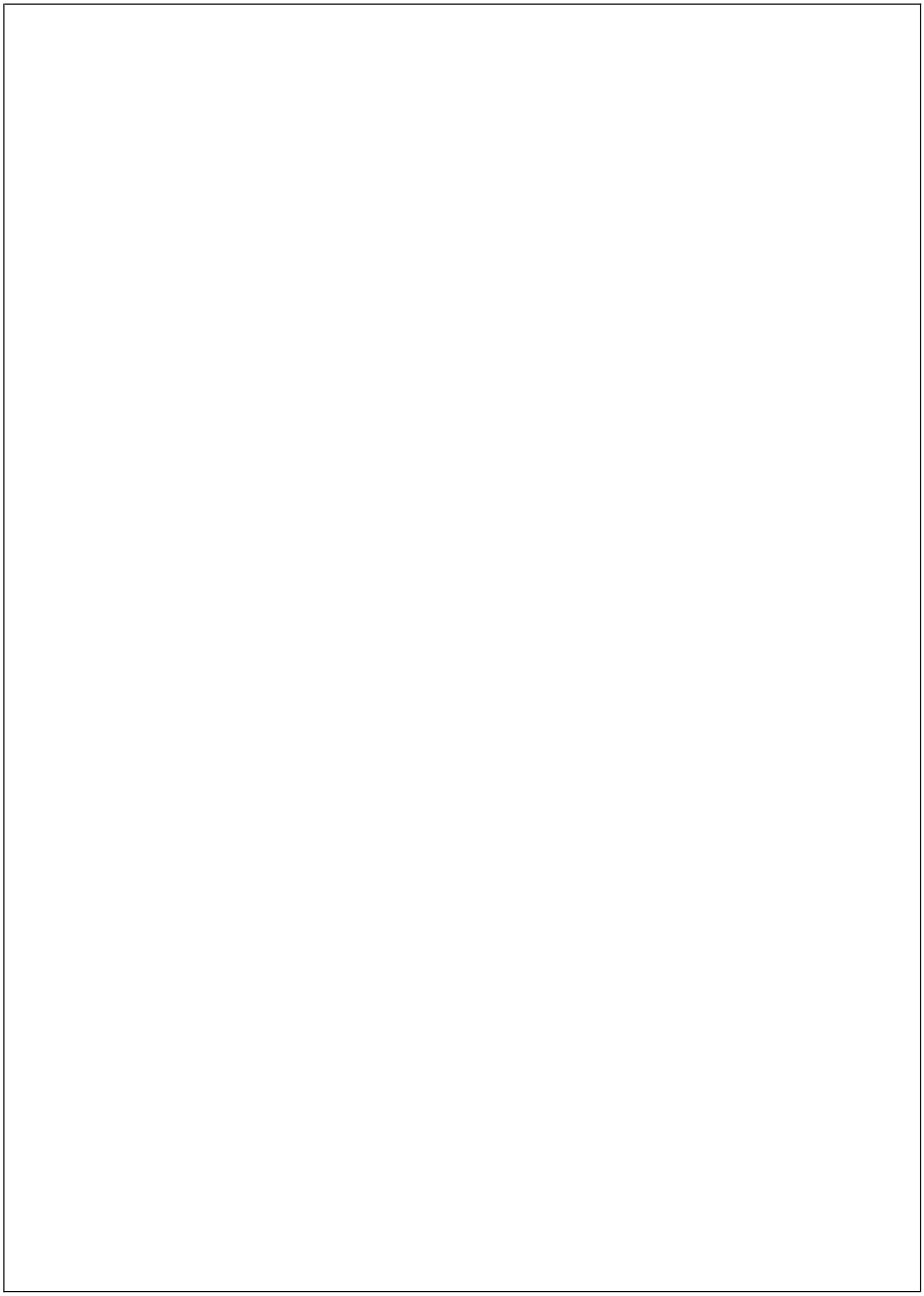
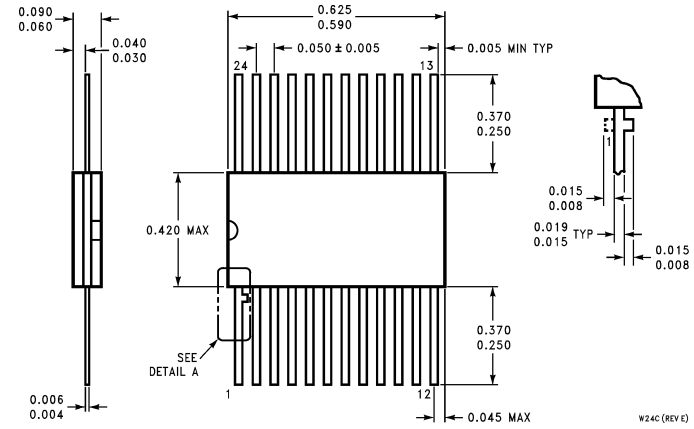


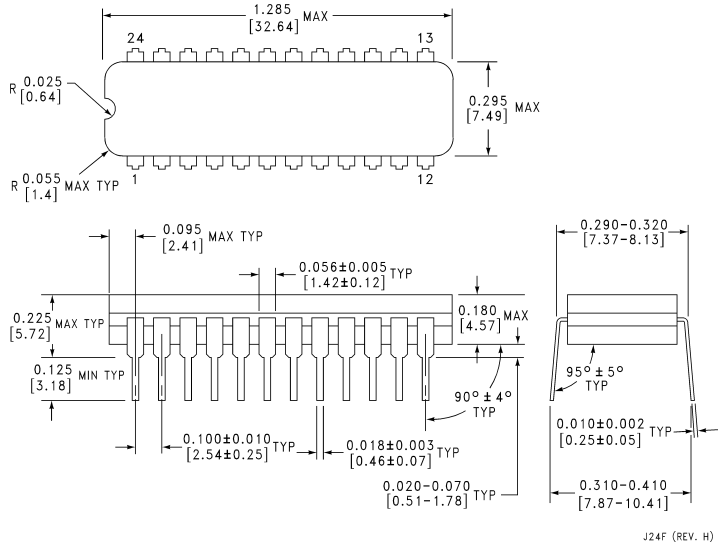
FIGURE 3. LVXC3245 for interfacing to 5V busses with pull-ups minimizes power consumption.



Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead (0.300" Wide) Ceramic Flatpack
Package Number W24C



24-Lead Ceramic Dual-in-line
Package Number J24F

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