National Semiconductor

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54LVX3384
10-Bit Low Power Bus Switch

General Description

The 54LVX3384 provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as two 5-bit switches with separate bus enable ($\overline{OE}$) signals. When $\overline{OE}$ is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

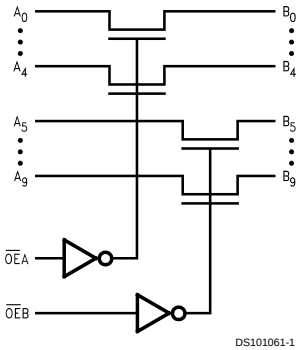
Features

- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Ultra low power with <0.1 µA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL levels
- Available in CDIP and Cerpack Packaging
- Standard Microcircuit Drawing (SMD) 5962-9950701

Ordering Code

Order Number	Package Number	Package Description
54LVX3384J-QML	J24F	24-Lead Ceramic Dual-in-line
54LVX3384W-QML	W24C	24-Lead Cerpack

Logic Diagram



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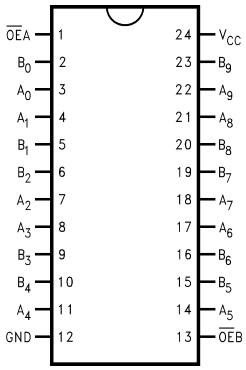
Pin Descriptions

Pin Names	Description
$\overline{OE}A$, $\overline{OE}B$	Bus Switch Enable
A_0–A_9	Bus A
B_0–B_9	Bus B

Connection Diagram

Pin Assignment for CDIP and Cerpack



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Truth Table

$\overline{OE}A$	$\overline{OE}B$	B_0–B_4	B_5–B_9	Function
L	L	A_0–A_4	A_5–A_9	Connect
L	H	A_0–A_4	HIGH-Z State	Connect
H	L	HIGH-Z State	A_5–A_9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−20 mA
DC Output (I_{OUT}) Sink Current	100 mA
Storage Temperature Range (T_{STG})	−65˚C to +150˚C
Power Dissapation	500mW
Junction Temperature (T_J)	175˚C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−55˚C to +125˚C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −55˚C to +125˚C		Units	Condition
			Min	Max		
V_{IC}	Clamp Diode Voltage	4.5		−1.2	V	I_{IN}= − 18mA
V_{IH}	High Level Input Voltage	4.5-5.5	2.0		V	
V_{IL}	Low Level Input Voltage	4.5-5.5		0.8	V	
I_I	Input Leakage Current	5.5		±1.0	µA	$0 \le V_{IN} \le 5.5V$
I_{OZ}	TRI-STATE Leakage Current	5.5		±10.0	µA	$0 \le A, B \le V_{CC}$
R_{ON}	Switch On Resistance (Note 4)	4.5		10	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		20	Ω	V_{IN} = 0V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5		10	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{cc} per Input	5.5		2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND
I_{OFF}	Power Off Leakage Current	0.0		10	µA	V_{IN} = 5.5V or 0.0V
I_{OS}	Short Circuit Output Current (Note 5)	4.5	80		mA	V_{IN} = 4.5V, V_{OUT} = 0.0V

Note 4: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 5: Not more than one output tested at a time.

AC Electrical Characteristics

Symbol	Parameter	T_A = −55°C to +125°C, C_L = 50 pF, RU=RD=500Ω		Units	Conditions	Figure No.
		V_{CC} = 4.5 − 5.5V				
		Min	Max			
t_{PHL}, t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25	ns	V_I = open	*Figures 1, 2*
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}_A$, $\overline{OE}_B$ to An, Bn	1.0	6.0	ns	V_I = 7V for t_{PZL} V_I = open for t_{PZH}	*Figures 1, 2*
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}_A$, $\overline{OE}_B$ to An, Bn	1.0	6.0	ns	I_I = 7V for t_{PLZ} V_I = open for t_{PHZ}	*Figures 1, 2*

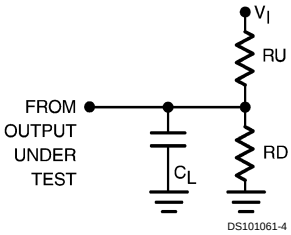
Note 6: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Control Input Capacitance	10	pF	V_{CC} = Open
$C_{I/O}$ (OFF)	Input/Output Capacitance	12	pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ohms source terminated in 50 Ohms
Note: C_L includes load and stray capacitance
Note: Input PRR=1.0 MHz, t_W = 500 nS

FIGURE 1. AC Test Circuit

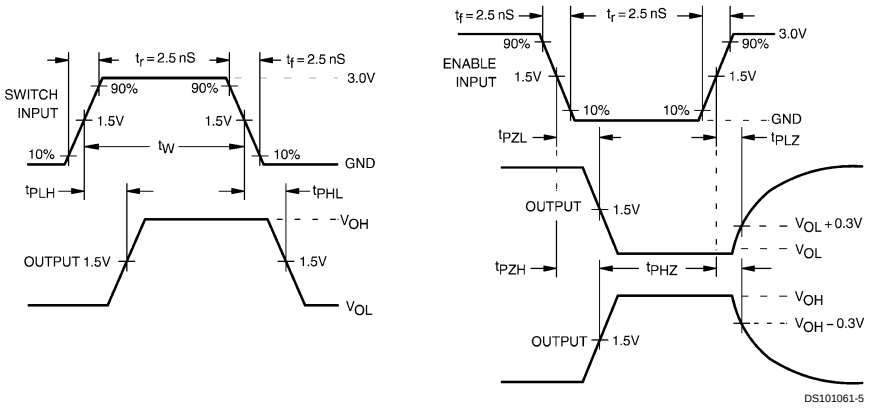
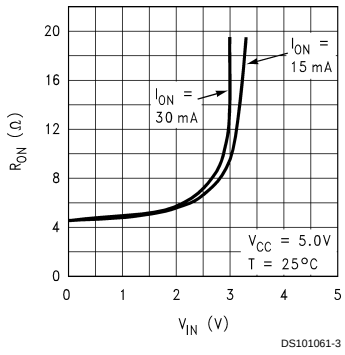
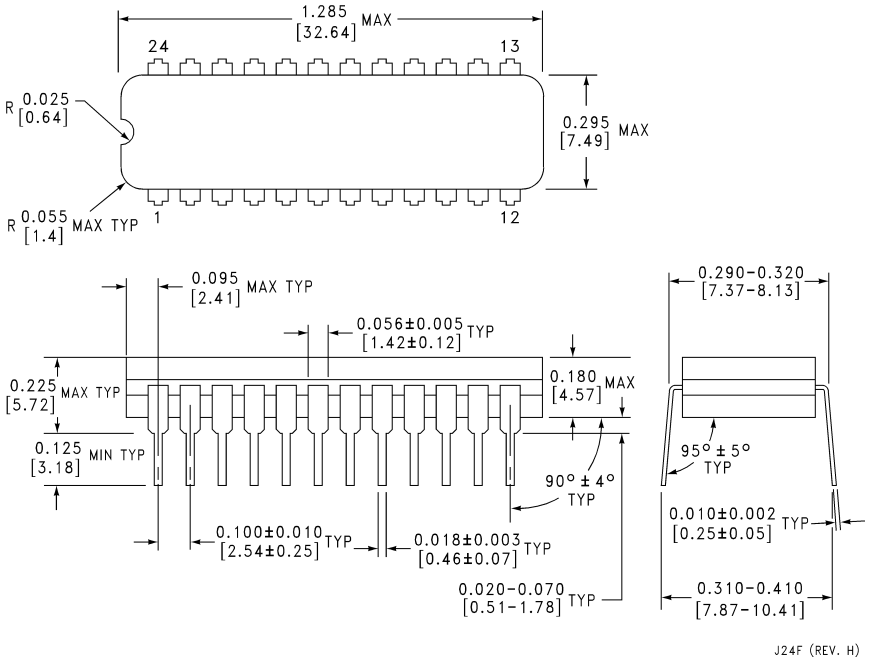


FIGURE 2. AC Waveforms

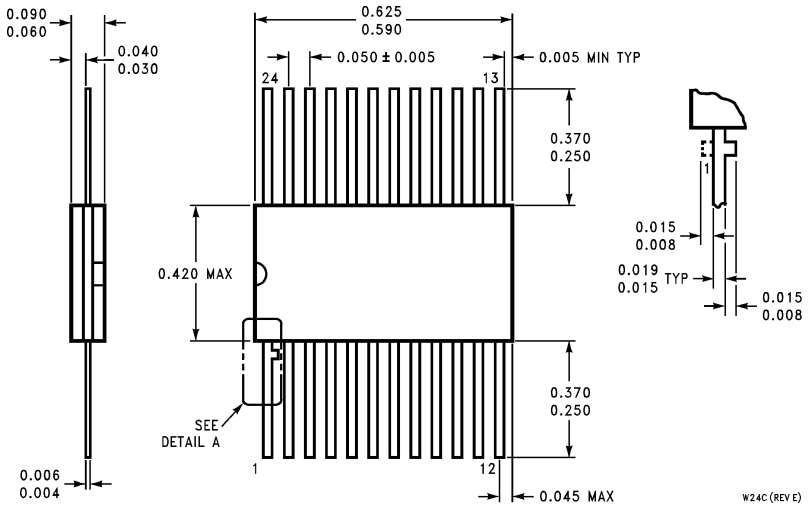
54LVX3384 V_{IN} vs R_{ON} (Typ)



Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-in-line
Package Number J24F



24-Lead Cerpack
Package Number W24C

Notes

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