

November 1994

# 54F/74F194

## 4-Bit Bidirectional Universal Shift Register

### General Description

The 'F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 'F194 is similar in operation to the 'F195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

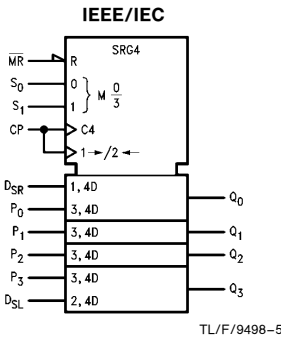
### Features

- Typical shift frequency of 150 MHz
- Asynchronous master reset
- Hold (do nothing) mode
- Fully synchronous serial or parallel data transfers

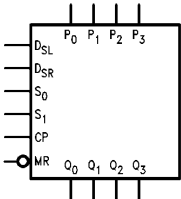
| Commercial        | Military          | Package Number | Package Description                               |
|-------------------|-------------------|----------------|---------------------------------------------------|
| 74F194PC          |                   | N16E           | 16-Lead (0.300" Wide) Molded Dual-In-Line         |
|                   | 54F194DM (Note 2) | J16A           | 16-Lead Ceramic Dual-In-Line                      |
| 74F194SC (Note 1) |                   | M16A           | 16-Lead (0.150" Wide) Molded Small Outline, JEDEC |
| 74F194SJ (Note 1) |                   | M16D           | 16-Lead (0.300" Wide) Molded Small Outline, EIAJ  |
|                   | 54F194FM (Note 2) | W16A           | 16-Lead Cerpack                                   |
|                   | 54F194LM (Note 2) | E20A           | 20-Lead Ceramic Leadless Chip Carrier, Type C     |

**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.  
**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

### Logic Symbols



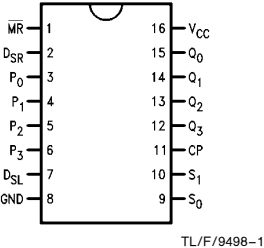
TL/F/9498-5



TL/F/9498-3

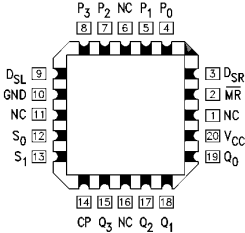
### Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9498-1

Pin Assignment for LCC



TL/F/9498-2

54F/74F194 4-Bit Bidirectional Universal Shift Register

## Unit Loading/Fan Out

| Pin Names       | Description                                  | 54F/74F       |                                                 |
|-----------------|----------------------------------------------|---------------|-------------------------------------------------|
|                 |                                              | U.L. HIGH/LOW | Input $I_{IH}/I_{IL}$<br>Output $I_{OH}/I_{OL}$ |
| $S_0, S_1$      | Mode Control Inputs                          | 1.0/1.0       | 20 $\mu A$ / -0.6 mA                            |
| $P_0-P_3$       | Parallel Data Inputs                         | 1.0/1.0       | 20 $\mu A$ / -0.6 mA                            |
| $D_{SR}$        | Serial Data Input (Shift Right)              | 1.0/1.0       | 20 $\mu A$ / -0.6 mA                            |
| $D_{SL}$        | Serial Data Input (Shift Left)               | 1.0/1.0       | 20 $\mu A$ / -0.6 mA                            |
| CP              | Clock Pulse Input (Active Rising Edge)       | 1.0/1.0       | 20 $\mu A$ / -0.6 mA                            |
| $\overline{MR}$ | Asynchronous Master Reset Input (Active LOW) | 1.0/1.0       | 20 $\mu A$ / -0.6 mA                            |
| $Q_0-Q_3$       | Parallel Outputs                             | 50/33.3       | -1 mA/20 mA                                     |

## Functional Description

The 'F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select ( $S_0, S_1$ ) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data ( $P_0-P_3$ ) and Serial data ( $D_{SR}, D_{SL}$ )

inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ( $\overline{MR}$ ) overrides all other inputs and forces the outputs LOW.

Mode Select Table

| Operating Mode | Inputs          |       |       |          |          |       | Outputs |       |       |       |
|----------------|-----------------|-------|-------|----------|----------|-------|---------|-------|-------|-------|
|                | $\overline{MR}$ | $S_1$ | $S_0$ | $D_{SR}$ | $D_{SL}$ | $P_n$ | $Q_0$   | $Q_1$ | $Q_2$ | $Q_3$ |
| Reset          | L               | X     | X     | X        | X        | X     | L       | L     | L     | L     |
| Hold           | H               | l     | l     | X        | X        | X     | $q_0$   | $q_1$ | $q_2$ | $q_3$ |
| Shift Left     | H               | h     | l     | X        | l        | X     | $q_1$   | $q_2$ | $q_3$ | L     |
|                | H               | h     | l     | X        | h        | X     | $q_1$   | $q_2$ | $q_3$ | H     |
| Shift Right    | H               | l     | h     | l        | X        | X     | L       | $q_0$ | $q_1$ | $q_2$ |
|                | H               | l     | h     | h        | X        | X     | H       | $q_0$ | $q_1$ | $q_2$ |
| Parallel Load  | H               | h     | h     | X        | X        | $p_n$ | $p_0$   | $p_1$ | $p_2$ | $p_3$ |

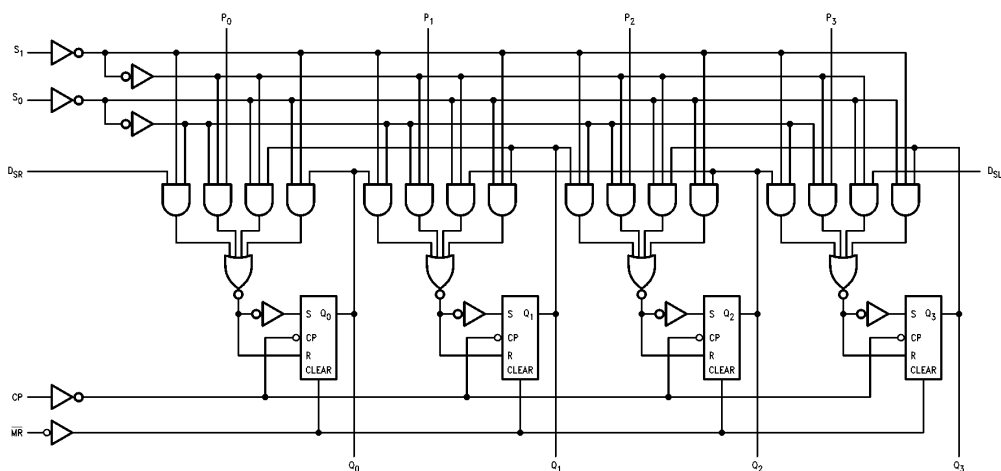
H (h) = High Voltage Level

L (l) = Low Voltage Level

$p_n$  ( $q_n$ ) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.

X = Immaterial

## Logic Diagram



TL/F/9498-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                                                     |                          |
|---------------------------------------------------------------------|--------------------------|
| Storage Temperature                                                 | −65°C to +150°C          |
| Ambient Temperature under Bias                                      | −55°C to +125°C          |
| Junction Temperature under Bias                                     | −55°C to +175°C          |
| Plastic                                                             | −55°C to +150°C          |
| V <sub>CC</sub> Pin Potential to Ground Pin                         | −0.5V to +7.0V           |
| Input Voltage (Note 2)                                              | −0.5V to +7.0V           |
| Input Current (Note 2)                                              | −30 mA to +5.0 mA        |
| Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V) |                          |
| Standard Output                                                     | −0.5V to V <sub>CC</sub> |
| TRI-STATE® Output                                                   | −0.5V to +5.5V           |

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

|                              |                 |
|------------------------------|-----------------|
| Free Air Ambient Temperature |                 |
| Military                     | −55°C to +125°C |
| Commercial                   | 0°C to +70°C    |
| Supply Voltage               |                 |
| Military                     | +4.5V to +5.5V  |
| Commercial                   | +4.5V to +5.5V  |

## DC Electrical Characteristics

| Symbol           | Parameter                         | 54F/74F                 |      |      | Units | V <sub>CC</sub> | Conditions                                           |
|------------------|-----------------------------------|-------------------------|------|------|-------|-----------------|------------------------------------------------------|
|                  |                                   | Min                     | Typ  | Max  |       |                 |                                                      |
| V <sub>IH</sub>  | Input HIGH Voltage                | 2.0                     |      |      | V     |                 | Recognized as a HIGH Signal                          |
| V <sub>IL</sub>  | Input LOW Voltage                 |                         |      | 0.8  | V     |                 | Recognized as a LOW Signal                           |
| V <sub>CD</sub>  | Input Clamp Diode Voltage         |                         |      | −1.2 | V     | Min             | I <sub>IN</sub> = −18 mA                             |
| V <sub>OH</sub>  | Output HIGH Voltage               | 54F 10% V <sub>CC</sub> | 2.5  |      | V     | Min             | I <sub>OH</sub> = −1 mA                              |
|                  |                                   | 74F 10% V <sub>CC</sub> | 2.5  |      |       |                 | I <sub>OH</sub> = −1 mA                              |
|                  |                                   | 74F 5% V <sub>CC</sub>  | 2.7  |      |       |                 | I <sub>OH</sub> = −1 mA                              |
| V <sub>OL</sub>  | Output LOW Voltage                | 54F 10% V <sub>CC</sub> |      | 0.5  | V     | Min             | I <sub>OL</sub> = 20 mA                              |
|                  |                                   | 74F 10% V <sub>CC</sub> |      | 0.5  |       |                 | I <sub>OL</sub> = 20 mA                              |
| I <sub>IH</sub>  | Input HIGH Current                | 54F                     |      | 20.0 | μA    | Max             | V <sub>IN</sub> = 2.7V                               |
|                  |                                   | 74F                     |      | 5.0  |       |                 |                                                      |
| I <sub>BVI</sub> | Input HIGH Current Breakdown Test | 54F                     |      | 100  | μA    | Max             | V <sub>IN</sub> = 7.0V                               |
|                  |                                   | 74F                     |      | 7.0  |       |                 |                                                      |
| I <sub>CEX</sub> | Output HIGH Leakage Current       | 54F                     |      | 250  | μA    | Max             | V <sub>OUT</sub> = V <sub>CC</sub>                   |
|                  |                                   | 74F                     |      | 50   |       |                 |                                                      |
| V <sub>ID</sub>  | Input Leakage Test                | 74F                     | 4.75 |      | V     | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded  |
| I <sub>OD</sub>  | Output Leakage Circuit Current    | 74F                     |      | 3.75 | μA    | 0.0             | V <sub>IOD</sub> = 150 mV<br>All Other Pins Grounded |
| I <sub>IL</sub>  | Input LOW Current                 |                         |      | −0.6 | mA    | Max             | V <sub>IN</sub> = 0.5V                               |
| I <sub>OS</sub>  | Output Short-Circuit Current      |                         | −60  | −150 | mA    | Max             | V <sub>OUT</sub> = 0V                                |
| I <sub>CC</sub>  | Power Supply Current              |                         | 33   | 46   | mA    | Max             |                                                      |

## AC Electrical Characteristics

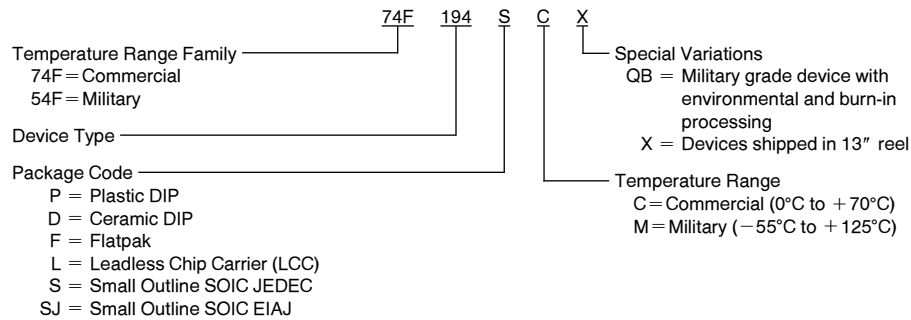
| Symbol           | Parameter                        | 74F                                                                            |     |      | 54F                                                |      | 74F                                                |      | Units |
|------------------|----------------------------------|--------------------------------------------------------------------------------|-----|------|----------------------------------------------------|------|----------------------------------------------------|------|-------|
|                  |                                  | $T_A = +25^{\circ}\text{C}$<br>$V_{CC} = +5.0\text{V}$<br>$C_L = 50\text{ pF}$ |     |      | $T_A, V_{CC} = \text{Mil}$<br>$C_L = 50\text{ pF}$ |      | $T_A, V_{CC} = \text{Com}$<br>$C_L = 50\text{ pF}$ |      |       |
|                  |                                  | Min                                                                            | Typ | Max  | Min                                                | Max  | Min                                                | Max  |       |
| $f_{\text{max}}$ | Maximum Shift Frequency          | 105                                                                            | 150 |      | 90                                                 |      | 90                                                 |      | MHz   |
| $t_{\text{PLH}}$ | Propagation Delay<br>CP to $Q_n$ | 3.5                                                                            | 5.2 | 7.0  | 3.0                                                | 8.5  | 3.5                                                | 8.0  | ns    |
| $t_{\text{PHL}}$ | Propagation Delay<br>MR to $Q_n$ | 3.5                                                                            | 5.5 | 7.0  | 3.0                                                | 8.5  | 3.5                                                | 8.0  |       |
| $t_{\text{PHL}}$ | Propagation Delay<br>MR to $Q_n$ | 4.5                                                                            | 8.6 | 12.0 | 4.5                                                | 14.5 | 4.5                                                | 14.0 | ns    |

## AC Operating Requirements

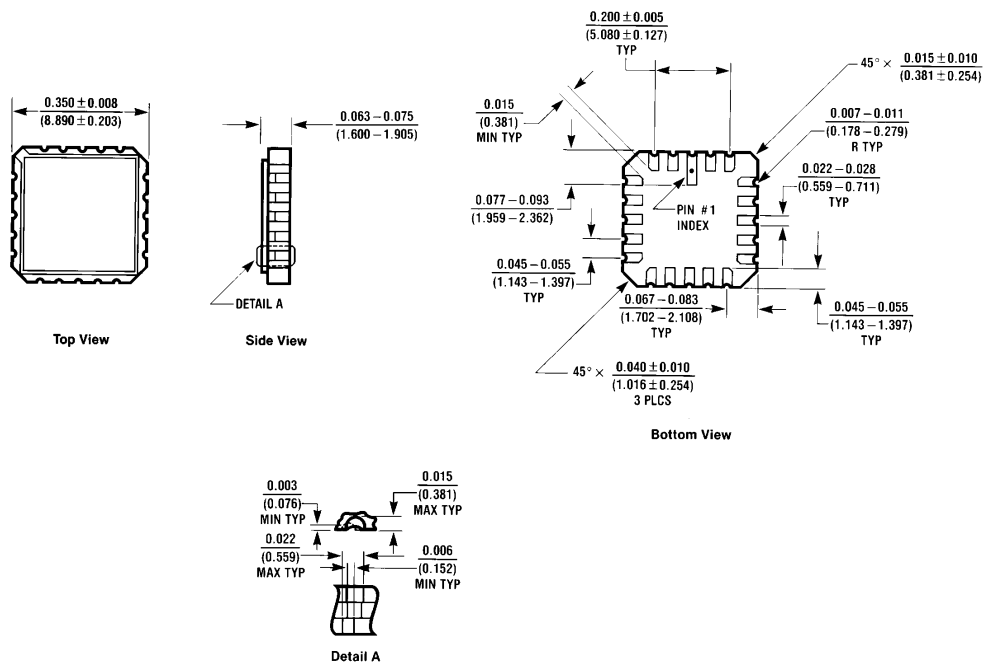
| Symbol           | Parameter                                                      | 74F                                                    |     | 54F                        |     | 74F                        |     | Units |
|------------------|----------------------------------------------------------------|--------------------------------------------------------|-----|----------------------------|-----|----------------------------|-----|-------|
|                  |                                                                | $T_A = +25^{\circ}\text{C}$<br>$V_{CC} = +5.0\text{V}$ |     | $T_A, V_{CC} = \text{Mil}$ |     | $T_A, V_{CC} = \text{Com}$ |     |       |
|                  |                                                                | Min                                                    | Max | Min                        | Max | Min                        | Max |       |
| $t_s(\text{H})$  | Setup Time, HIGH or LOW<br>$P_n$ or $D_{SR}$ or $D_{SL}$ to CP | 4.0                                                    |     | 6.0                        |     | 4.0                        |     | ns    |
| $t_s(\text{L})$  |                                                                | 4.0                                                    |     | 4.0                        |     | 4.0                        |     |       |
| $t_h(\text{H})$  | Hold Time, HIGH or LOW<br>$P_n$ or $D_{SR}$ or $D_{SL}$ to CP  | 1.0                                                    |     | 1.5                        |     | 1.0                        |     | ns    |
| $t_h(\text{L})$  |                                                                | 0                                                      |     | 1.0                        |     | 1.0                        |     |       |
| $t_s(\text{H})$  | Setup Time, HIGH or LOW<br>$S_n$ to CP                         | 10.0                                                   |     | 10.5                       |     | 11.0                       |     | ns    |
| $t_s(\text{L})$  |                                                                | 8.0                                                    |     | 8.0                        |     | 8.0                        |     |       |
| $t_h(\text{H})$  | Hold Time, HIGH or LOW<br>$S_n$ to CP                          | 0                                                      |     | 0                          |     | 0                          |     | ns    |
| $t_h(\text{L})$  |                                                                | 0                                                      |     | 0                          |     | 0                          |     |       |
| $t_w(\text{H})$  | CP Pulse Width, HIGH                                           | 5.0                                                    |     | 5.5                        |     | 5.5                        |     | ns    |
| $t_w(\text{L})$  | $\overline{\text{MR}}$ Pulse Width, LOW                        | 5.0                                                    |     | 5.0                        |     | 5.0                        |     | ns    |
| $t_{\text{rec}}$ | Recovery Time $\overline{\text{MR}}$ to CP                     | 9.0                                                    |     | 9.0                        |     | 11.0                       |     | ns    |

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

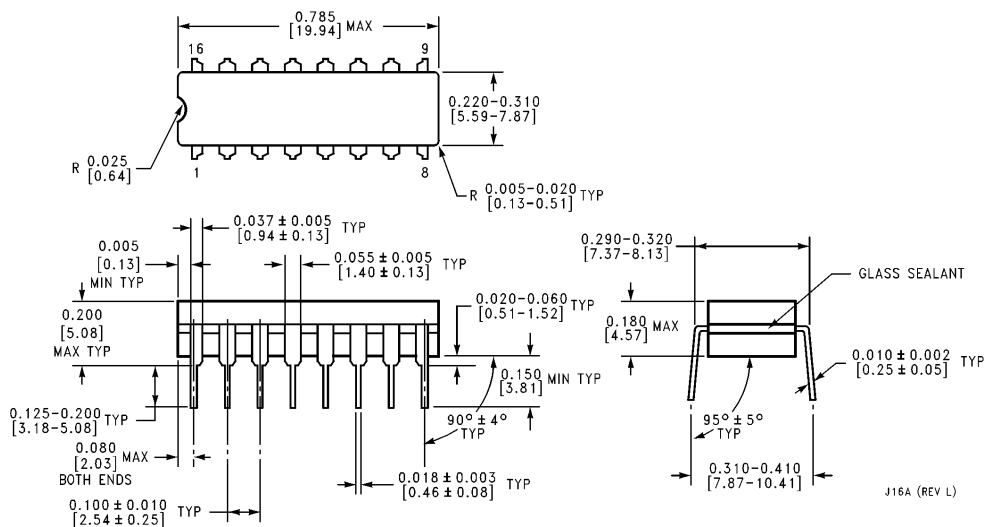


## Physical Dimensions inches (millimeters)

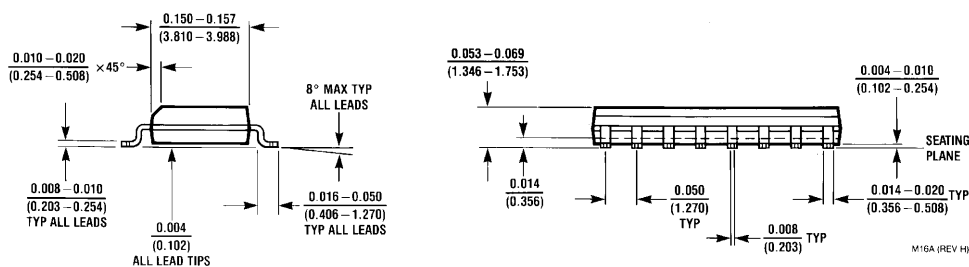
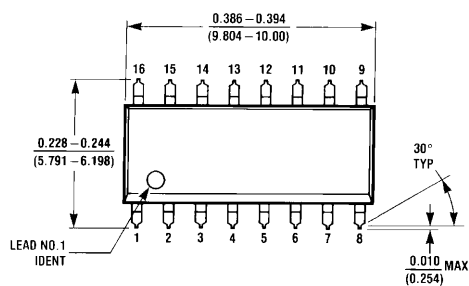


**20-Lead Ceramic Leadless Chip Carrier (L)**  
**NS Package Number E20A**

E20A (REV D)

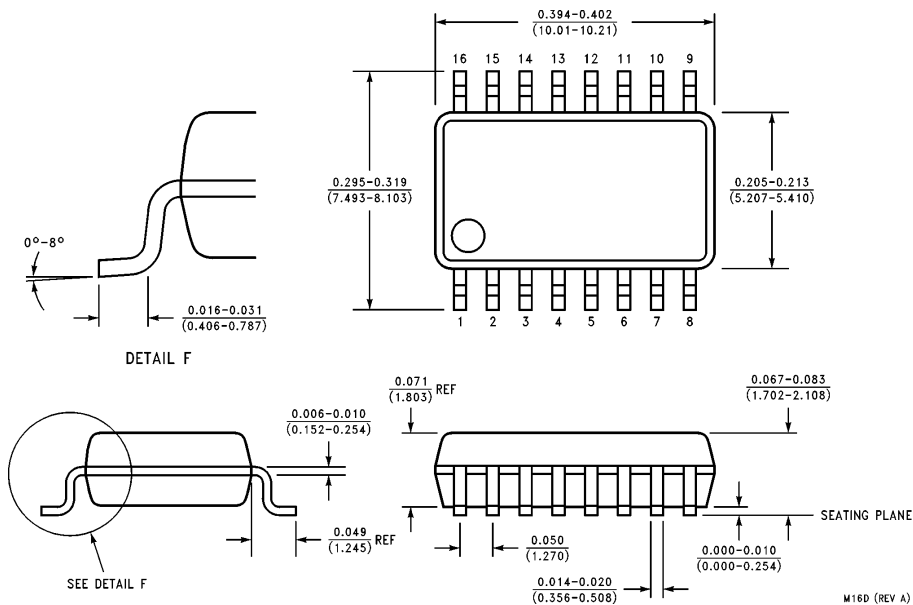
**Physical Dimensions** inches (millimeters) (Continued)

**16-Lead Ceramic Dual-In-Line Package (D)**  
**NS Package Number J16A**

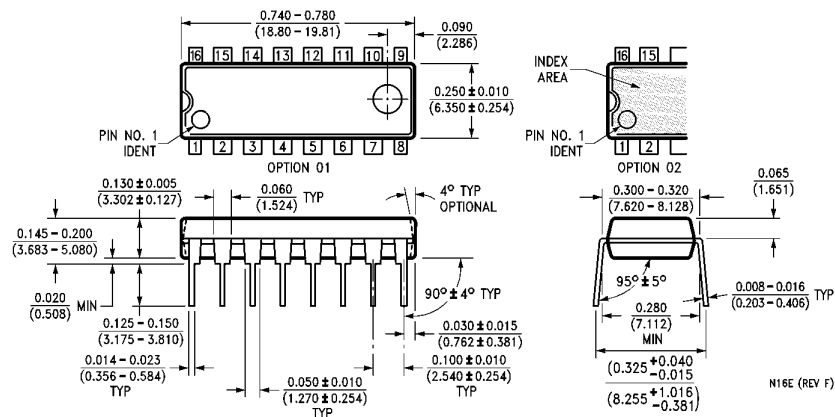


**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)  
NS Package Number M16A**

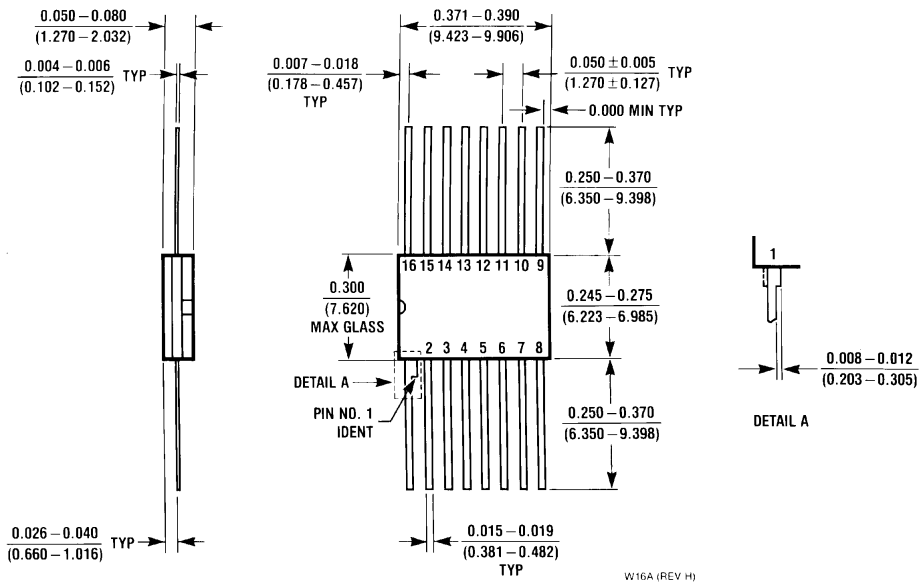
# Physical Dimensions inches (millimeters) (Continued)



**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)**  
**NS Package Number M16D**



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)**  
**NS Package Number N16E**

**Physical Dimensions** inches (millimeters) (Continued)

**16-Lead Ceramic Flatpak (F)**  
**NS Package Number W16A**

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