

## 74ACQ543 • 54ACTQ/74ACTQ543

### Quiet Series Octal Registered Transceiver with TRI-STATE® Outputs

#### General Description

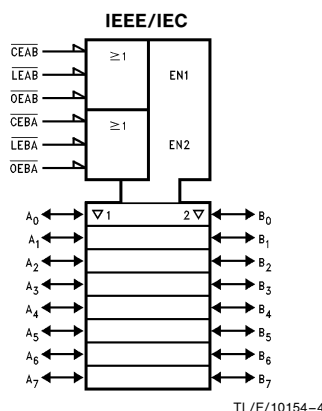
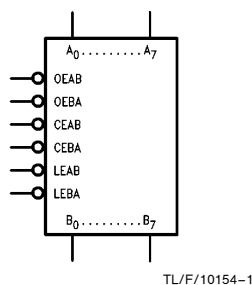
The ACQ/ACTQ543 is a non-inverting octal transceiver containing two sets of D-type registers for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### Features

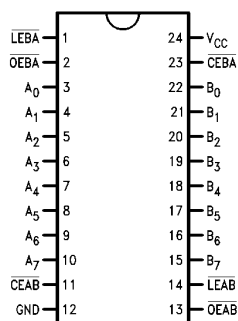
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- 8-bit octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back registers for storage
- Outputs source/sink 24 mA
- 4 kV minimum ESD immunity
- 300 mil slim PDIP/SOIC
- Standard Military Drawing (SMD)  
— 54ACTQ543: 5962-9219201

#### Logic Symbols



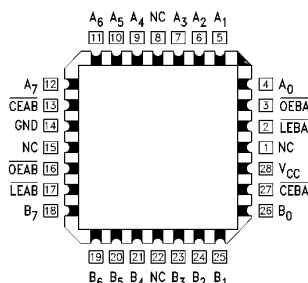
#### Connection Diagrams

Pin Assignment for  
DIP, SOIC, QSOP and Flatpak



TL/F/10154-2

Pin Assignment  
for LCC



TL/F/10154-3

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Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
$A_0-A_7$	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
$B_0-B_7$	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

## Functional Description

The 'ACQ/'ACTQ543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{CEAB}$ ) input must be LOW in order to enter data from  $A_0-A_7$  or take data from  $B_0-B_7$ , as indicated in the Data I/O Control Table. With  $\overline{CEAB}$  LOW, a LOW signal on the A-to-B Latch Enable ( $\overline{LEAB}$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{LEAB}$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$  inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

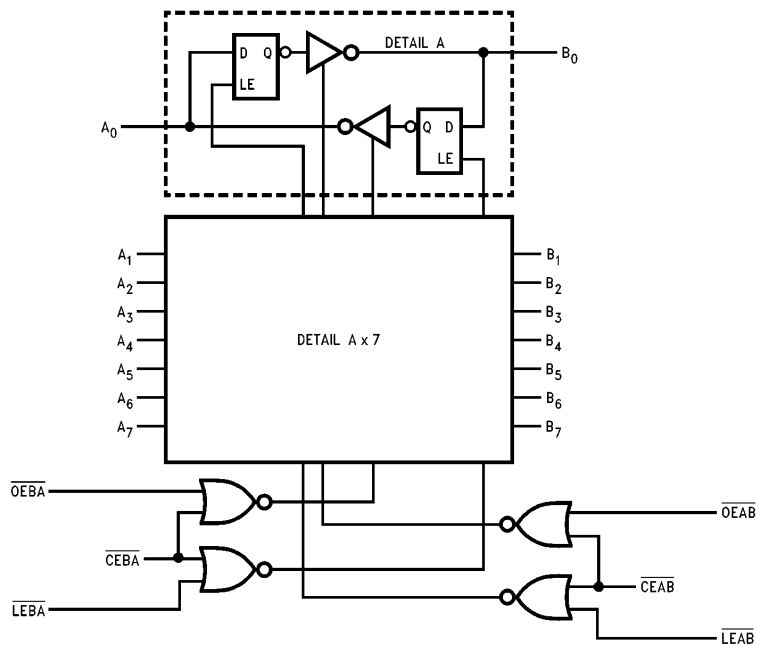
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$

## Logic Diagram



TL/F/10154-8

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	−0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	−65°C to +150°C
DC Latch-up Source or Sink Current	±300 mA
Junction Temperature ( $T_J$ )	
CDIP	175°C
PDIP	140°C

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## Recommended Operating Conditions

Supply Voltage $V_{CC}$	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ ) (Note 2)	
74ACQ/ACTQ	−40°C to +85°C
54ACTQ	−55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACQ Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note:** All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

## DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	74ACQ		74ACQ		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V <sub>IL</sub>	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V <sub>OH</sub>	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I <sub>OUT</sub> = −50 μA
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> −12 mA I <sub>OH</sub> −24 mA −24 mA
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V <sub>OL</sub>	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I <sub>OUT</sub> = 50 μA
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 12 mA I <sub>OL</sub> 24 mA 24 mA
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V <sub>I</sub> = V <sub>CC</sub> , GND (Note 1)

\*Maximum of 8 outputs loaded; thresholds on input associated with output under test.

## DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74ACQ		74ACQ		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits				
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>		5.5			−75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 1)	
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5		±0.6	±6.0	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.1	1.5		V	Figures 2-12, 13 (Notes 2, 3)	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	−0.6	−1.2		V	Figures 2-12, 13 (Notes 2, 3)	
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Notes 2, 4)	
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Notes 2, 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

**Note 2:** Plastic DIP package.

**Note 3:** Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

**Note 4:** Max number of Data Inputs (n) switching. (n−1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	74ACTQ		54ACTQ		74ACTQ		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = −55°C to +125°C		T <sub>A</sub> = −40°C to +85°C			
			Typ	Guaranteed Limits						
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	2.0 2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	0.8 0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	4.4	V	I <sub>OUT</sub> = −50 μA	
		5.5	5.49	5.4	5.4	5.4	5.4			
		4.5		3.86	3.70	3.76		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> −24 mA	
		5.5		4.86	4.70	4.76		V	I <sub>OH</sub> −24 mA	
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
		5.5	0.001	0.1	0.1	0.1	0.1			
		4.5		0.36	0.50	0.44		V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 24 mA	
		5.5		0.36	0.50	0.44		V	I <sub>OL</sub> 24 mA	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND	
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5		±0.6	±11.0	6.0	6.0	μA	V <sub>(OE)</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND	
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.6	1.5	1.5	mA	V <sub>I</sub> = V <sub>CC</sub> − 2.1V	
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5			50	75	75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>		5.5			−50	−75	−75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 1)	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.1	1.5				V	Figures 2-12, 13 (Notes 2, 3)	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	−0.6	−1.2				V	Figures 2-12, 13 (Notes 2, 3)	
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2				V	(Notes 2, 4)	
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8				V	(Notes 2, 4)	

\*Maximum of 8 outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ@ 25°C.

**Note 2:** Plastic DIP package.

**Note 3:** Max number of outputs defined as (n), (n−1) Data Inputs are driven 0V to 3V, one output @ GND.

**Note 4:** Max number of Data Inputs (n) switching. (n−1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACQ			74ACQ		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	3.3 5.0	1.5 1.5	8.0 5.0	11.0 7.0	1.5 1.5	11.5 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA, LEAB to A <sub>n</sub> , B <sub>n</sub>	3.3 5.0	1.5 1.5	9.0 6.0	12.5 8.0	1.5 1.5	13.0 8.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub> CEBA or CEAB to A <sub>n</sub> or B <sub>n</sub>	3.3 5.0	1.5 1.5	10.5 7.0	15.0 9.5	1.5 1.5	15.5 10.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub> CEBA or CEAB to A <sub>n</sub> or B <sub>n</sub>	3.3 5.0	1.0 1.0	8.0 5.0	11.0 7.0	1.0 1.0	11.5 7.5	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew**	3.3 5.0		1.0 0.5	1.5 1.0		1.5 1.0	ns

\*Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

\*\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design. Not tested.

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACQ		74ACQ	Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF	
			Typ	Guaranteed Minimum		
t <sub>s</sub>	Setup Time, HIGH or LOW A <sub>n</sub> or B <sub>n</sub> to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	3.3 5.0		3.0	3.0	ns
t <sub>h</sub>	Hold Time, HIGH or LOW A <sub>n</sub> or B <sub>n</sub> to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	3.3 5.0		1.5	1.5	ns
t <sub>w</sub>	Latch Enable Pulse Width, LOW	3.3 5.0		4.0	4.0	ns

\*Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.0V ±0.3V

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACTQ			54ACTQ		74ACTQ		Units
			T <sub>A</sub> = + 25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = −55°C to + 125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = −40°C to + 85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	5.0	1.5	5.5	7.5	2.0	9.5	1.5	8.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA, LEAB to A <sub>n</sub> , B <sub>n</sub>	5.0	1.5	6.5	8.5	2.0	11.0	1.5	9.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub> CEBA or CEAB to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	8.0	10.0	1.5	13.0	1.5	10.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEBA or OEAB to A <sub>n</sub> or B <sub>n</sub> CEBA or CEAB to A <sub>n</sub> or B <sub>n</sub>	5.0	1.0	5.5	7.5	1.5	9.0	1.0	8.0	ns
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew**	5.0		0.5	1.0				1.0	ns

\*Voltage Range 5.0 is 5.0V ±0.5V

\*\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design. Not tested.

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACTQ		54ACTQ		74ACTQ		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = −55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50 pF		
			Typ	Guaranteed Minimum					
t <sub>s</sub>	Setup Time, HIGH or LOW A <sub>n</sub> or B <sub>n</sub> to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	5.0		3.0	3.0	3.0		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW A <sub>n</sub> or B <sub>n</sub> to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	5.0		1.5	1.5	1.5		ns	
t <sub>w</sub>	Latch Enable Pulse Width, LOW	5.0		4.0	4.0	4.0		ns	

\*Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	70.0	pF	V <sub>CC</sub> = 5.0V

## FACT Noise Characteristics

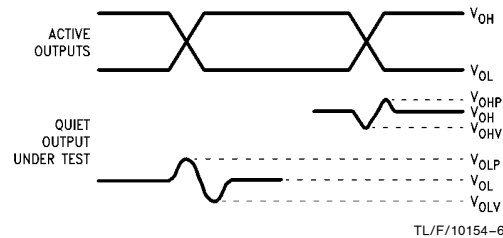
The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

### Equipment:

Hewlett Packard Model 8180A Word Generator  
PC-163A Test Fixture  
Tektronics Model 7854 Oscilloscope

### Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set  $V_{CC}$  to 5.0V
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.



**FIGURE 8. Quiet Output Noise Voltage Waveforms**

**Note A.**  $V_{OHP}$  and  $V_{OLP}$  are measured with respect to ground reference.

**Note B.** Input pulses have the following characteristics:  $f = 1$  MHz,  
 $t_r = 3$  ns,  $t_f = 3$  ns, skew < 150 ps.

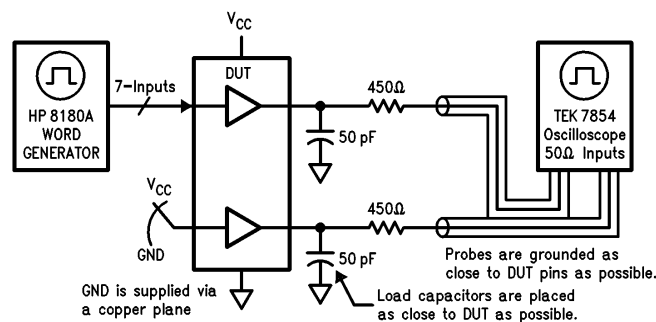
6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

### $V_{OLP}/V_{OLV}$ and $V_{OHP}/V_{OHV}$ :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output during the HL transition. Measure  $V_{OHP}$  and  $V_{OHV}$  on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

### $V_{ILD}$ and $V_{IHD}$ :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level,  $V_{IL}$ , until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input LOW voltage level at which oscillation occurs is defined as  $V_{ILD}$ .
- Next increase the input HIGH voltage level on the word generator,  $V_{IH}$  until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability on the measurements.



**FIGURE 9. Simultaneous Switching Test Circuit**



The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

Temperature Range Family — 74ACTQ 543 P C QR

74ACQ = Commercial  
74ACTQ = Commercial TTL-Compatible  
54ACTQ = Military TTL-Compatible

Device Type —

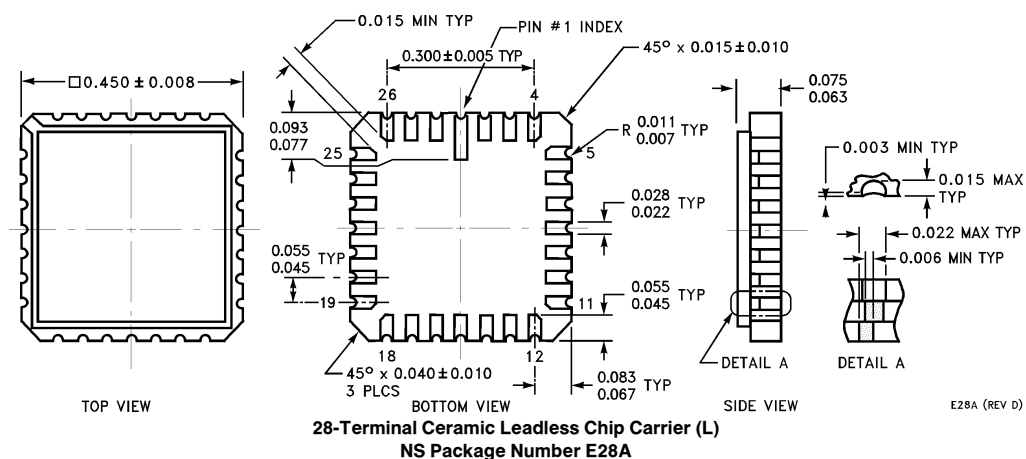
Package Code —

P = Plastic DIP  
D = Ceramic DIP  
F = Flatpak  
L = Leadless Ceramic Chip Carrier (LCC)  
S = Small Outline Package (SOIC)  
QS = Quarter Size Outline Package (QSOP)

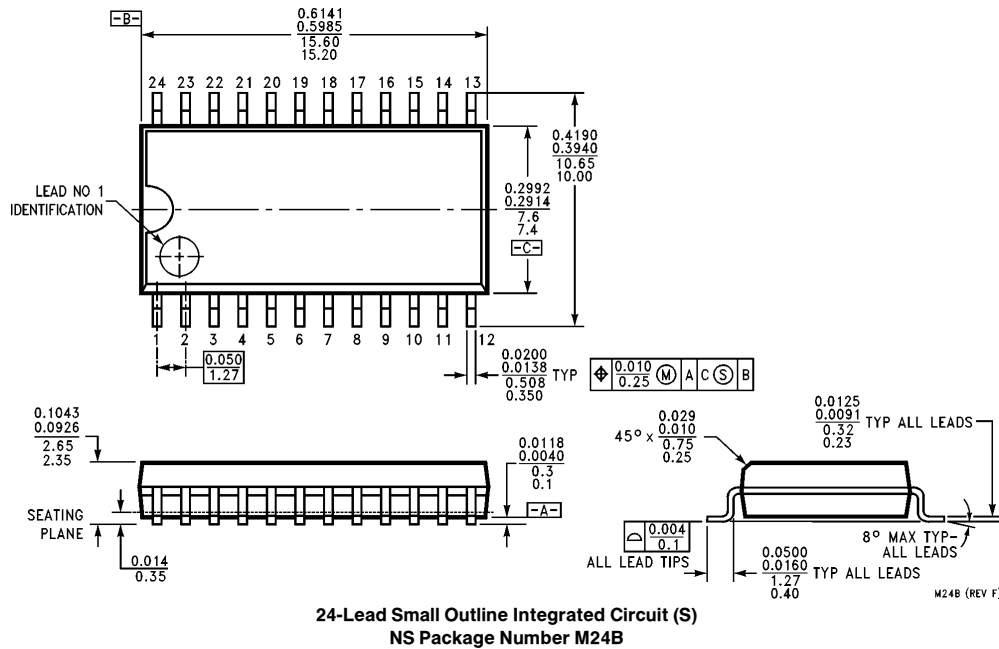
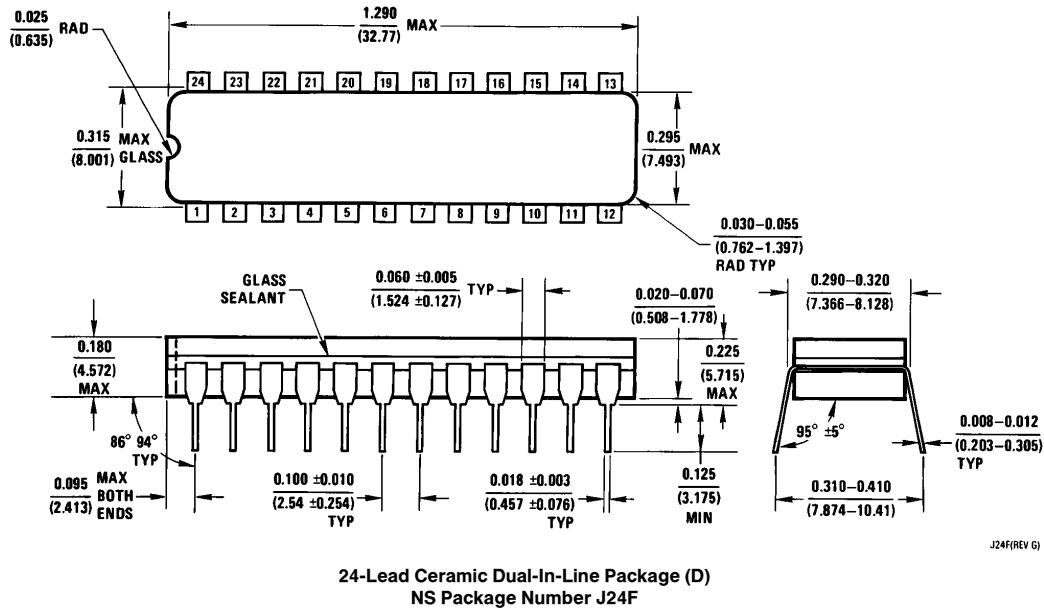
Special Variations  
X = Device shipped in 13" reels  
QR = Commercial grade device with burn-in  
QB = Military grade device with environmental and burn-in processing shipped in tubes

Temperature Range  
C = Commercial (–40°C to +85°C)  
M = Military (–55°C to +125°C)

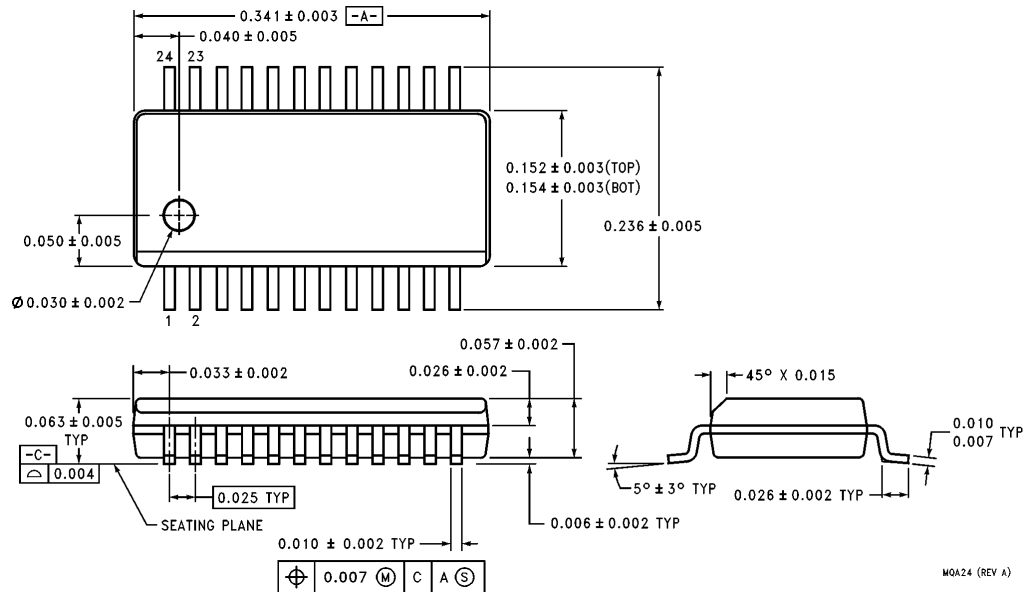
### Physical Dimensions inches (millimeters)



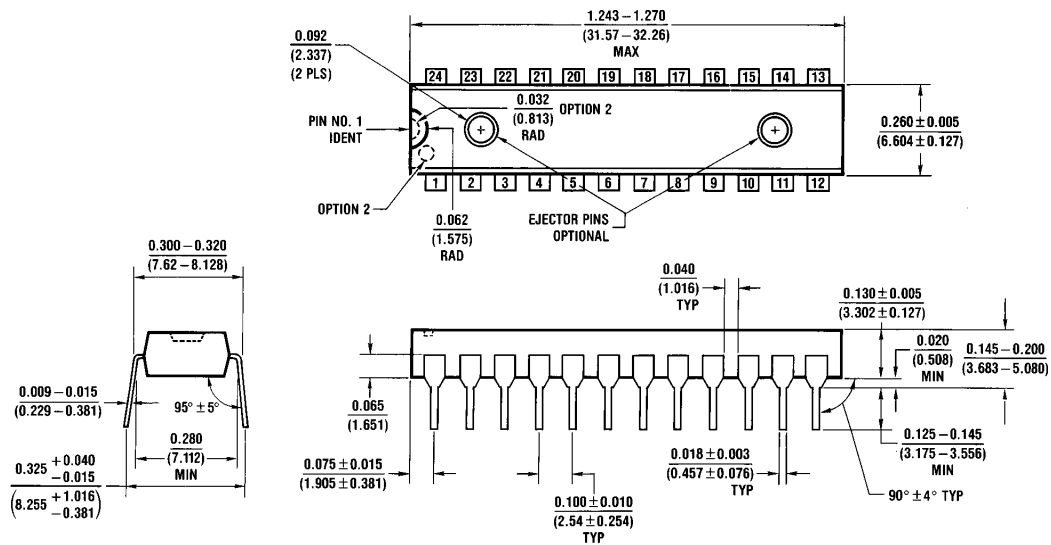
# Physical Dimensions inches (millimeters) (Continued)



# Physical Dimensions inches (millimeters) (Continued)



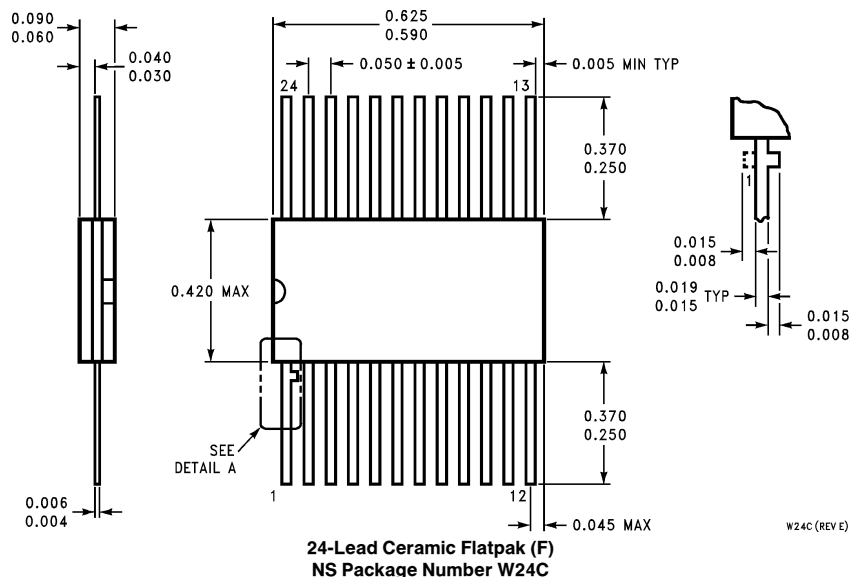
**24-Lead Quarter Size Outline Package (QS)**  
**NS Package Number MQA24**



**24-Lead Plastic Dual-In-Line Package (P)**  
**NS Package Number N24C**

# Physical Dimensions inches (millimeters) (Continued)

Lit. # 114664



## LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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