5410 series

VCXO Module ICs with Built-in Varicap

OVERVIEW

The 5410 series are VCXO module ICs supported 20MHz to 62MHz fundamental oscillation. They employ a recently developed varicap diode fabrication process at fixation communication usage that provides a low phase noise characteristic and a wide frequency pulling range without any external components. The 5410 series are ideal for wide pulling range, low phase noise, VCXO modules.

FEATURES

- VCXO with recently developed varicap diode built-in
- Wide frequency pulling range
  ±150ppm@A1 version, VC=1.65±1.65V, f=40MHz
  (Crystal unit: γ= 330, C0 = 1.3pF)
  ±140ppm@B1 version, VC=1.65±1.65V, f=61.44MHz
  (Crystal unit: γ= 350, C0 = 3.2pF)
- Oscillation frequency range (for fundamental oscillation):
  20 to 40MHz (A1～A5 version)
  40 to 62MHz (B1～B3 version)
- Low phase noise: -135dBc/Hz@A1 version, 1kHz Offset, f=40MHz
  -160dBc/Hz@A1 version, 10MHz Offset, f=40MHz
  (Crystal unit: γ= 330, C0 = 1.3pF)
  -126dBc/Hz@B1 version, 1kHz Offset, f=61.44MHz
  -160dBc/Hz@B1 version, 10MHz Offset, f=61.44MHz
  (Crystal unit: γ= 350, C0 = 3.2pF)
- Operating supply voltage range: 2.97 to 3.63V
- Operating current consumption
  1.6mA@A1 version, f=40MHz, Q pin no load
  2.7mA@B1 version, f=61.44MHz, Q pin no load
- Frequency divider built-in
  Selectable by version: f_{OSC},f_{OSC}/2,f_{OSC}/4,f_{OSC}/8,f_{OSC}/16
- CMOS output
- Output drive capability: 2.8mA
- -40 to 105°C operating temperature range
- Standby function
  High impedance in standby mode, oscillator stops
- CMOS output duty level (1/2V_{DD})
- 50±5% output duty
- Wafer form (WF5410xx)
- Chip form (CF5410xx)

APPLICATIONS

Miniature VCXO modules for fixation communication

SERIES CONFIGURATION

Operating supply voltage range [V]	Recommended operating frequency range*1 [MHz]	Output frequency and version name				
		f_{OSC}	f_{OSC}/2	f_{OSC}/4	f_{OSC}/8	f_{OSC}/16
2.97 to 3.63	20 to 40	5410A1	5410A2	5410A3	5410A4	5410A5
	40 to 62	5410B1	5410B2	5410B3	-	-

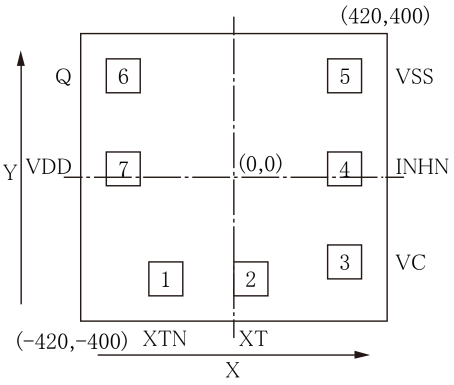
*1. The recommended oscillation frequency is a yardstick value derived from the resonator used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to resonator characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

ORDERING INFORMATION

Device	Package	Version name
WF5410xx-4	Wafer form	WF5410□□-4 Form WF: Wafer form CF: Chip (Die) form Frequency divider function Oscillation frequency range A: 20 to 40MHz B: 40 to 62MHz
CF5410xx-4	Chip form	

PAD LAYOUT

(Unit: µm)



Chip size: 0.84mm × 0.80mm

Chip thickness: 130µm

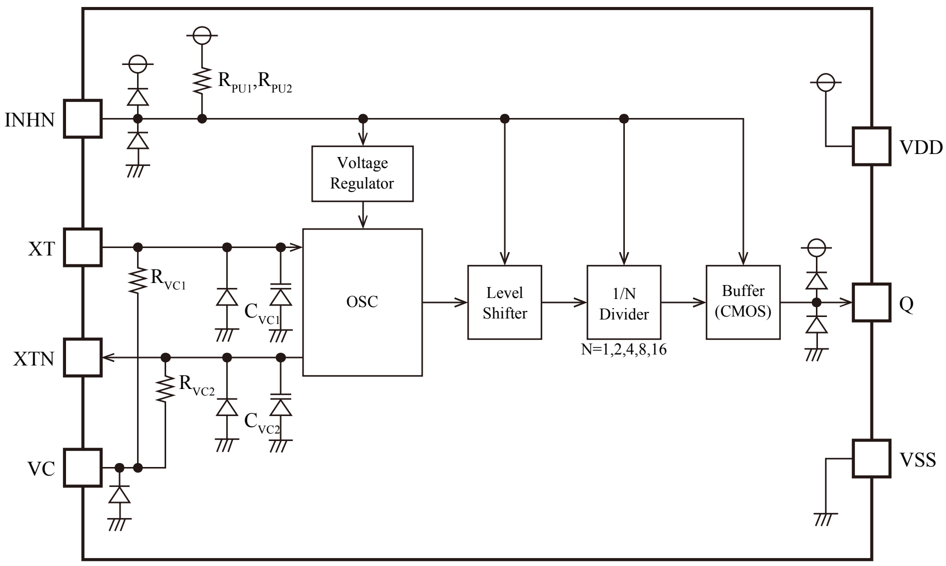
PAD size: 90µm

Chip base: V_{SS} level

PIN DESCRIPTION and PAD COORDINATE

No.	Pin	I/O	Description	PAD coordinate [µm]	
				X	Y
1	XTN	O	Crystal connection pins.	-189.0	-295.0
2	XT	I	Crystal is connected between XT and XTN.	59.4	-295.0
3	VC	I	Oscillation frequency control voltage input pin (positive polarity) (frequency increase with increasing voltage)	315.0	-244.6
4	INHN	I	Input pin controlled output state (oscillator stops when LOW), power-saving pull-up resistor built-in	315.0	34.2
5	VSS	-	(-) ground	315.0	280.2
6	Q	O	Output one of f_{OSC}, $f_{OSC}/2$, $f_{OSC}/4$, $f_{OSC}/8$, $f_{OSC}/16$	-315.0	280.2
7	VDD	-	(+) supply voltage	-315.0	34.2

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Condition		Rating	Unit
Supply voltage range*1	V_{DD}	Between VDD and VSS		-0.3 to +5.0	V
Input voltage range*1*2	V_{IN}	Input pins		-0.3 to V_{DD}+0.3	V
Output voltage range*1*2	V_{OUT}	Output pins		-0.3 to V_{DD}+0.3	V
Junction temperature*3	T_j			+125	°C
Storage temperature range*4	T_{STG}	Wafer form, Chip form		-65 to +125	°C
Output current*3	I_{OUT}	Q pin	T_a = -40～+85°C	±20	mA
			T_a = -40～+105°C	±10	

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.
*2. V_{DD} is a V_{DD} value of recommended operating conditions.
*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.
*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Oscillation frequency range*1	f_{OSC}	5410A1～5410A5 version	20		40	MHz
		5410B1～5410B3 version	40		62	
Output frequency range	f_{OUT}	5410A1～5410A5 version	1.25		40	MHz
		5410B1～5410B3 version	10		62	
Operating supply voltage	V_{DD}	Between VDD and VSS*2	2.97		3.63	V
Input voltage	V_{IN}	VC pin , INHN pin	V_{SS}		V_{DD}	V
Operating temperature	T_a		-40		+105	°C
Output load	C_L	Q pin			15	pF

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
*2. Mount a ceramic chip capacitor that is larger than 0.01μF proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5410 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics
5410A1～5410A5 version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +105°C unless otherwise noted.

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Current consumption	I_{DD}	5410A1(f_{OSC}), measurement 1, no load, INHN="OPEN", V_{DD}=3.3V, f_{OSC}=40MHz, f_{OUT}=40MHz		1.6	3.0	mA
		5410A2(f_{OSC}/2), measurement 1, no load, INHN="OPEN", V_{DD}=3.3V, f_{OSC}=40MHz, f_{OUT}=20MHz		1.2	1.8	mA
		5410A3(f_{OSC}/4), measurement 1, no load, INHN="OPEN", V_{DD}=3.3V, f_{OSC}=40MHz, f_{OUT}=10MHz		1.1	1.6	mA
		5410A4(f_{OSC}/8), measurement 1, no load, INHN="OPEN", V_{DD}=3.3V, f_{OSC}=40MHz, f_{OUT}= 5MHz		1.0	1.5	mA
		5410A5(f_{OSC}/16), measurement 1, no load, INHN="OPEN", V_{DD}=3.3V, f_{OSC}=40MHz, f_{OUT}=2.5MHz		0.9	1.4	mA
Standby current	I_{STB}	measurement 1, INHN="Low", T_a = -40～+85°C			10	µA
		measurement 1, INHN="Low", T_a = -40～+105°C			100	µA
HIGH-level output voltage	V_{OH}	measurement 2, Q pin, I_{OH}=-2.8mA	V_{DD}-0.4			V
LOW-level output voltage	V_{OL}	measurement 2, Q pin, I_{OL}=2.8mA			0.4	V
HIGH-level input voltage	V_{IH}	measurement 3, INHN pin	0.7V_{DD}			V
LOW-level input voltage	V_{IL}	measurement 3, INHN pin			0.3V_{DD}	V
Output leakage current	I_Z	measurement 4, Q pin, T_a=25°C , INHN="Low"	-1		1	µA
Pull-up resistance	R_{PU1}	measurement 5, INHN pin, V_{INHN}=0V	1	3.5	9	MΩ
	R_{PU2}	measurement 5, INHN pin, V_{INHN}=0.7V_{DD}	23	47	71	kΩ
Oscillator block built-in resistance	R_{VC1}	measurement 6, between XT and VC, A1 version	210	420	630	kΩ
		measurement 6, between XT and VC, A2, A3, A4, A5 version	397	793	1190	kΩ
	R_{VC2}	measurement 6, between XTN and VC	116	233	350	kΩ
Oscillator block built-in capacitance	C_{VC1}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance., V_C=0.3V	5.1	5.6	6.2	pF
		V_C=1.65V	2.5	3.1	3.6	pF
		V_C=3.0V	1.2	1.5	1.8	pF
	C_{VC2}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance., V_C=0.3V	7.6	8.4	9.3	pF
		V_C=1.65V	3.8	4.7	5.4	pF
		V_C=3.0V	1.7	2.3	2.8	pF
Input leakage resistance	R_{VIN}	measurement 7, VC pin, T_a=25°C	10			MΩ
Maximum modulation frequency	F_M	measurement 10, -3dB frequency, T_a=25°C, V_{DD}=3.3V, V_C=1.65V±1.65V, crystal=40MHz (R1=42Ω, C0=1.3pF)	15	25		kHz

5410B1～5410B3 version

V_{DD}=2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a= -40 to +105°C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				MIN	TYP	MAX	
Current consumption	I_{DD}	5410B1(f_{OSC}), measurement 1, no load, INHN=”OPEN”, V_{DD}=3.3V, f_{OSC}=61.44MHz, f_{OUT}=61.44MHz			2.7	5.0	mA
		5410B2(f_{OSC}/2), measurement 1, no load, INHN=”OPEN”, V_{DD}=3.3V, f_{OSC}=61.44MHz, f_{OUT}=30.72MHz			2.0	3.2	mA
		5410B3(f_{OSC}/4), measurement 1, no load, INHN=”OPEN”, V_{DD}=3.3V, f_{OSC}=61.44MHz, f_{OUT}=15.36MHz			1.6	2.6	mA
Standby current	I_{STB}	measurement 1, INHN=“Low”	T_a = -40～+85°C			10	μA
			T_a = -40～+105°C			100	
HIGH-level output voltage	V_{OH}	measurement 2, Q pin, I_{OH}=-2.8mA		V_{DD}-0.4			V
LOW-level output voltage	V_{OL}	measurement 2, Q pin, I_{OL}=2.8mA				0.4	V
HIGH-level input voltage	V_{IH}	measurement 3, INHN pin		0.7V_{DD}			V
LOW-level input voltage	V_{IL}	measurement 3, INHN pin				0.3V_{DD}	V
Output leakage current	I_Z	measurement 4, Q pin, T_a=25°C , INHN=“Low”		-1		1	μA
Pull-up resistance	R_{PU1}	measurement 5, INHN pin, V_{INHN}=0V		1	3.5	9	MΩ
	R_{PU2}	measurement 5, INHN pin, V_{INHN}=0.7V_{DD}		23	47	71	kΩ
Oscillator block built-in resistance	R_{VC1}	measurement 6, between XT and VC	B1 version	210	420	630	kΩ
			B2, B3 version	303	606	909	
	R_{VC2}	measurement 6, between XTN and VC		116	233	350	
Oscillator block built-in capacitance	C_{VC1}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	V_C=0.3V	5.1	5.6	6.2	pF
			V_C=1.65V	2.5	3.1	3.6	
			V_C=3.0V	1.2	1.5	1.8	
	C_{VC2}	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	V_C=0.3V	5.1	5.6	6.2	pF
			V_C=1.65V	2.5	3.1	3.6	
			V_C=3.0V	1.2	1.5	1.8	
Input leakage resistance	R_{VIN}	measurement 7, VC pin, T_a=25°C		10			MΩ
Maximum modulation frequency	F_M	measurement 10, -3dB frequency, T_a=25°C V_{DD}=3.3V, V_C=1.65V±1.65V crystal=61.44MHz (R1=20Ω, C0=3.2pF)		15	25		kHz

Switching Characteristics

5410A1～5410A5 version

V_{DD} = 2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}= 0V, T_a = -40 to +105°C unless otherwise noted

Parameter	Symbol	Condition		Rating			Unit
				MIN	TYP	MAX	
AC HIGH-level output voltage	V_{TOP}	measurement 8, C_L=15pF		0.9V_{DD}			V
AC LOW-level output voltage	V_{BASE}	measurement 8, C_L=15pF				0.1V_{DD}	V
Q pin Output rise time	t_r	measurement 8, C_L=15pF 0.1V_{DD}→0.9V_{DD}	T_a = -40～+85°C		2.8	6.0	ns
			T_a = -40～+105°C			6.5	
Q pin Output fall time	t_f	measurement 8, C_L=15pF 0.9V_{DD}→0.1V_{DD}	T_a = -40～+85°C		3.0	6.0	ns
			T_a = -40～+105°C			6.5	
Q pin Output duty cycle	DUTY	measurement 8, V_{DD}=3.3V C_L=15pF, T_a=25°C,		45	50	55	%
Q pin Output enable time	t_{OE}	measurement 9, T_a=25°C, C_L=15pF				2	ms
Q pin Output disable delay time	t_{OD}	measurement 9, T_a=25°C, C_L=15pF				200	ns

Note. The ratings are measured by using the NPC standard crystal and jig. They may vary due to crystal characteristics, so they must be carefully evaluated.

5410B1～5410B3 version

V_{DD} = 2.97 to 3.63V, V_C=0.5V_{DD}, V_{SS}= 0V, T_a = -40 to +105°C unless otherwise noted

Parameter	Symbol	Condition		Rating			Unit
				MIN	TYP	MAX	
AC HIGH-level output voltage	V_{TOP}	measurement 8, C_L=15pF		0.9V_{DD}			V
AC LOW-level output voltage	V_{BASE}	measurement 8, C_L=15pF				0.1V_{DD}	V
Q pin Output rise time	t_r	measurement 8, C_L=15pF 0.1V_{DD}→0.9V_{DD}	T_a = -40～+85°C		2.2	5.0	ns
			T_a = -40～+105°C			5.5	
Q pin Output fall time	t_f	measurement 8, C_L=15pF 0.9V_{DD}→0.1V_{DD}	T_a = -40～+85°C		2.4	5.0	ns
			T_a = -40～+105°C			5.5	
Q pin Output duty cycle	DUTY	measurement 8, V_{DD}=3.3V C_L=15pF, T_a=25°C,		45	50	55	%
Q pin Output enable time	t_{OE}	measurement 9, T_a=25°C, C_L=15pF				2	ms
Q pin Output disable delay time	t_{OD}	measurement 9, T_a=25°C, C_L=15pF				200	ns

Note. The ratings are measured by using the NPC standard crystal and jig. They may vary due to crystal characteristics, so they must be carefully evaluated.

Switching Time Measurement Waveform

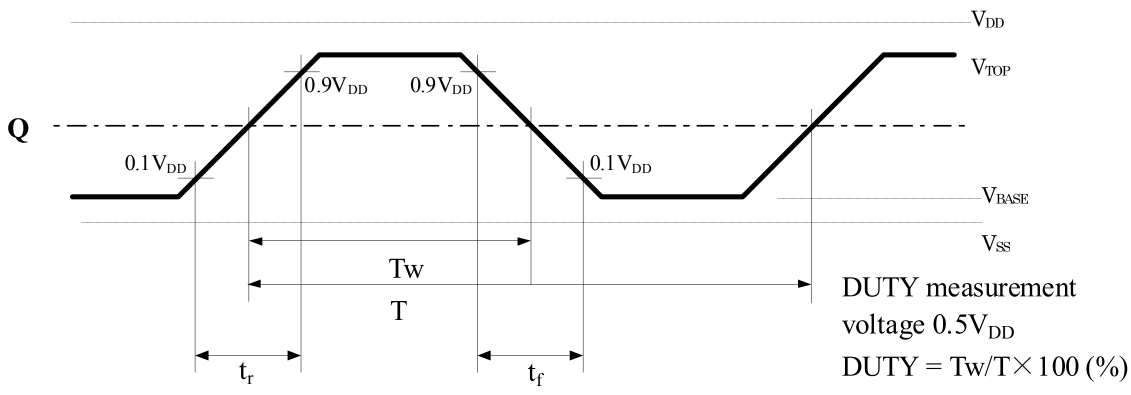
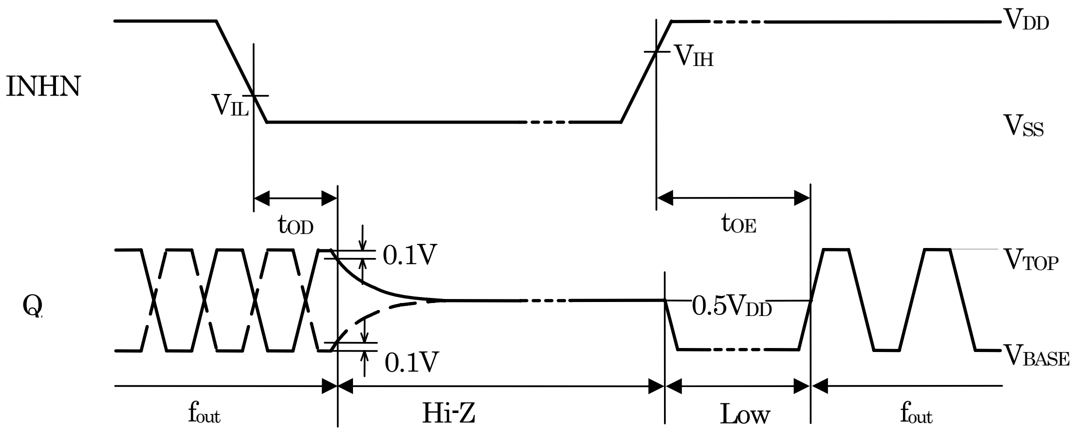


Figure 1. Output switching waveform



When INHN goes HIGH to LOW, the Q output becomes high impedance.

When INHN goes LOW to HIGH, the Q output goes LOW once and then becomes normal output operation after having detected oscillation signals.

Figure 2. Switching waveform controlled output state

FUNCTIONAL DESCRIPTION

INHN Function

Q output is stopped and becomes high impedance.

Power Saving Pull-up Resistor

The INHN pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level (HIGH or LOW).
When INHN is tied to LOW level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance. When INHN is left open circuit or tied to HIGH level, the pull-up resistance becomes small (R_{PU2}), thus internal circuit of INHN becomes HIGH level.
Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

Boot function

It becomes easy to start oscillation by making XT pin potential to V_{DD} level when oscillation starts up. A current flows into VC pin when the voltage below a V_{DD} level is being applied to VC pin. A boot function is canceled after an oscillation start.

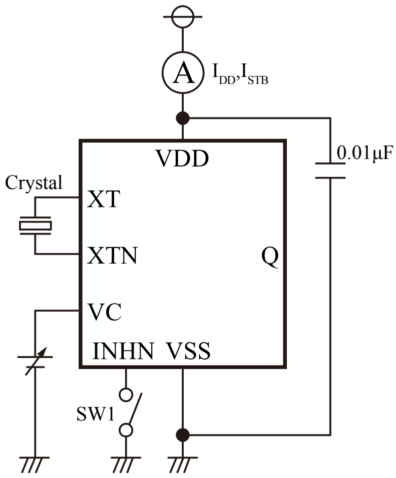
Oscillation Start-up Detector Function

The 5410 series have an oscillation detection circuit. The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit starts up. This function avoids the abnormal oscillation in the initial power up and in a reactivation by INHN.

MEASUREMENT CIRCUITS

MEASUREMENT CIRCUIT 1

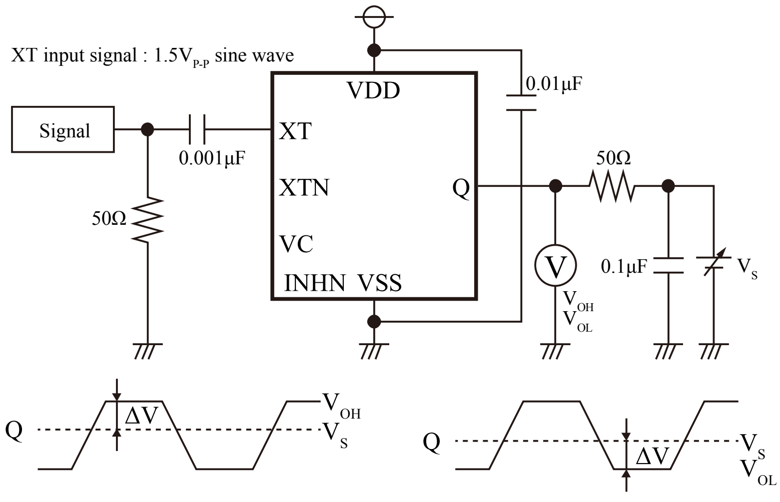
Measurement Parameter: I_{DD}, I_{STB}



Parameter	SW1
I_{DD}	OFF
I_{STB}	ON

MEASUREMENT CIRCUIT 2

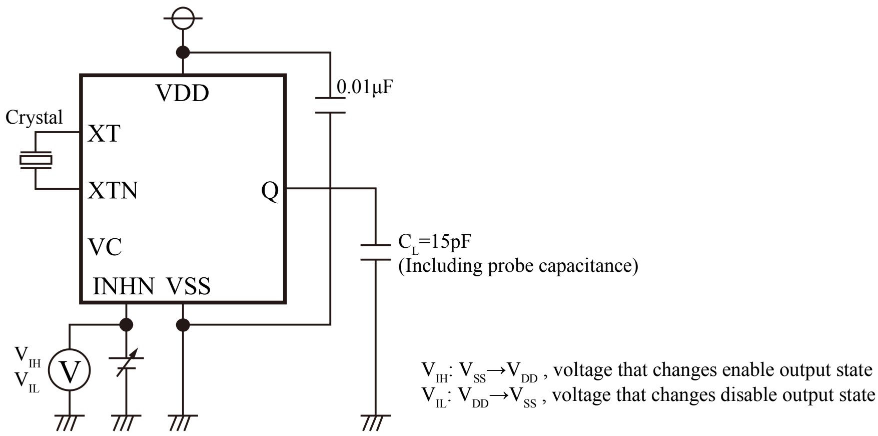
Measurement Parameter: V_{OH}, V_{OL}



V_S adjusted so that $\Delta V=50\times I_{OH}$ V_S adjusted so that $\Delta V=50\times I_{OL}$

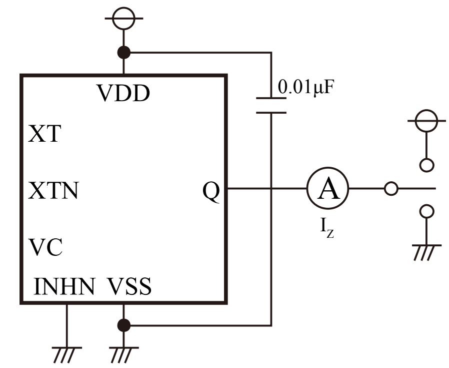
MEASUREMENT CIRCUIT 3

Measurement Parameter: V_{IH}, V_{IL}



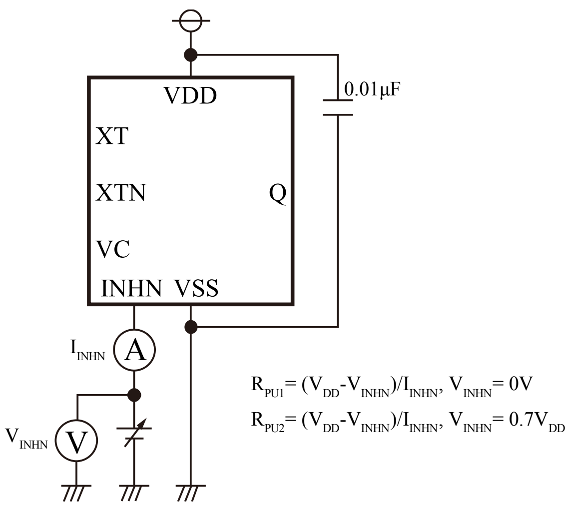
MEASUREMENT CIRCUIT 4

Measurement Parameter: I_Z



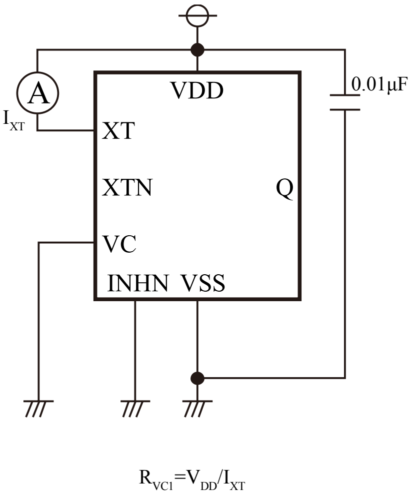
MEASUREMENT CIRCUIT 5

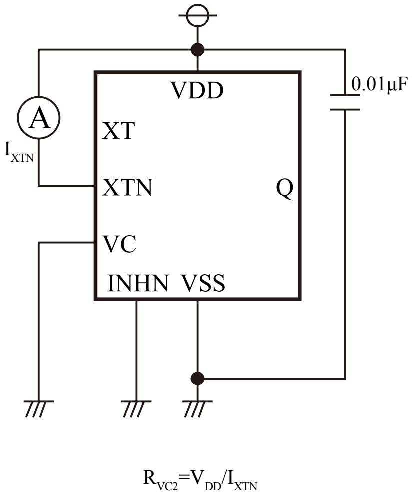
Measurement Parameter: R_{PU1}, R_{PU2}



MEASUREMENT CIRCUIT 6

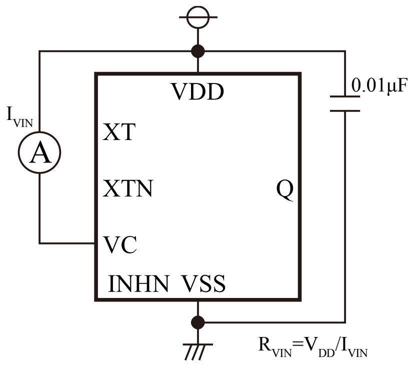
Measurement Parameter: R_{VC1}, R_{VC2}





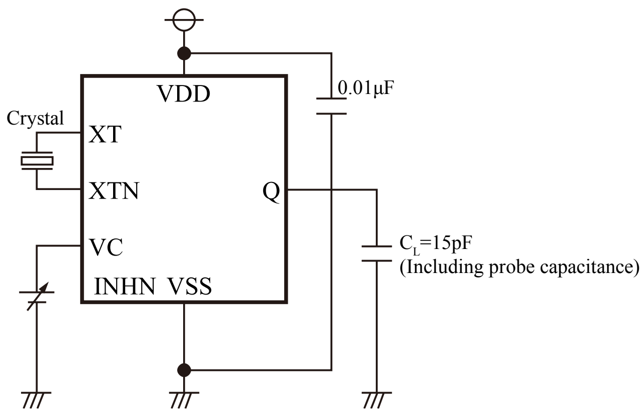
MEASUREMENT CIRCUIT 7

Measurement Parameter: R_{VIN}



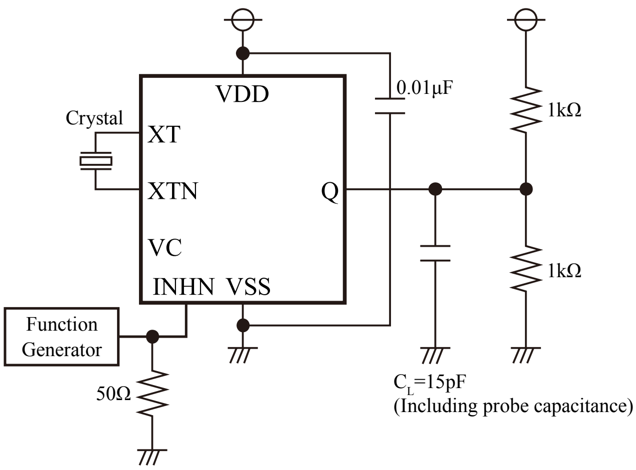
MEASUREMENT CIRCUIT 8

Measurement Parameter: DUTY, t_r, t_f, Pulling Range, CL_{OSC}, V_{TOP}, T_{BASE}



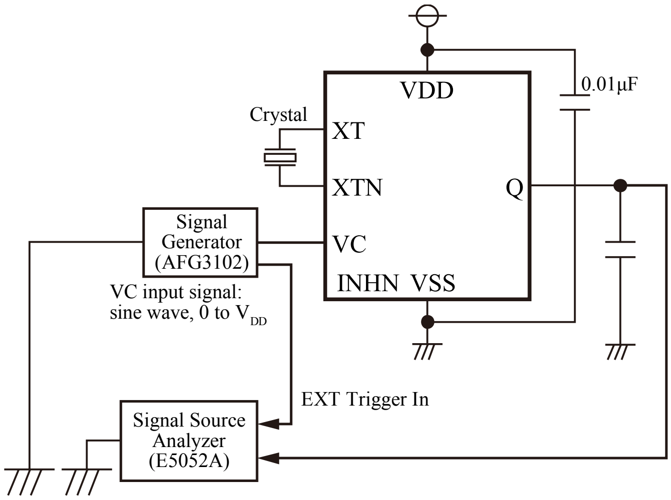
MEASUREMENT CIRCUIT 9

Measurement Parameter: t_{OE}, t_{OD}



MEASUREMENT CIRCUIT 10

Measurement Parameter: F_M



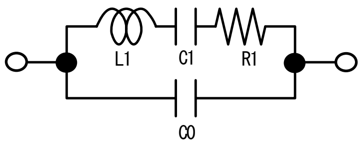
REFERENCE DATA

The following characteristics are measured using the crystal below. Note that the characteristics will vary with the crystal used.

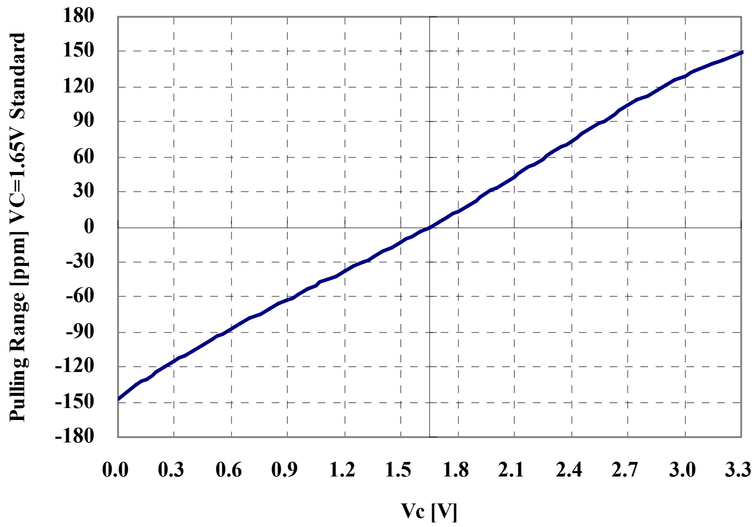
Crystal used for measurement

Parameter	5410Ax	5410Bx
f_s(MHz)	39.98946	61.40941
C0(pF)	1.3	3.2
γ(=C0/C1)	330	350

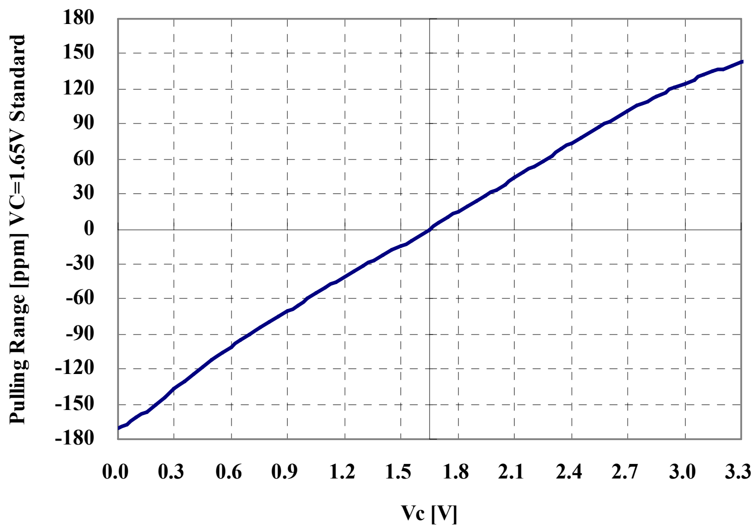
Crystal parameters



Frequency Pulling Range



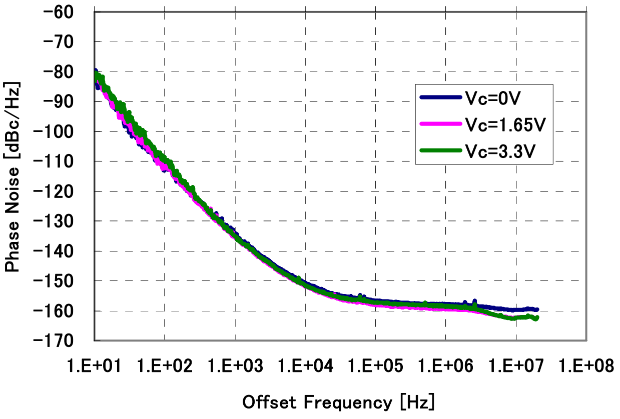
[5410Ax] V_{DD}=3.3V, T_a=25°C, f_{OSC}=40MHz, V_C=1.65V



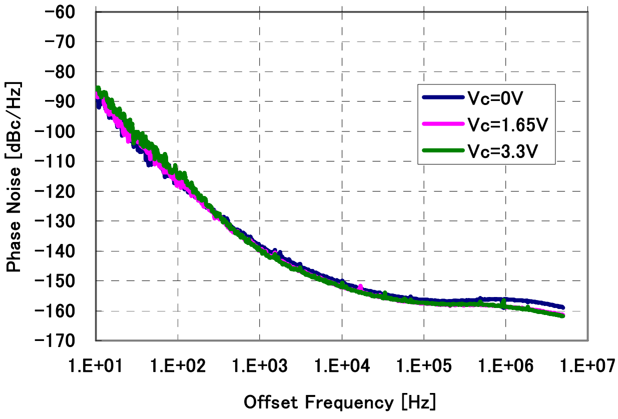
[5410Bx] V_{DD}=3.3V, T_a=25°C, f_{OSC}=61.44MHz, V_C=1.65V

Refer to “MEASUREMENT CIRCUIT8” for measurement circuit diagram.

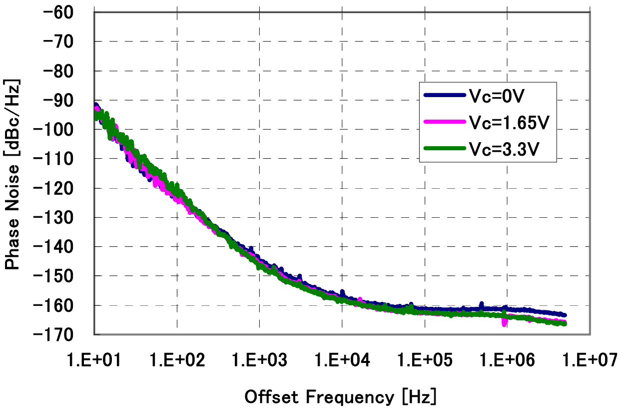
Phase Noise



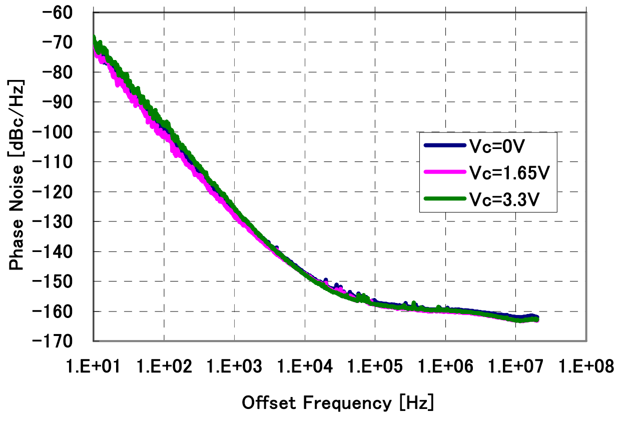
[5410A1] V_{DD}=3.3V, T_a=25°C, f_{OSC}=40MHz, f_{OUT}=40MHz



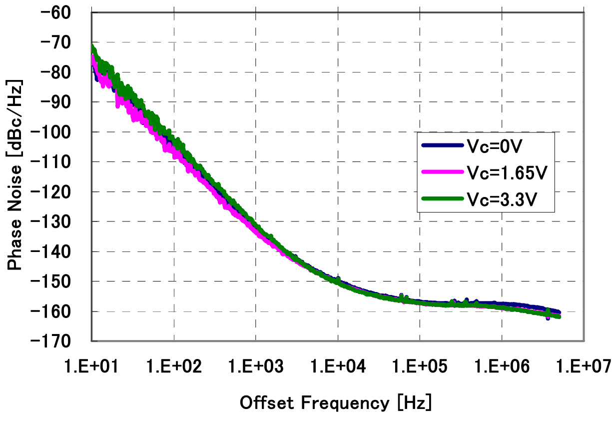
[5410A2] V_{DD}=3.3V, T_a=25°C, f_{OSC}=40MHz, f_{OUT}=20MHz



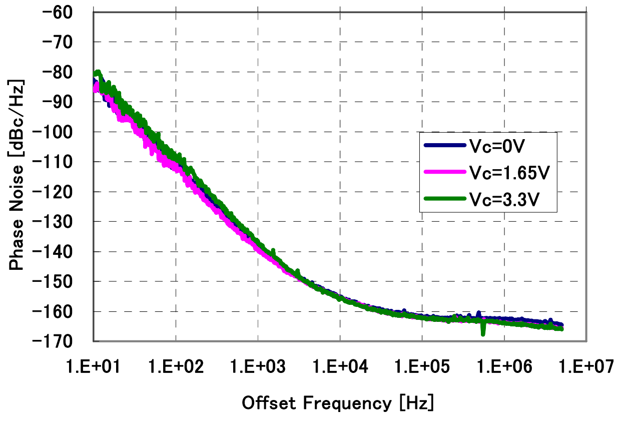
[5410A3] V_{DD}=3.3V, T_a=25°C, f_{OSC}=40MHz, f_{OUT}=10MHz



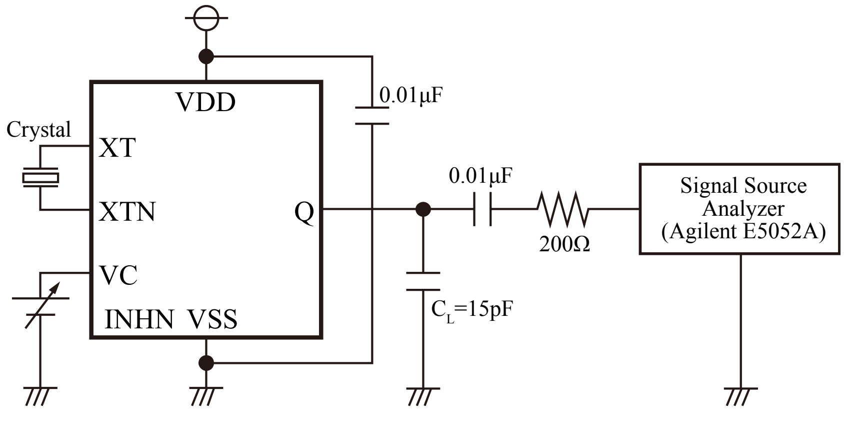
[5410B1] V_{DD}=3.3V, T_a=25°C, f_{OSC}=61.44MHz, f_{OUT}=61.44MHz



[5410B2] V_{DD}=3.3V, T_a=25°C, f_{OSC}=61.44MHz, f_{OUT}=30.72MHz

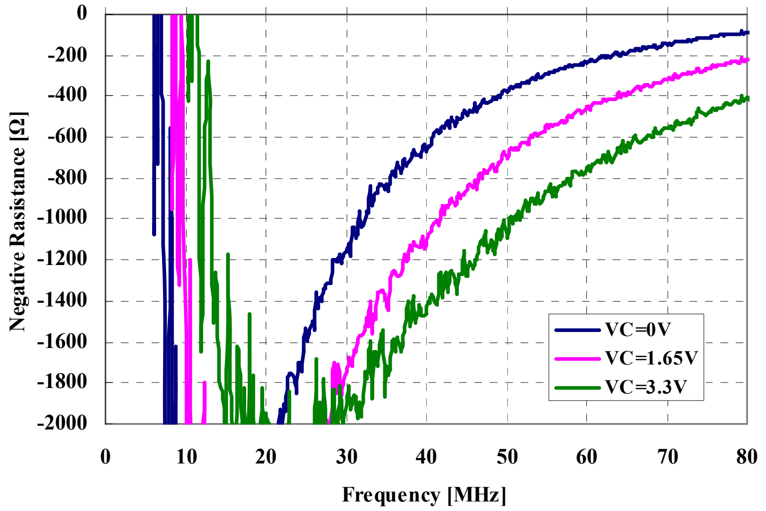


[5410B3] V_{DD}=3.3V, T_a=25°C, f_{OSC}=61.44MHz, f_{OUT}=15.36MHz

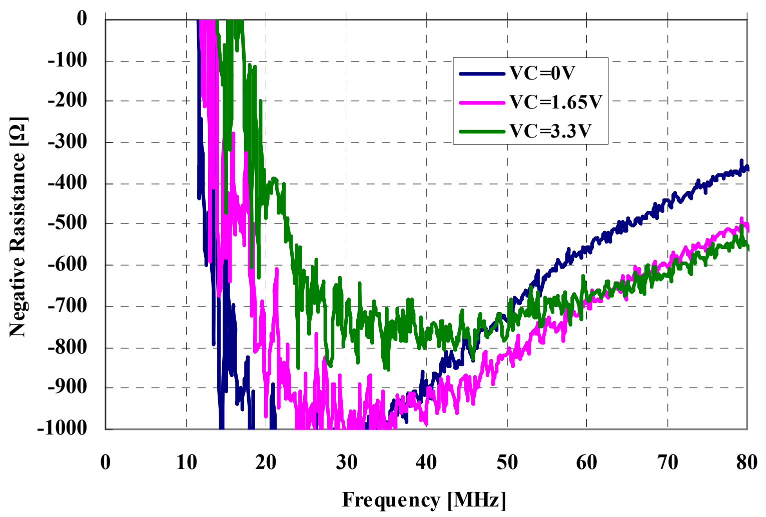


Measurement circuit diagram

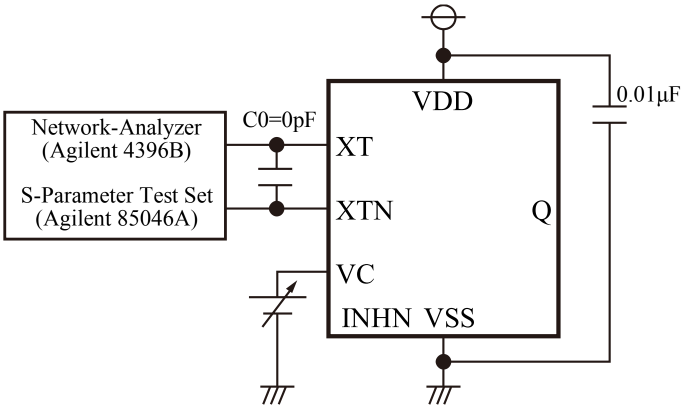
Negative Resistance



[5410Ax] V_{DD}=3.3V, T_a=25°C, C0=0pF, boot



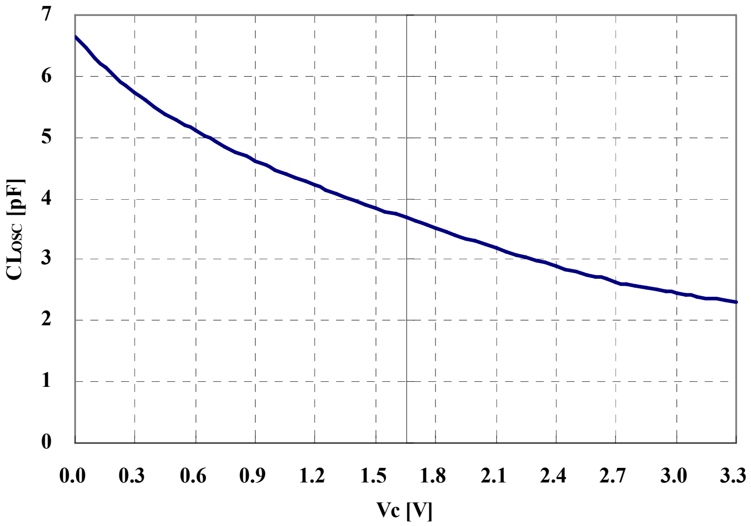
[5410Bx] V_{DD}=3.3V, T_a=25°C, C0=0pF, boot



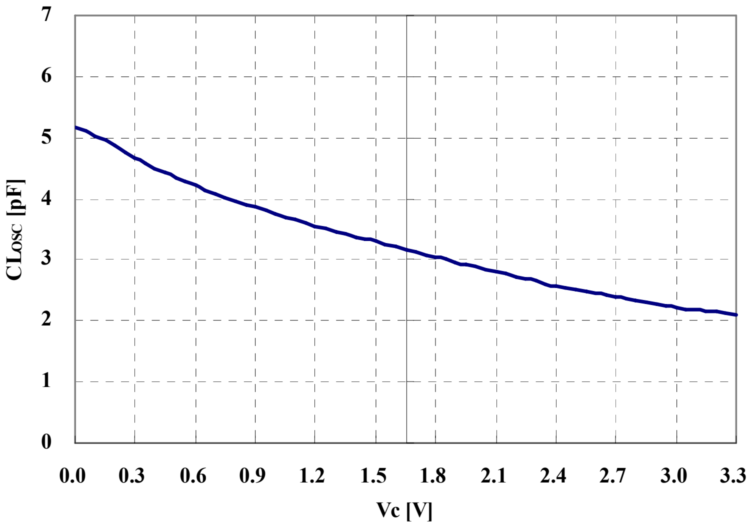
Measurement circuit diagram

They were performed with Agilent 4396B using the NPC test jig.
They may vary in a measurement jig, and measurement environment.

Equivalent Capacity (CL_{OSC}) of Oscillation Circuit



[5410Ax] V_{DD}=3.3V, T_a=25°C, f_{OSC} =40MHz



[5410Bx] V_{DD}=3.3V, T_a=25°C, f_{OSC} =61.44MHz

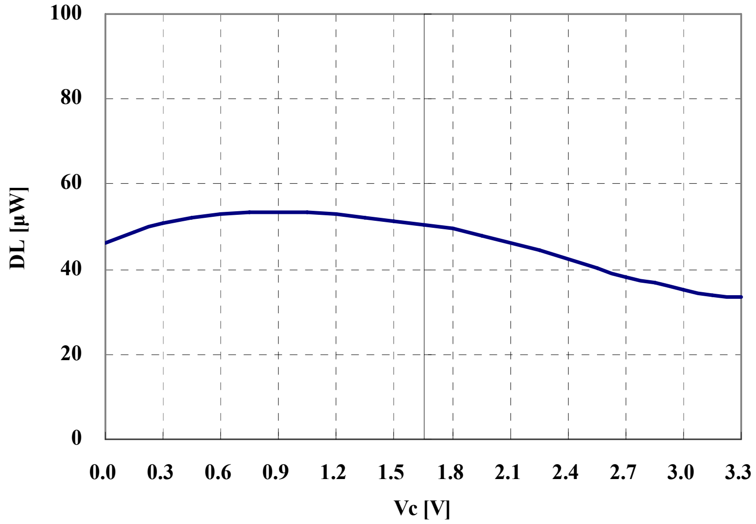
CL_{OSC}: Equivalent capacity of oscillation circuit requested from oscillation frequency

$$CLosc = \frac{C1}{\left(\frac{f_{OSC}}{fs}\right)^2 - 1} - C0$$

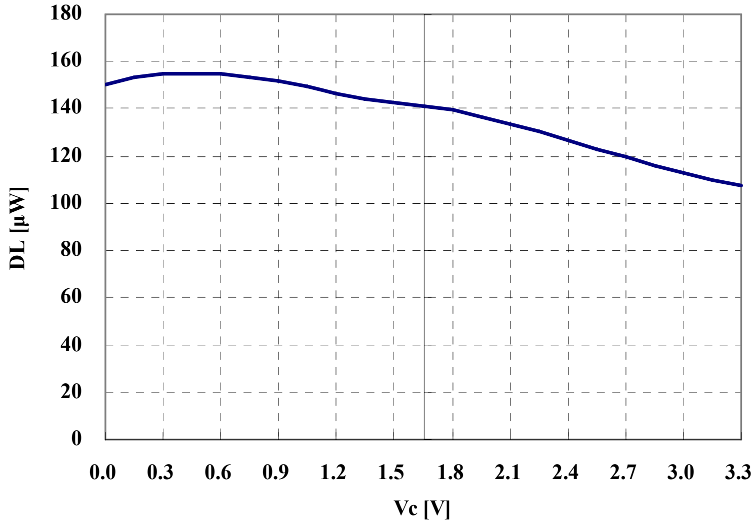
C1: Equivalent series capacity of crystal unit
C0: Equivalent parallel capacity of crystal unit
fs: Series resonating frequency of crystal unit

Refer to "MEASUREMENT CIRCUIT8" for measurement circuit diagram.

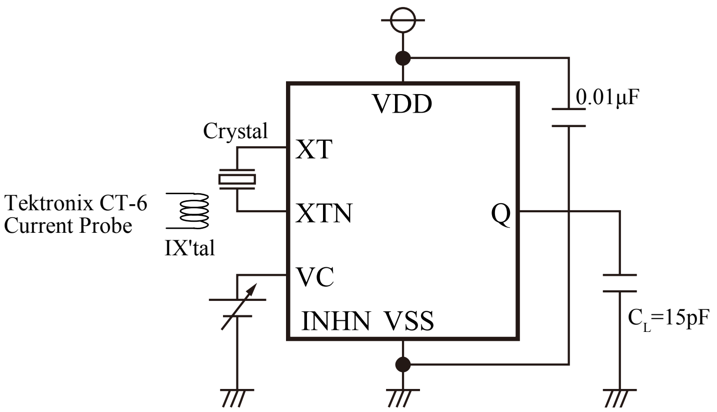
Drive Level



[5410Ax] V_{DD}=3.3V, T_a=25°C, f_{OSC} =40MHz

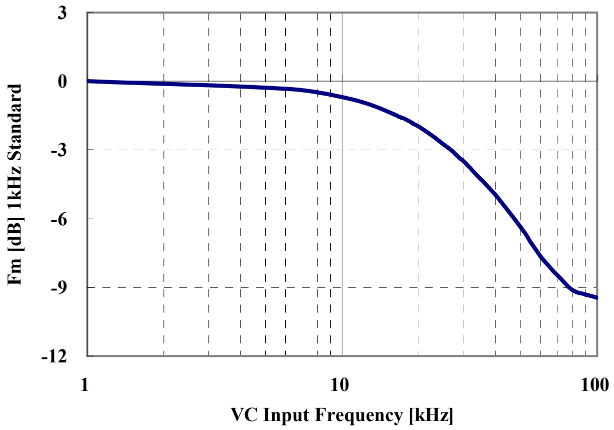


[5410Bx] V_{DD}=3.3V, T_a=25°C, f_{OSC} =61.44MHz

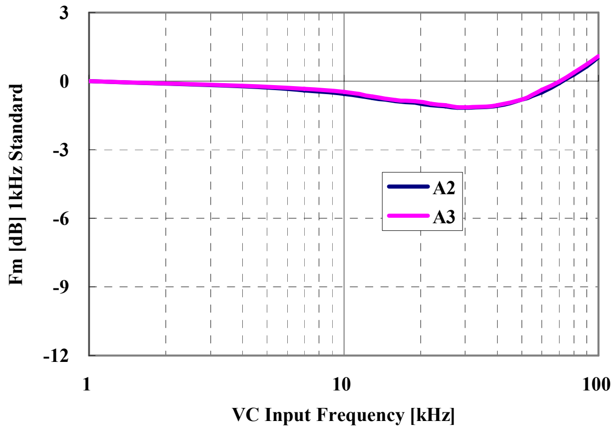


Measurement circuit diagram

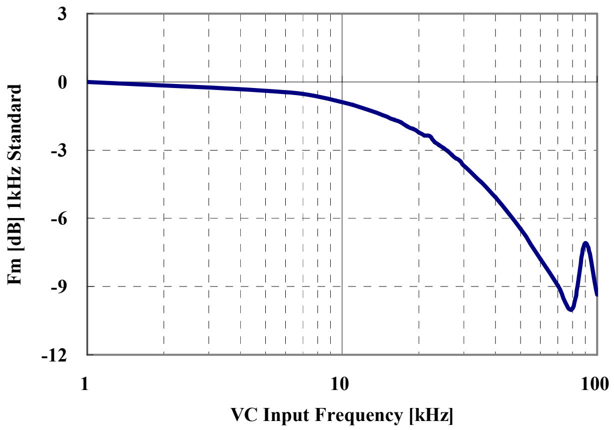
Maximum Modulation Frequency



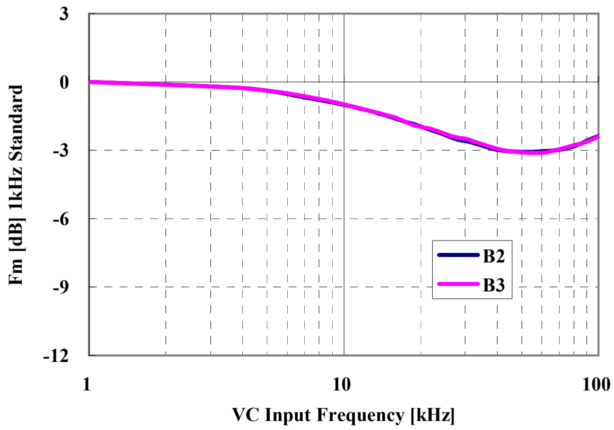
[5410A1] V_{DD}=3.3V, T_a=25°C, f_{OSC} =40MHz



[5410A2,A3] V_{DD}=3.3V, T_a=25°C, f_{OSC} =40MHz



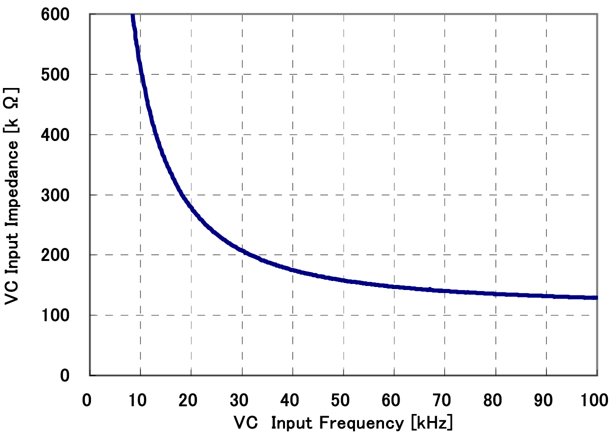
[5410B1] V_{DD}=3.3V, T_a=25°C, f_{OSC} =61.44MHz



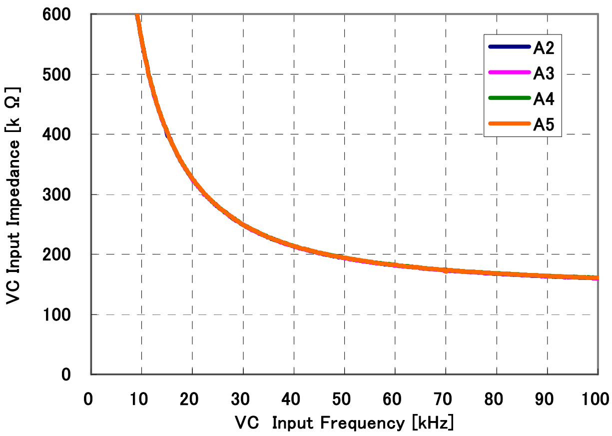
[5410B2,B3] V_{DD}=3.3V, T_a=25°C, f_{OSC} =61.44MHz

Refer to “MEASUREMENT CIRCUIT10” for measurement circuit diagram.

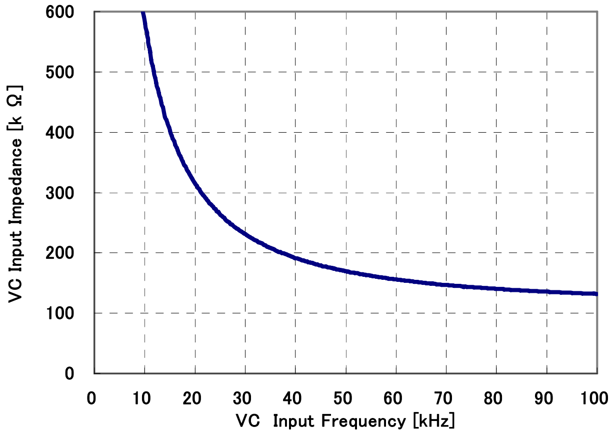
AC Input Impedance (VC pin)



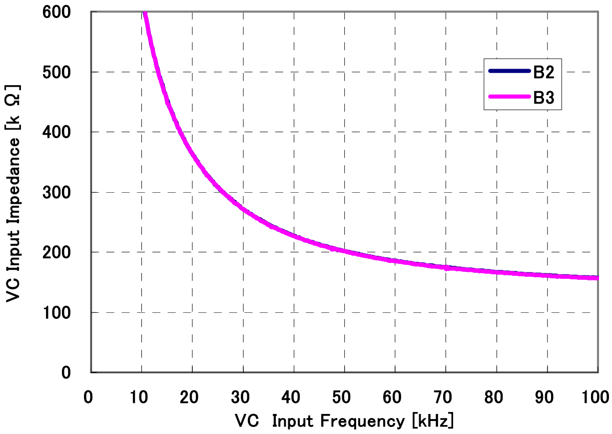
[5410A1] T_a=25°C, V_C=0V



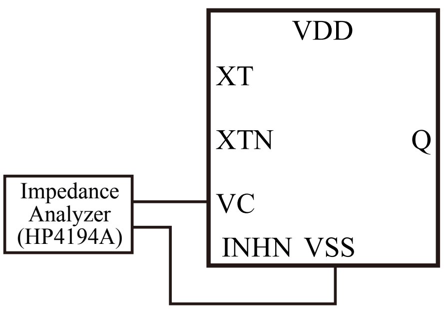
[5410A2,A3,A4,A5] T_a=25°C, V_C=0V



[5410B1] T_a=25°C, V_C=0V



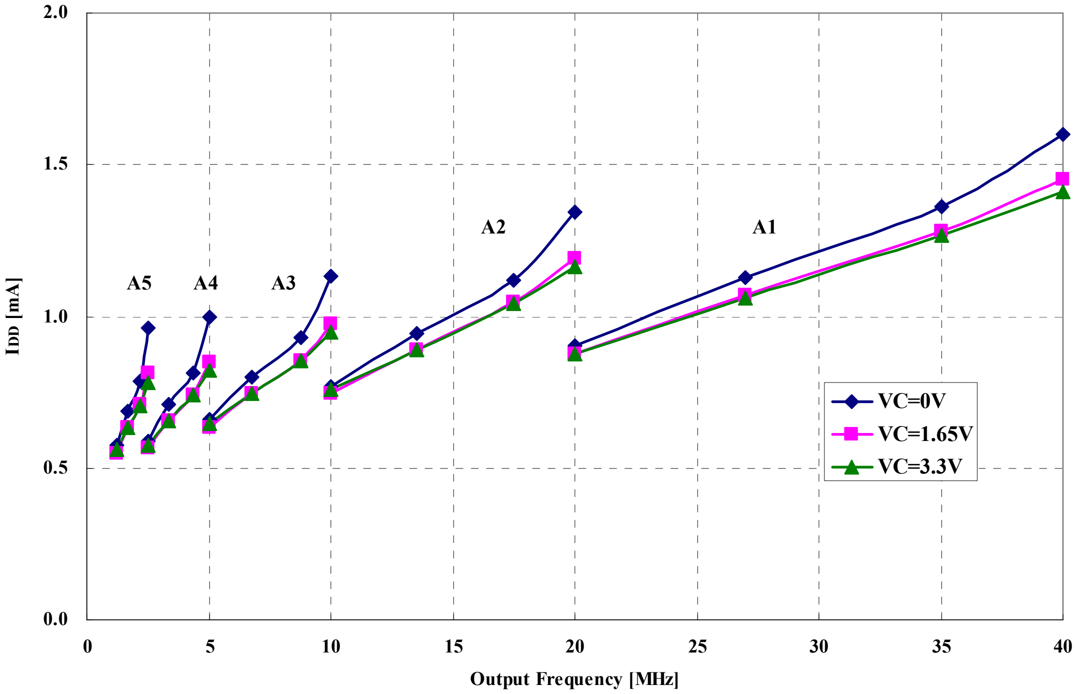
[5410B2,B3] T_a=25°C, V_C=0V



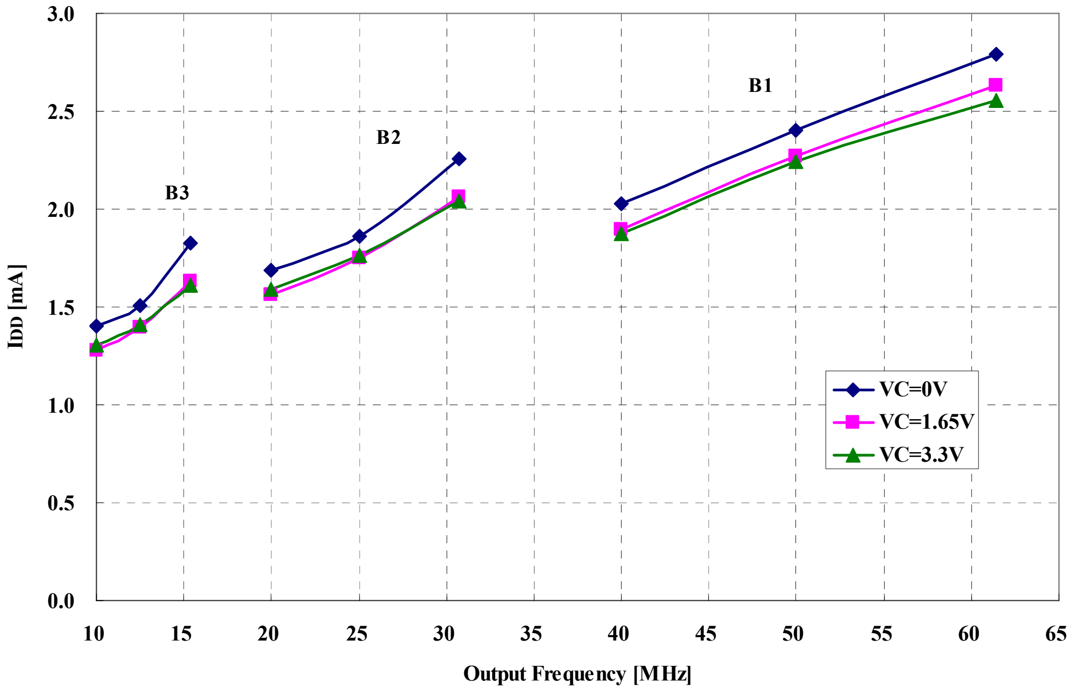
VC input signal: 1kHz to 100kHz, 0.1V_{p-p}

Measurement circuit diagram

Operating Current Consumption



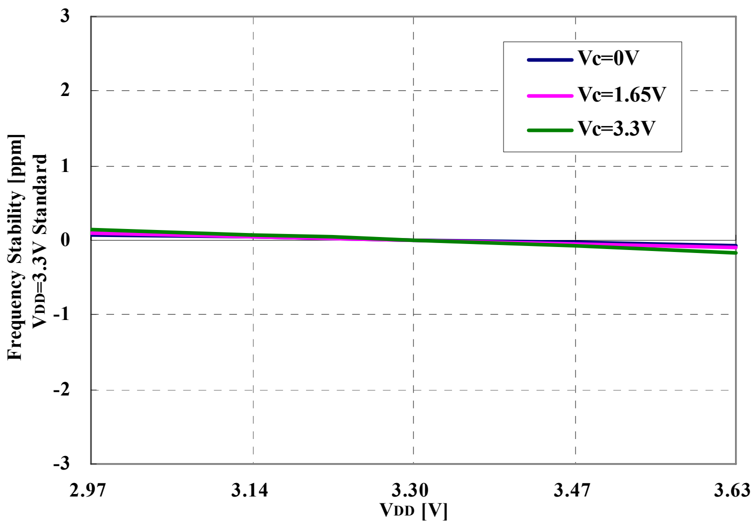
[5410Ax] V_{DD}=3.3V, T_a=25°C



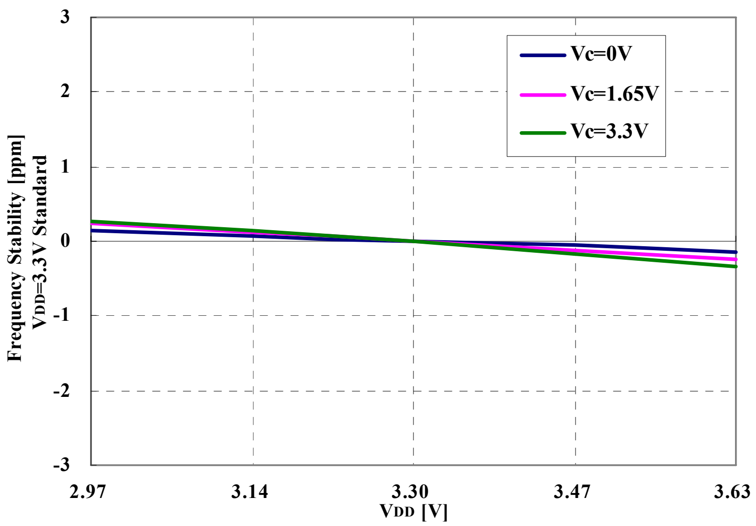
[5410Bx] V_{DD}=3.3V, T_a=25°C

Refer to "MEASUREMENT CIRCUIT1" for measurement circuit diagram.

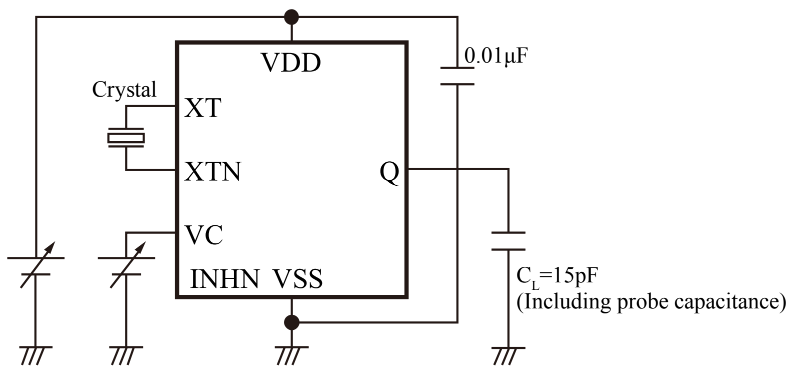
Frequency Deviation by Voltage



[5410Ax] V_{DD}=3.3V, T_a=25°C, f_{OSC} =40MHz

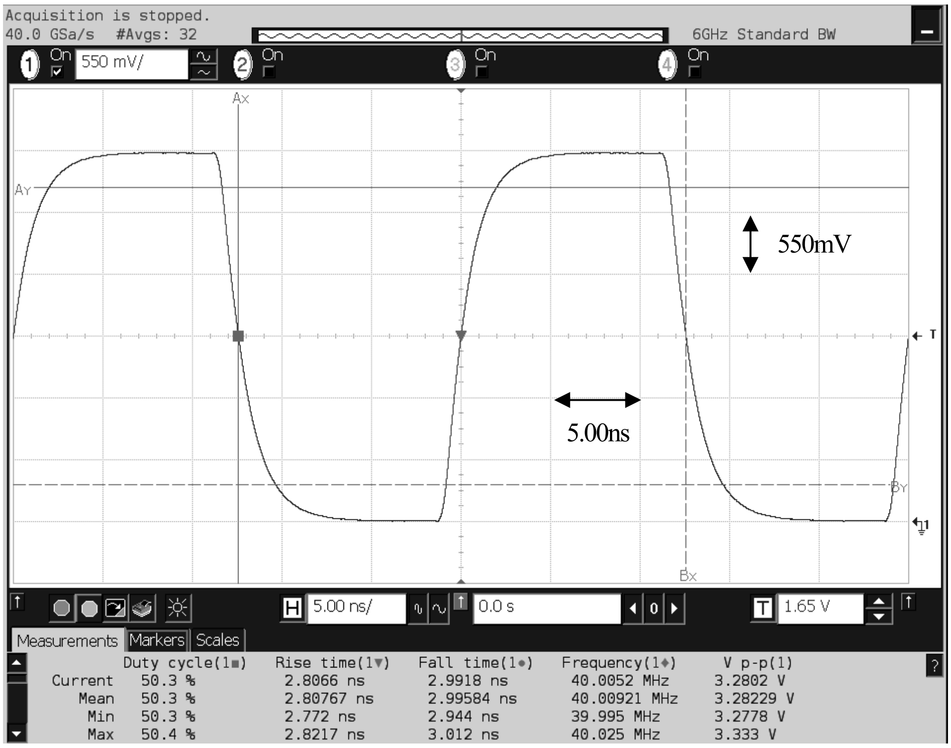


[5410Bx] V_{DD}=3.3V, T_a=25°C, f_{OSC} =61.44MHz

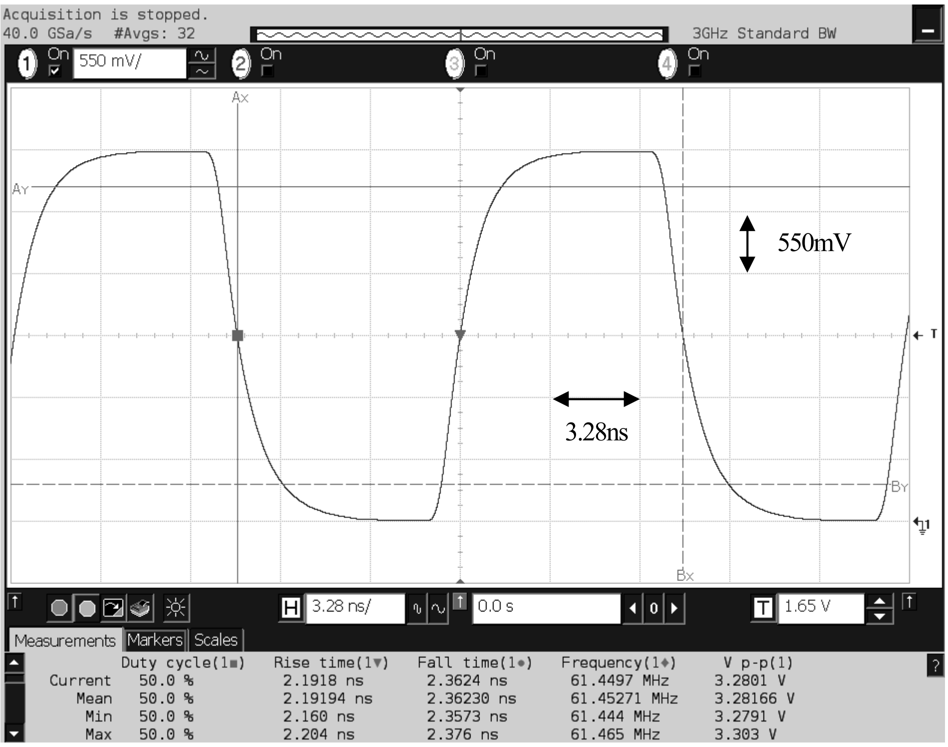


Measurement circuit diagram

Output Waveform



[5410A1] V_{DD}=3.3V, V_C=1.65V, T_a=25°C, f_{OSC} =40MHz, C_L=15pF



[5410B1] V_{DD}=3.3V, V_C=1.65V, T_a=25°C, f_{OSC} =61.44MHz, C_L=15pF

Refer to “MEASUREMENT CIRCUIT8” for measurement circuit diagram.

Measurement equipment: Oscilloscope Agilent DSO80604B

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