2 Mbit / 3 Mbit / 4 Mbit / 8 Mbit Firmware Hub

SST49LF002A / SST49LF003A / SST49LF004A / SST49LF008A

Advance Information

FEATURES:

- **Firmware Hub for Intel 8xx Chipsets**
- **2 Mbit, 3 Mbit, 4 Mbit, or 8 Mbit SuperFlash memory array for code/data storage**
  - SST49LF002A: 256K x8 (2 Mbit)
  - SST49LF003A: 384K x8 (3 Mbit)
  - SST49LF004A: 512K x8 (4 Mbit)
  - SST49LF008A: 1024K x8 (8 Mbit)
- **Flexible Erase Capability**
  - Uniform 4 KByte Sectors
  - Uniform 16 KByte overlay blocks for SST49LF002A
  - Uniform 64 KByte overlay blocks for SST49LF003A/004A/008A
  - Top Boot Block protection
    - 16 KByte for SST49LF002A
    - 64 KByte for SST49LF003A/004A/008A
  - Chip-Erase for PP Mode Only
- **Single 3.0-3.6V Read and Write Operations**
- **Superior Reliability**
  - Endurance:100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Read Current: 6 mA (typical)
  - Standby Current: 10 µA (typical)
- **Fast Sector-Erase/Byte-Program Operation**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14 µs (typical)
  - Chip Rewrite Time:
    SST49LF002A: 4 seconds (typical)
    SST49LF003A: 6 seconds (typical)
    SST49LF004A: 8 seconds (typical)
    SST49LF008A: 15 seconds (typical)
  - Single-pulse Program or Erase
  - Internal timing generation
- **Two Operational Modes**
  - Firmware Hub Interface (FWH) Mode for in-system operation
  - Parallel Programming (PP) Mode for fast production programming
- **Firmware Hub Hardware Interface Mode**
  - 5-signal communication interface supporting byte Read and Write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write protect for entire chip and/or top Boot Block
  - Block Locking Register for all blocks
  - Standard SDP Command Set
  - Data# Polling and Toggle Bit for End-of-Write detection
  - 5 GPI pins for system design flexibility
  - 4 ID pins for multi-chip selection
- **Parallel Programming (PP) Mode**
  - 11-pin multiplexed address and 8-pin data I/O interface
  - Supports fast In-System or PROM programming for manufacturing
- **CMOS and PCI I/O Compatibility**
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)

PRODUCT DESCRIPTION

The SST49LF00xA flash memory devices are designed to be read-compatible with the Intel 82802 Firmware Hub (FWH) device for PC-BIOS application. It provides protection for the storage and update of code and data in addition to adding system design flexibility through five general purpose inputs. Two interface modes are supported by the SST49LF00xA: Firmware Hub (FWH) Interface Mode for In-System programming and Parallel Programming (PP) Mode for fast factory programming of PC-BIOS applications.

The SST49LF00xA flash memory devices are manufactured with SST's proprietary, high performance SuperFlash Technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST49LF00xA devices significantly improve performance and reliability, while lowering power consumption. The SST49LF00xA devices write (Program or Erase) with a single 3.0-3.6V power supply. It uses less energy during Erase and Program than alternative flash memory technologies. The total energy consumed is a function of the applied voltage, current and time of application. Since for

any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies. The SST49LF00xA products provide a maximum Byte-Program time of 20 µsec. The entire memory can be erased and programmed byte-by-byte typically in 15 seconds for an 8-Mbit device, when using status detection features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. The SuperFlash technology provides fixed Erase and Program time, independent of the number of Erase/Program cycles that have performed. Therefore the system software or hardware does not have to be calibrated or correlated to the cumulated number of Erase/Program cycles as is necessary with alternative flash memory technologies, whose Erase and Program time increase with accumulated Erase/Program cycles.

To protect against inadvertent write, the SST49LF00xA devices employ hardware and software data (SDP) protection schemes. It is offered with typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

To meet high density, surface mount requirements, the SST49LF00xA device is offered in 32-lead TSOP and 32-lead PLCC packages. See Figures 7 and 8 for pinouts and Table 8 for pin descriptions.

Mode Selection and Description

The SST49LF00xA flash memory devices can operate in two distinct interface modes: the Firmware Hub Interface (FWH) mode and the Parallel Programming (PP) mode. The IC (Interface Configuration pin) is used to set the interface mode selection. If the IC pin is set to logic High, the device is in PP mode; while if the IC pin is set Low, the device is in the FWH mode. The IC selection pin must be configured prior to device operation. The IC pin is internally pulled down if the pin is not connected. In FWH mode, the device is configured to interface with its host using Intel's Firmware Hub proprietary protocol. Communication between Host and the SST49LF00xA occurs via the 4-bit I/O communication signals, FWH [3:0] and the FWH4. In PP mode, the device is programmed via an 11-bit address and an 8-bit data I/O parallel signals. The address inputs are multiplexed in row and column selected by control signal R/C# pin. The column addresses are mapped to the higher internal addresses, and the row addresses are mapped to the lower internal addresses. See the Device Memory Maps in Figures 3 through 6 for address assignments.

FIRMWARE HUB (FWH) MODE

Device Operation

The FWH mode uses a 5-signal communication interface, FWH[3:0] and FWH4, to control operations of the SST49LF00xA. Operations such as Memory Read and Memory Write uses Intel FWH propriety protocol. JEDEC Standard SDP (Software Data Protection) Byte-Program, Sector-Erase and Block-Erase command sequences are incorporated into the FWH memory cycles. Chip-Erase is only available in PP Mode.

The device enters standby mode when FWH4 is high and no internal operation is in progress. The device is in ready mode when FWH4 is low and no activity is on the FWH bus.

Firmware Hub Interface Cycles

Addresses and data are transferred to and from the SST49LF00xA by a series of "fields," where each field contains 4 bits of data. ST49LF00xA supports only single-byte read and writes, and all fields are one clock cycle in length. Field sequences and contents are strictly defined for Read and Write operations. Addresses in this section refer to addresses as seen from the SST49LF00xA's "point of view," some calculation will be required to translate these to the actual locations in the memory map (and vice versa) if multiple memory device is used on the bus. Tables 1 and 2 list the field sequences for Read and Write cycles.

TABLE 1: FWH READ CYCLE

Clock Cycle	Field Name	Field Contents FWH[3:0][1]	FWH[3:0] Direction	Comments
1	START	1101	IN	FWH4 must be active (low) for the part to respond. Only the last start field (before FWH4 transitioning high) should be recognized. The START field contents indicate a FWH memory read cycle.
2	IDSEL	0000 to 1111	IN	Indicates which FWH device should respond. If the to IDSEL (ID select) field matches the value ID[3:0], then that particular device will respond to the whole bus cycle.
3-9	IMADDR	YYYY	IN	These seven clock cycles make up the 28-bit memory address. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first.
10	IMSIZE	0000 (1 byte)	IN	A field of this size indicates how many bytes will be or transferred during multi-byte operations. The SST49LF00xA will only support single-byte operation. IMSIZE=0000b
11	TAR0	1111	IN then Float	In this clock cycle, the master (Intel ICH) has driven the bus then float to all '1's and then floats the bus, prior to the next clock cycle. This is the first part of the bus "turnaround cycle."
12	TAR1	1111 (float)	Float then OUT	The SST49LF00xA takes control of the bus during this cycle. During the next clock cycle, it will be driving "sync data."
13	RSYNC	0000 (READY)	OUT	During this clock cycle, the FWH will generate a "ready-sync" (RSYNC) indicating that the least-significant nibble of the least-significant byte will be available during the next clock cycle.
14	DATA	YYYY	OUT	YYYY is the least-significant nibble of the least-significant data byte.
15	DATA	YYYY	OUT	YYYY is the most-significant nibble of the least-significant data byte.
16	TAR0	1111	OUT then Float	In this clock cycle, the SST49LF00xA has driven the bus to all ones and then floats the bus prior to the next clock cycle. This is the first part of the bus "turnaround cycle."
17	TAR1	1111 (float)	Float then IN	The master (Intel ICH) resumes control of the bus during this cycle.

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1. Field contents are valid on the rising edge of the present clock cycle.

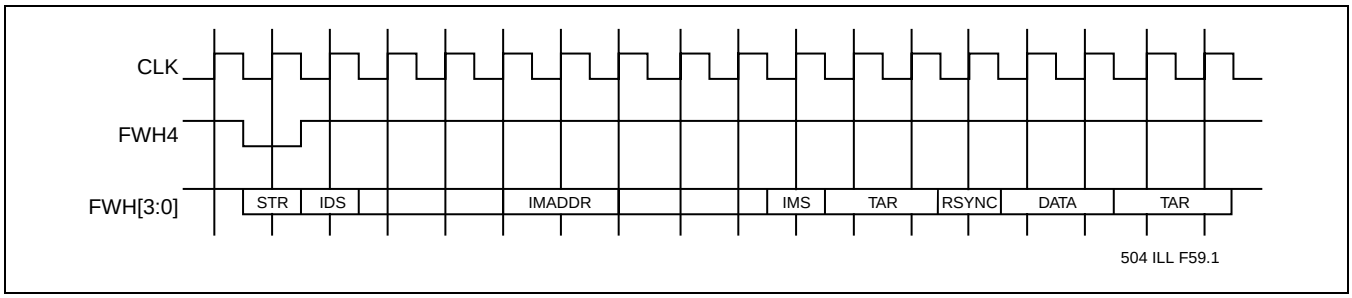

FIGURE 1: SINGLE-BYTE READ WAVEFORMS

TABLE 2: FWH WRITE CYCLE

Clock Cycle	Field Name	Field Contents FWH[3:0][1]	FWH[3:0] Direction	Comments
1	START	1110	IN	FWH4 must be active (low) for the part to respond. Only the last start field (before FWH4 transitioning high) should be recognized. The START field contents indicate a FWH memory read cycle.
2	IDSEL	0000 to 1111	IN	Indicates which SST49LF00xA device should respond. If the IDSEL (ID select) field matches the value ID[3:0], then that particular device will respond to the whole bus cycle.
3-9	IMADDR	YYYY	IN	These seven clock cycles make up the 28-bit memory address. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first.
10	IMSIZE	0000 (1 byte)	IN	This size field indicates how many bytes will be transferred during multi-byte operations. The FWH only supports single-byte writes. IMSIZE=0000b
11	DATA	YYYY	IN	This field is the least-significant nibble of the data byte. This data is either the data to be programmed into the flash memory or any valid flash command.
12	DATA	YYYY	IN	This field is the most-significant nibble of the data byte.
13	TAR0	1111	IN then Float	In this clock cycle, the master (Intel ICH) has driven the then float bus to all ‘1’s and then floats the bus prior to the next clock cycle. This is the first part of the bus “turnaround cycle.”
14	TAR1	1111 (float)	Float then OUT	The SST49LF00xA takes control of the bus during this cycle. During the next clock cycle it will be driving the “sync” data.
15	RSYNC	0000	OUT	The SST49LF00xA outputs the values 0000, indicating that it has received data or a flash command.
16	TAR0	1111	OUT then Float	In this clock cycle, the SST49LF00xA has driven the bus to all then float ‘1’s and then floats the bus prior to the next clock cycle. This is the first part of the bus “turnaround cycle.”
17	TAR1	1111 (float)	Float then IN	The master (Intel ICH) resumes control of the bus during this cycle.

T2.4 504

1. Field contents are valid on the rising edge of the present clock cycle.

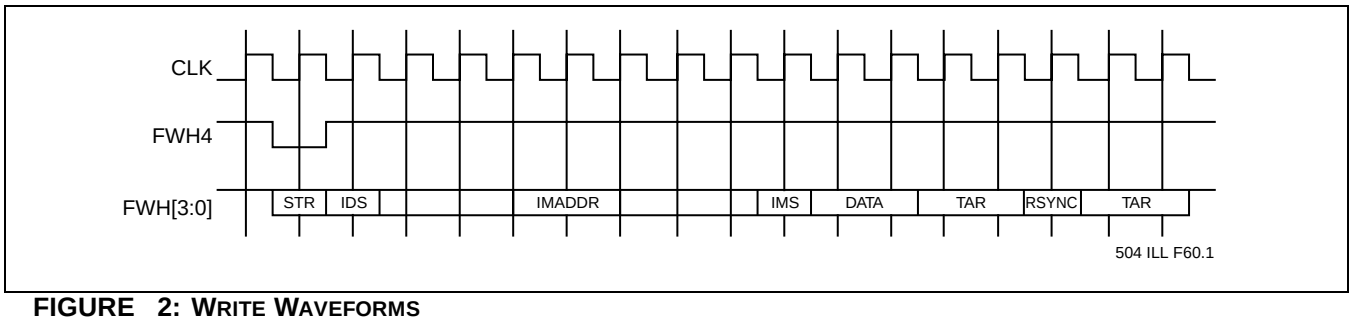

FIGURE 2: WRITE WAVEFORMS

Abort Mechanism

If FWH4 is driven low for one or more clock cycles during a FWH cycle, the cycle will be terminated and the device will wait for the ABORT command. The host must drive the FWH[3:0] with '1111b' (ABORT command) to return the device to ready mode. If abort occurs during the internal write cycle, the data may be incorrectly programmed or erased. It is required to wait for the Write operation to complete prior to initiation of the abort command. It is recommended to check the Write status with Data# Polling (DQ_7) or Toggle Bit (DQ_6) pins. One other option is to wait for the fixed write time to expire.

Response To Invalid Fields

During FWH operations, the FWH will not explicitly indicate that it has received invalid field sequences. The response to specific invalid fields or sequences is as follows:

Address out of range: The FWH address sequence is 7 fields long (28 bits), but only the last five address fields (20 bits) will be decoded by SST49LF00xA.

Address A_{22} has the special function of directing reads and writes to the flash core (A_{22}=1) or to the register space (A_{22}=0).

The SST49LF003A features are equivalent to the SST49LF004A with 128 KByte less memory. For the SST49LF003A, operations beyond the 3-Mbit boundary (below 20000H) are not valid (see Device Memory Map). Invalid address range locations will read as 00H.

Invalid IMSIZE field: If the FWH receives an invalid size field during a Read or Write operation, the device will reset and no operation will be attempted. The SST49LF00xA will not generate any kind of response in this situation. Invalid-size fields for a Read/Write cycle are anything but 0000b.

Once valid START, IDSEL, and IMSIZE fields are received, the SST49LF00xA always will respond to subsequent inputs as if they were valid. As long as the states of device FWH[3:0] and FWH4 are known, the response of the SST49LF00xA to signals received during the FWH cycle should be predictable. The SST49LF00xA will make no attempt to check the validity of incoming flash operation commands.

Device Memory Hardware Write Protection

The Top Boot Lock (TBL#) and Write Protect (WP#) pins are provided for hardware write protection of device memory in the SST49LF00xA. The TBL# pin is used to write protect 16 boot sectors (64 KByte) at the highest flash memory address range for the SST49LF003A/004A/008A and 4 boot sectors (16 KByte) for SST49LF002A. WP# pin write protects the remaining sectors in the flash memory.

An active low signal at the TBL# pin prevents Program and Erase operations of the top boot sectors. When TBL# pin is held high, write protection of the top boot sectors is then determined by the Boot Block Locking register. The WP# pin serves the same function for the remaining sectors of the device memory. The TBL# and WP# pins write protection functions operate independently of one another.

Both TBL# and WP# pins must be set to their required protection states prior to starting a Program or Erase operation. A logic level change occurring at the TBL# or WP# pin during a Program or Erase operation could cause unpredictable results. TBL# and WP# pins cannot be left unconnected.

TBL# is internally ORed with the top Boot Block Locking register. When TBL# is low, the top Boot Block is hardware write protected regardless of the state of the Write-Lock bit for the Boot Block Locking register. Clearing the Write-Protect bit in the register when TBL# is low will have no functional effect, even though the register may indicate that the block is no longer locked.

WP# is internally ORed with the Block Locking register. When WP# is low, the blocks are hardware write protected regardless of the state of the Write-Lock bit for the corresponding Block Locking registers. Clearing the Write-Protect bit in any register when WP# is low will have no functional effect, even though the register may indicate that the block is no longer locked.

Reset

A V_{IL} on INIT# or RST# pin initiates a device reset. INIT# and RST# pins have the same function internally. It is required to drive INIT# or RST# pins low during a system reset to ensure proper CPU initialization.

During a Read operation, driving INIT# or RST# pins low deselects the device and places the output drivers, FWH[3:0], in a high-impedance state. The reset signal must be held low for a minimal duration of time T_{RSTP}. A reset latency will occur if a reset procedure is performed during a Program or Erase operation. See Table 18, Reset Timing Parameters for more information. A device reset during an active Program or Erase will abort the operation and memory contents may become invalid due to data being altered or corrupted from an incomplete Erase or Program operation.

Write Operation Status Detection

The SST49LF00xA device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is incorporated into the FWH Read Cycle. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the SST49LF00xA device is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. Proper status will not be given using Data# Polling if the address is in the invalid range.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop.

Multiple Device Selection

The four ID pins, ID[3:0], allow multiple devices to be attached to the same bus by using different ID strapping in a system. When the SST49LF00xA is used as a boot device, ID[3:0] must be strapped as 0000, all subsequent devices should use a sequential up-count strapping (i.e. 0001, 0010, 0011, etc.). The SST49LF00xA will compare the strapping values, if there is a mismatch, the device will ignore the remainder of the cycle and go into standby mode. For further information regarding FWH device mapping and paging, please refer to the Intel 82801(ICH) I/O Controller Hub documentation. Since there is no ID support in PP Mode, to program multiple devices a stand-alone PROM programmer is recommended.

REGISTERS

There are three types of registers available on the SST49LF00xA, the General Purpose Inputs Register, Block Locking Registers and the JEDEC ID Registers. These registers appear at their respective address location in the 4 GByte system memory map. Unused register locations will read as 00H. Any attempt to read or write any registers during internal Write operation will be ignored.

General Purpose Inputs Register

The GPI_REG (General Purpose Inputs Register) passes the state of FGPI[4:0] pins at power-up on the SST49LF00xA. It is recommended that the FGPI[4:0] pins are in the desired state before FWH4 is brought low for the beginning of the bus cycle, and remain in that state until the end of the cycle. There is no default value since this is a pass-through register. The GPI register for the boot device appears at FFBC0100H in the 4 GByte system memory map, and will appear elsewhere if the device is not the boot device. Register is not available for read when the device is in Erase/Program operation. See Table 3 for the GPI_REG bits and function.

TABLE 3: GENERAL PURPOSE INPUTS REGISTER

Bit	Function	Pin #	
		32-PLCC	32-TSOP
7:5	Reserved	-	-
4	FGPI[4] Reads status of general purpose input pin	30	6
3	FGPI[3] Reads status of general purpose input pin	3	11
2	FGPI[2] Reads status of general purpose input pin	4	12
1	FGPI[1] Reads status of general purpose input pin	5	13
0	FGPI[0] Reads status of general purpose input pin	6	14

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Advance Information

Block Locking Registers

SST49LF00xA provides software controlled lock protection through a set of Block Locking registers. The Block Locking Registers are read/write registers and it is accessible through standard addressable memory locations specified in Table 4 and Table 5. Unused register locations will read as 00H.

TABLE 4: BLOCK LOCKING REGISTERS FOR SST49LF002A[1]

Register	Block Size	Protected Memory Address Package	Memory Map Register Address
T_BLOCK_LK	16K	3FFFFH - 3C000H	FFBF8002H
T_MINUS01_LK	16K 16K 16K	3BFFFH - 38000H 37FFFH - 34000H 33FFFH - 30000H	FFBF0002H
T_MINUS02_LK	16K 16K	2FFFFH - 2C000H 2BFFFH - 28000H	FFBE8002H
T_MINUS03_LK	16K 16K	27FFFH - 24000H 23FFFH - 20000H	FFBE0002H
T_MINUS04_LK	16K 16K	1FFFFH - 1C000H 1BFFFH - 18000H	FFBD8002H
T_MINUS05_LK	16K 16K	17FFFH - 14000H 13FFFH - 10000H	FFBD0002H
T_MINUS06_LK	16K 16K	0FFFFH - 0C000H 0BFFFH - 08000H	FFBC8002H
T_MINUS07_LK	16K 16K	07FFFH - 04000H 03FFFH - 00000H	FFBC0002H

T4.1 504

1. Default value at power up is 01H

TABLE 5: BLOCK LOCKING REGISTERS FOR SST49LF003A/004A/008A[1]

Register	Block Size	Protected Memory Address Range			Memory Map Register Address
		SST49LF003A	SST49LF004A	SST49LF008A	
T_BLOCK_LK	64K	07FFFFH - 070000H	07FFFFH - 070000H	0FFFFFH - 0F0000H	FFBF0002H
T_MINUS01_LK	64K	06FFFFH - 060000H	06FFFFH - 060000H	0EFFFFH - 0E0000H	FFBE0002H
T_MINUS02_LK	64K	05FFFFH - 050000H	05FFFFH - 050000H	0DFFFFH - 0D0000H	FFBD0002H
T_MINUS03_LK	64K	04FFFFH - 040000H	04FFFFH - 040000H	0CFFFFH - 0C0000H	FFBC0002H
T_MINUS04_LK	64K	03FFFFH - 030000H	03FFFFH - 030000H	0BFFFFH - 0B0000H	FFBB0002H
T_MINUS05_LK	64K	02FFFFH - 020000H	02FFFFH - 020000H	0AFFFFH - 0A0000H	FFBA0002H
T_MINUS06_LK	64K		01FFFFH - 010000H	09FFFFH - 090000H	FFB90002H
T_MINUS07_LK	64K		00FFFFH - 000000H	08FFFFH - 080000H	FFB80002H
T_MINUS08_LK	64K			07FFFFH - 070000H	FFB70002H
T_MINUS09_LK	64K			06FFFFH - 060000H	FFB60002H
T_MINUS10_LK	64K			05FFFFH - 050000H	FFB50002H
T_MINUS11_LK	64K			04FFFFH - 040000H	FFB40002H
T_MINUS12_LK	64K			03FFFFH - 030000H	FFB30002H
T_MINUS13_LK	64K			02FFFFH - 020000H	FFB20002H
T_MINUS14_LK	64K			01FFFFH -010000H	FFB10002H
T_MINUS15_LK	64K			00FFFFH - 000000H	FFB00002H

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1. Default value at power up is 01H

TABLE 6: BLOCK LOCKING REGISTER BITS

Reserved Bit [7..2]	Lock-Down Bit [1]	Write-Lock Bit [0]	Lock Status
000000	0	0	Full Access
000000	0	1	Write Locked (Default State at Power-Up)
000000	1	0	Locked Open (Full Access Locked Down)
000000	1	1	Write Locked Down

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Write Lock

The Write-Lock bit, bit 0, controls the lock state described in Table 6. The default Write status of all blocks after power-up is write locked. When bit 0 of the Block Locking register is set, Program and Erase operations for the corresponding block are prevented. Clearing the Write-Lock bit will unprotect the block. The Write-Lock bit must be cleared prior to starting a Program or Erase operation since it is sampled at the beginning of the operation.

The Write-Lock bit functions in conjunction with the hardware Write Lock pin TBL# for the top Boot Block. When TBL# is low, it overrides the software locking scheme. The top Boot Block Locking register does not indicate the state of the TBL# pin.

The Write-Lock bit functions in conjunction with the hardware WP# pin for blocks 0 to 6. When WP# is low, it overrides the software locking scheme. The Block Locking register does not indicate the state of the WP# pin.

Lock Down

The Lock-Down bit, bit 1, controls the Block Locking register as described in Table 6. When in the FWH interface mode, the default Lock Down status of all blocks upon power-up is not locked down. Once the Lock-Down bit is set, any future attempted changes to that Block Locking register will be ignored. The Lock-Down bit is only cleared upon a device reset with RST# or INIT# or power down. Current Lock Down status of a particular block can be determined by reading the corresponding Lock-Down bit. Once a block's Lock-Down bit is set, the Write-Lock bits for that block can no longer be modified, and the block is locked down in its current state of write accessibility.

JEDEC ID Registers

The JEDEC ID registers for the boot device appear at FFBC0000H and FFBC0001H in the 4 GByte system memory map, and will appear elsewhere if the device is not the boot device. Register is not available for read when the device is in Erase/Program operation. Unused register location will read as 00H. Refer to the relevant application note for details. See Table 7 for the device ID code.

PARALLEL PROGRAMMING MODE

Device Operation

Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of WE#. During the software command sequence the row address is latched on the falling edge of R/C# and the column address is latched on the rising edge of R/C#.

Read

The Read operation of the SST49LF00xA device is controlled by OE#. OE# is the output control and is used to gate data from the output pins. Refer to the Read cycle timing diagram, Figure 14, for further details.

Reset

A V_{IL} on RST# pin initiates a device reset.

Byte-Program Operation

The SST49LF00xA device is programmed on a byte-by-byte basis. Before programming, one must ensure that the sector, in which the byte which is being programmed exists, is fully erased. The Byte-Program operation is initiated by executing a four-byte command load sequence for Software Data Protection with address (BA) and data in the last byte sequence. During the Byte-Program operation, the row address (A_{10}-A_0) is latched on the falling edge of R/C# and the column Address (A_{21}-A_{11}) is latched on the rising edge of R/C#. The data bus is latched in the rising edge of WE#. The Program operation, once initiated, will be completed, within 20 µs. See Figure 15 for Program operation timing diagram, Figure 18 for timing waveforms, and Figure 26 for its flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 19 for Sector-Erase timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

Block-Erase Operation

The Block-Erase Operation allows the system to erase the device in 64 KByte uniform block size for the SST49LF003A/SST49LF004A/SST49LF008A and 16 KByte uniform block size for the SST49LF002A. The Block-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Block-Erase command (50H) and block address. The internal Block-Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 20 for timing waveforms. Any commands written during the Block-Erase operation will be ignored.

Chip-Erase

The SST49LF00xA device provides a Chip-Erase operation only in PP Mode, which allows the user to erase the entire memory array to the '1's state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE#. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 10 for the command sequence, Figure 21 for timing diagram, and Figure 29 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

Write Operation Status Detection

The SST49LF00xA device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the SST49LF00xA device is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# pulse for Program operation. For Sector- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# pulse. See Figure 16 for Data# Polling timing diagram and Figure 27 for a flowchart. Proper status will not be given using Data# Polling if the address is in the invalid range.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# pulse for Program operation. For Sector-, Block- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# pulse. See Figure 17 for Toggle Bit timing diagram and Figure 27 for a flowchart.

Data Protection

The SST49LF00xA device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST49LF00xA provides the JEDEC approved Software Data Protection scheme for all data alteration operation, i.e., program and erase. Any Program operation requires the inclusion of a series of three byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six byte load sequence. The SST49LF00xA device is shipped with the Software Data Protection permanently enabled. See Table 10 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within T_{RC}.

Electrical Specifications

The AC and DC specifications for the FWH Interface signals (FWH[3:0], CLK, FWH4, and RST#) as defined in Section 4.2.2 of the *PCI Local Bus Specification, Rev. 2.1*. Refer to Table 11 for the DC voltage and current specifications. Refer to the tables on pages 20 through 24 for the AC timing specifications for Clock, Read/Write, and Reset operations.

Product Identification

The product identification mode identifies the device as the SST49LF00xA and manufacturer as SST.

TABLE 7: PRODUCT IDENTIFICATION

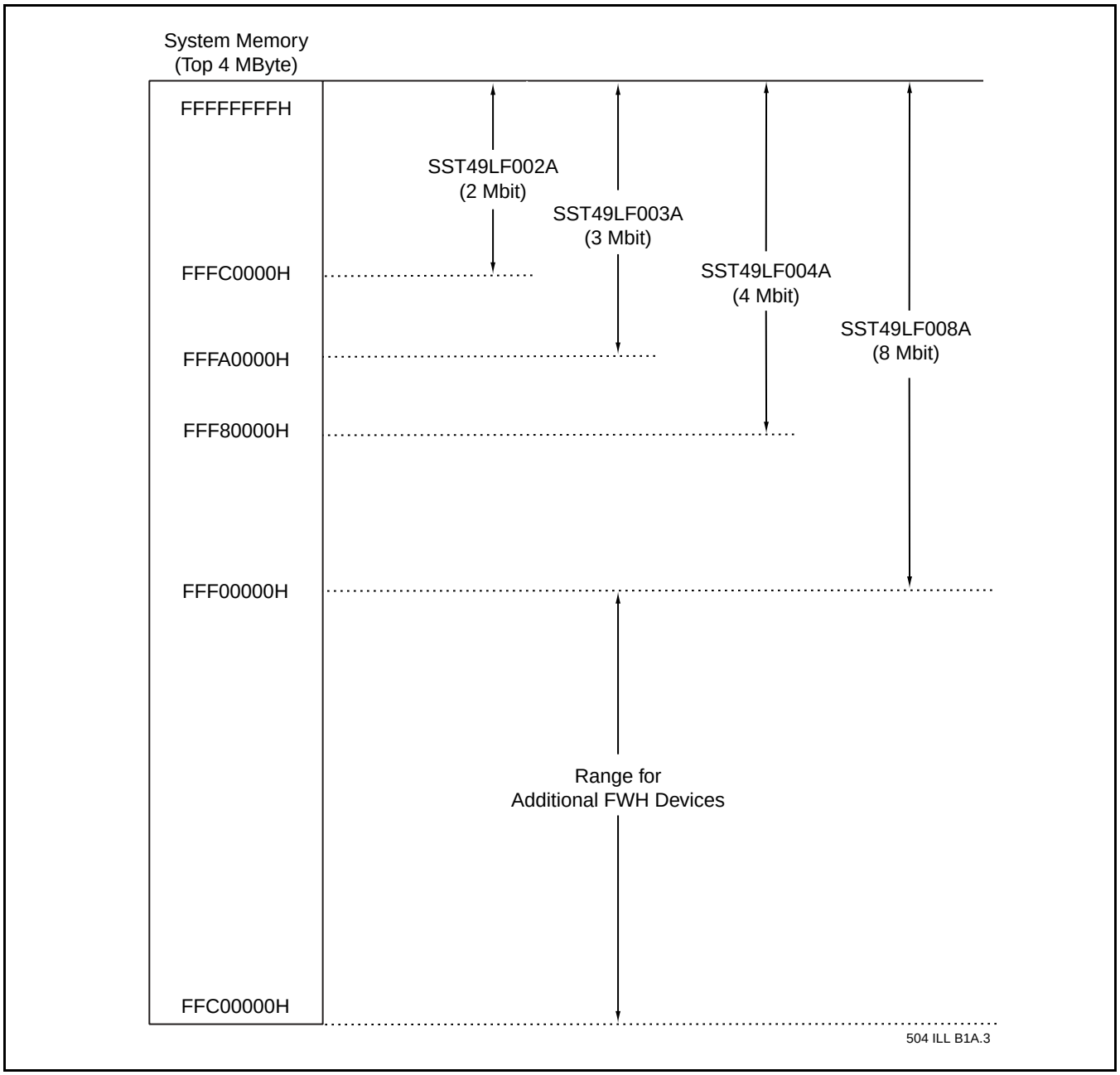
	Byte	Data	JEDEC ID Address Location
Manufacturer's ID	0000H	BFH	FFBC0000H
Device ID			
SST49LF002A	0001H	57H	FFBC0001H
SST49LF003A	0001H	1BH	FFBC0001H
SST49LF004A	0001H	60H	FFBC0001H
SST49LF008A	0001H	5AH	FFBC0001H

T7.5 504

Design Considerations

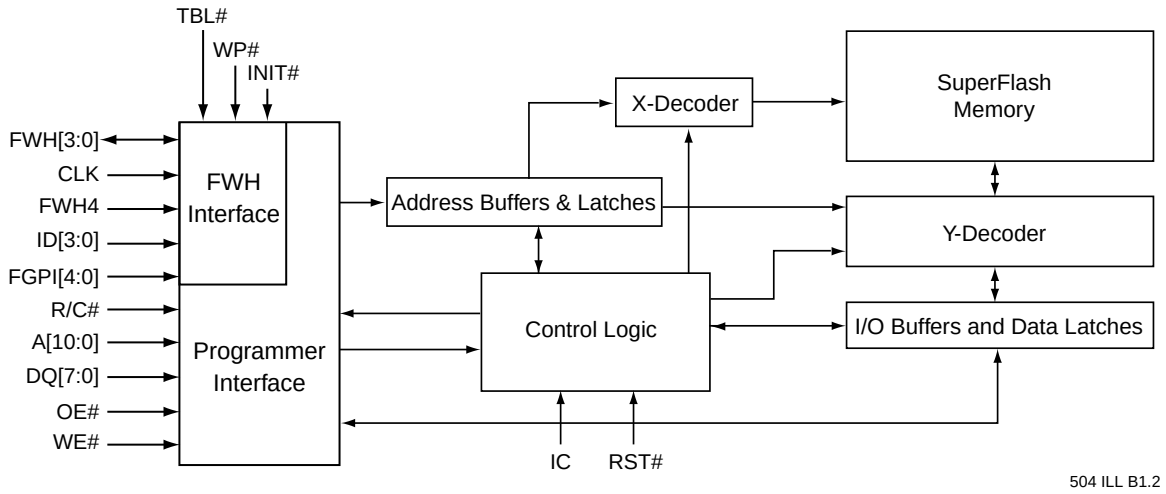
SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS} less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 1 cm of the V_{DD} pin. If you use a socket for programming purposes add an additional 1-10 µF next to each socket.

The RST# pin must remain stable at V_{IH} for the entire duration of an Erase operation. WP# must remain stable at V_{IH} for the entire duration of the Erase and Program operations for non-Boot Block sectors. To write data to the top Boot Block sectors, the TBL# pin must also remain stable at V_{IH} for the entire duration of the Erase and Program operations.



BOOT-CONFIGURATION SYSTEM MEMORY MAP

FUNCTIONAL BLOCK DIAGRAM



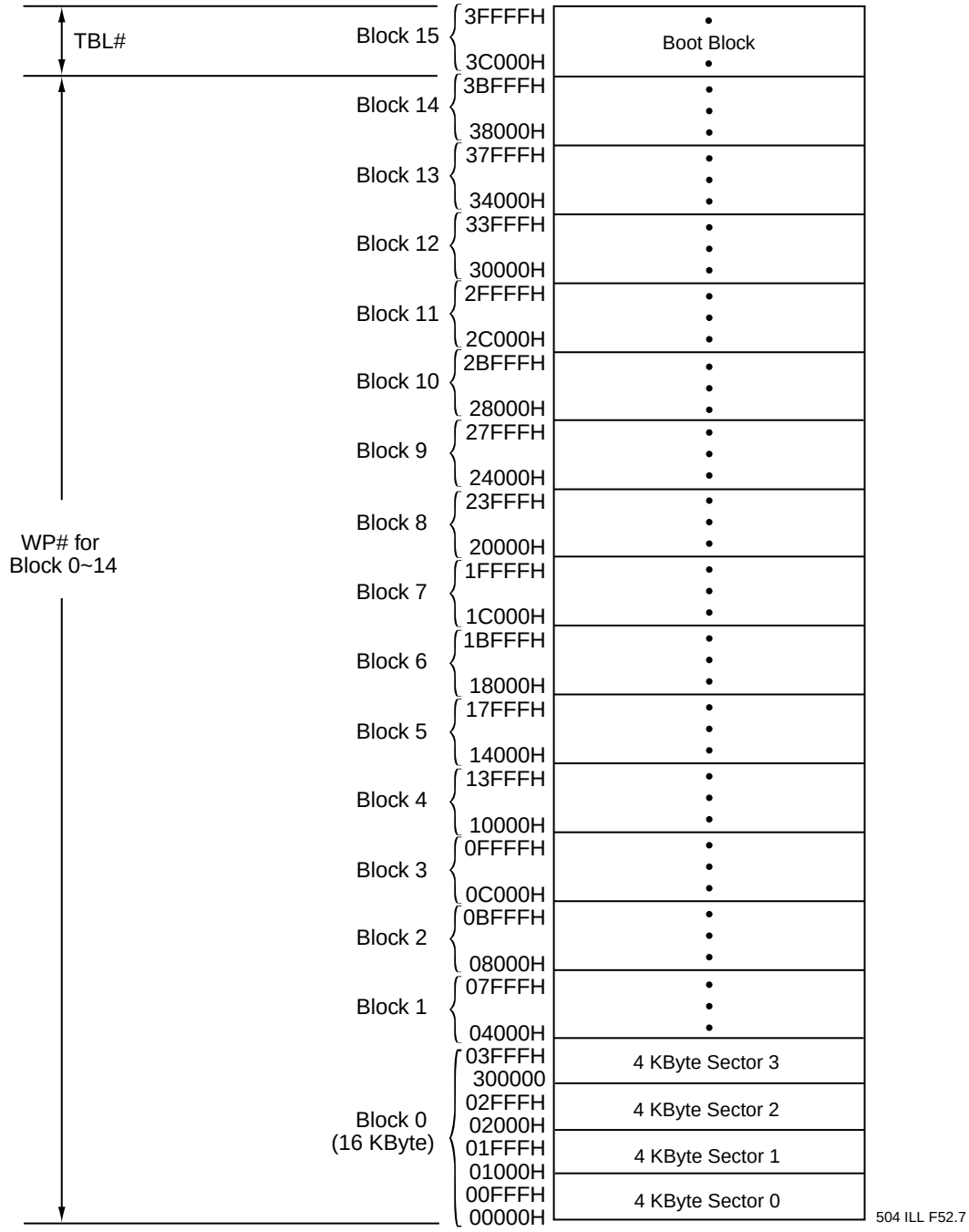
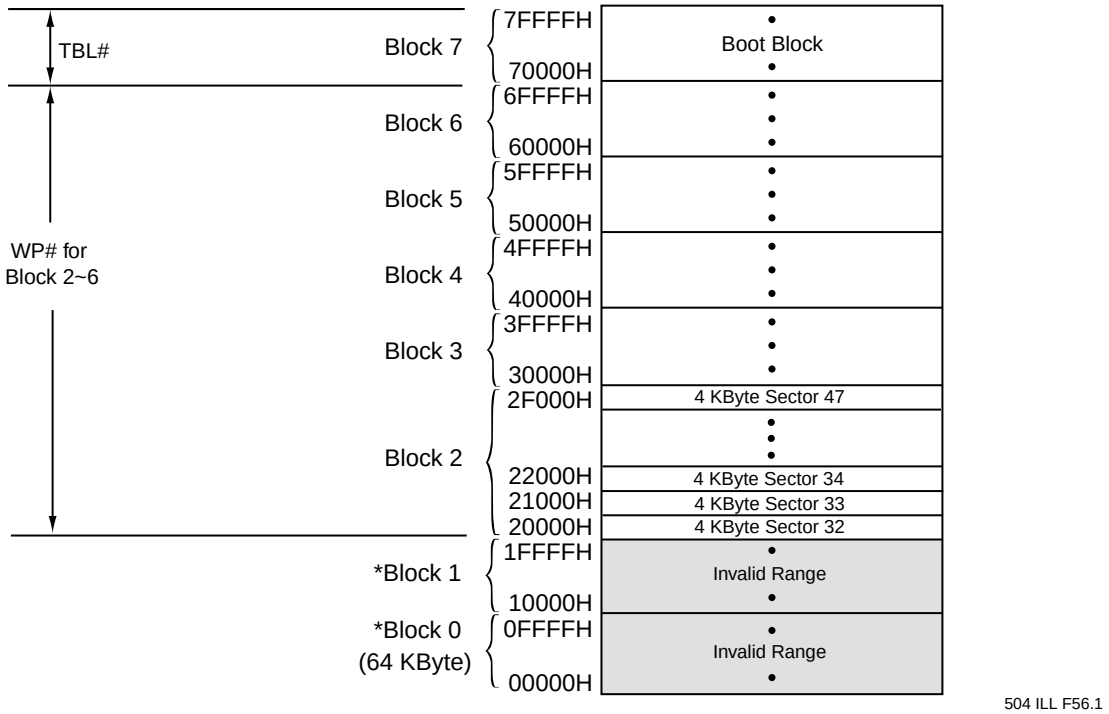


FIGURE 3: DEVICE MEMORY MAP FOR SST49LF002A



* operations to shaded area are not valid.

FIGURE 4: DEVICE MEMORY MAP FOR SST49LF003A

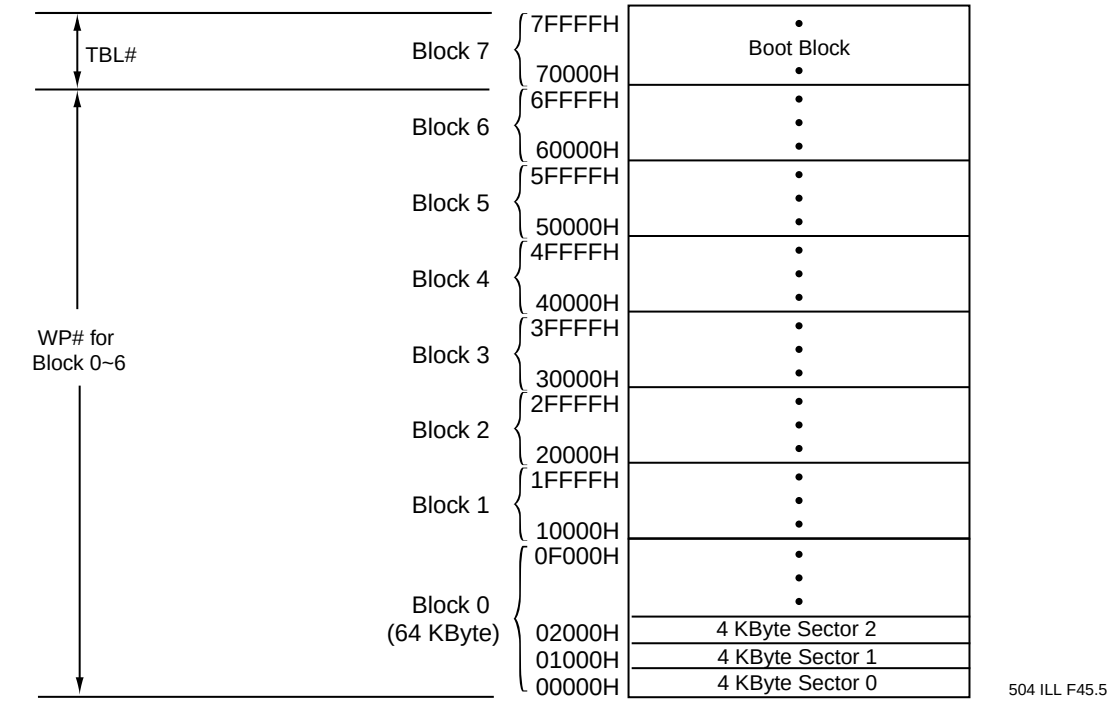


FIGURE 5: DEVICE MEMORY MAP FOR SST49LF004A

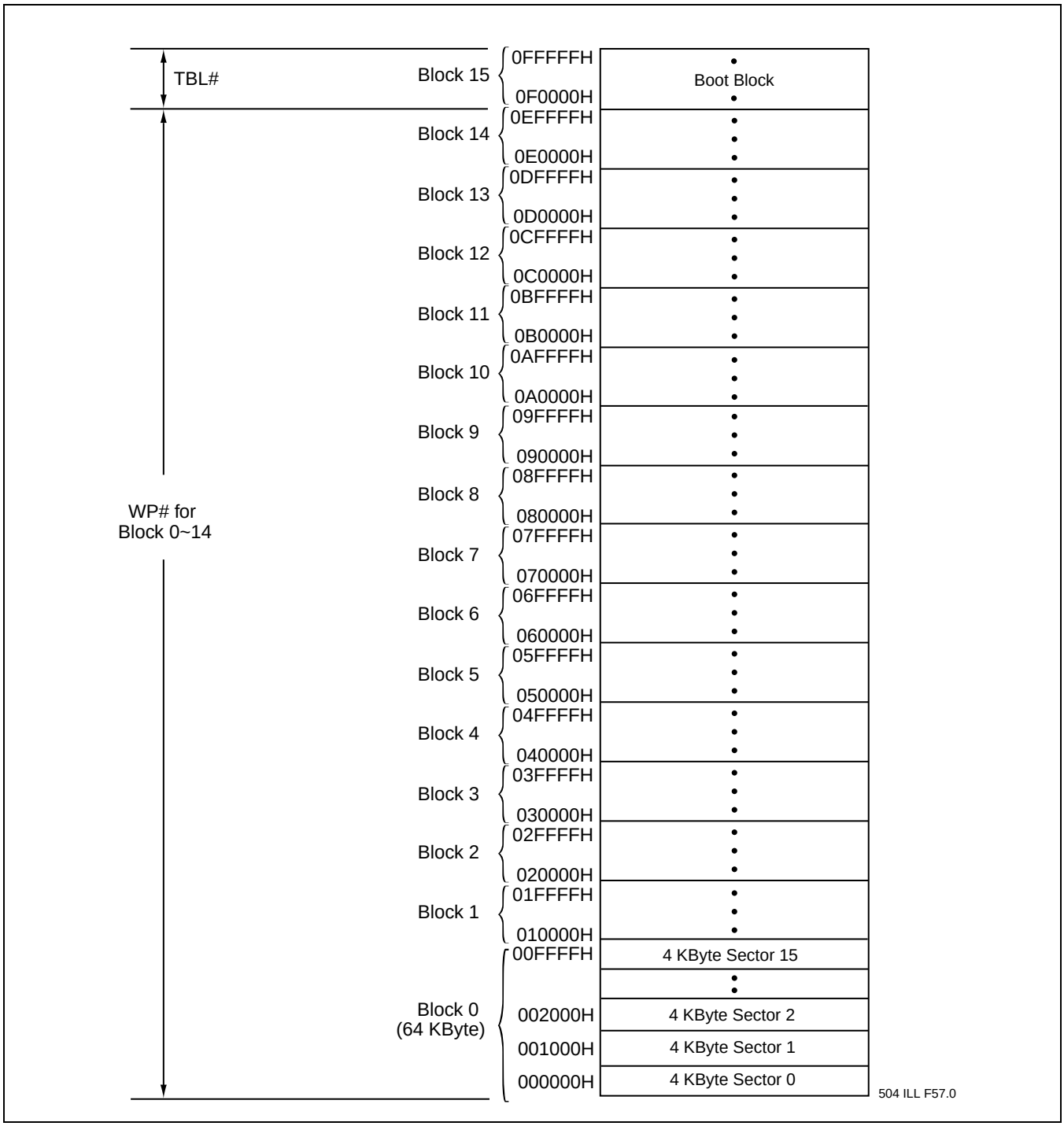


FIGURE 6: DEVICE MEMORY MAP FOR SST49LF008A

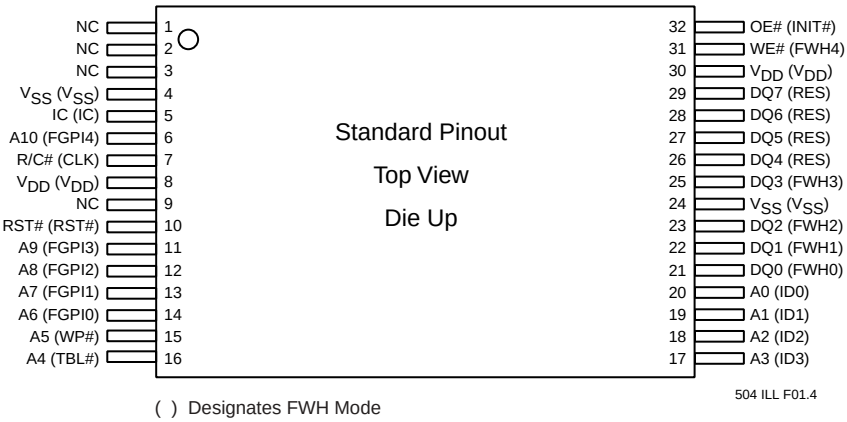


FIGURE 7: PIN ASSIGNMENTS FOR 32-LEAD TSOP (8MM X 14MM)

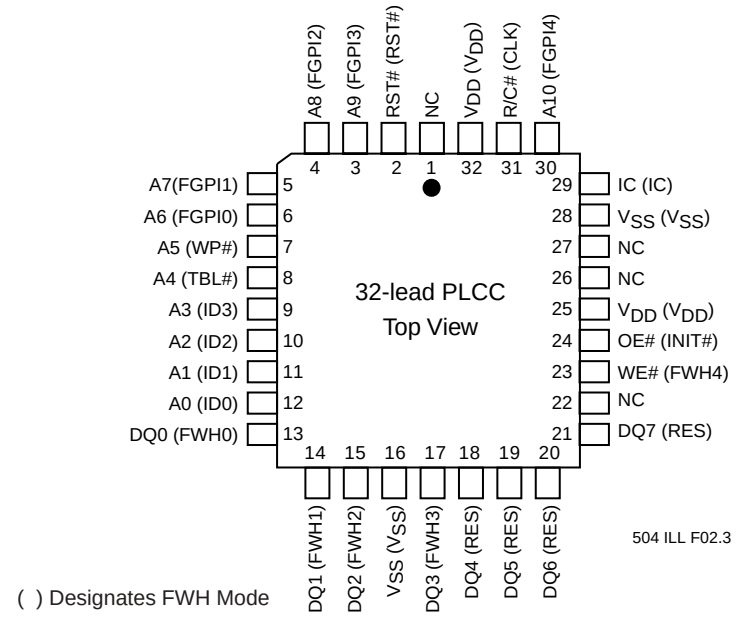


FIGURE 8: PIN ASSIGNMENTS FOR 32-LEAD PLCC

Advance Information

TABLE 8: PIN DESCRIPTION

Symbol	Pin Name	Type[1]	Interface		Functions
			PP	FWH	
A_{10}-A_0	Address	I	X		Inputs for low-order addresses during Read and Write operations. Addresses are internally latched during a Write cycle. For the programming interface, these addresses are latched by R/C# and share the same pins as the high-order address inputs.
DQ_7-DQ_0	Data	I/O	X		To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# is high.
OE#	Output Enable	I	X		To gate the data output buffers
WE#	Write Enable	I	X		To control the Write operations
IC	Interface Configuration Pin	I	X	X	This pin determines which interface is operational. When held high, programmer mode is enabled and when held low, FWH mode is enabled. This pin must be setup at power-up or before return from reset and not change during device operation. This pin is internally pulled- down with a resistor between 20-100 KΩ.
INIT#	Initialize	I		X	This is the second reset pin for in-system use. This pin is internally combined with the RST# pin; If this pin or RST# pin is driven low, identical operation is exhibited.
ID[3:0]	Identification Inputs	I		X	These four pins are part of the mechanism that allows multiple parts to be attached to the same bus. The strapping of these pins is used to identify the component.The boot device must have ID[3:0]=0000 and it is recommended that all subsequent devices should use sequential up-count strapping. These pins are internally pulled-down with a resistor between 20-100 KΩ.
FGPI[4:0]	General Purpose Inputs	I		X	These individual inputs can be used for additional board flexibility. The state of these pins can be read through GPI_REG register. These inputs should be at their desired state before the start of the PCI clock cycle during which the read is attempted, and should remain in place until the end of the Read cycle. Unused GPI pins must not be floated.
TBL#	Top Block Lock	I		X	When low, prevents programming to the Boot Block sectors at top of memory. When TBL# is high it disables hardware write protection for the top block sectors. This pin cannot be left unconnected.
FWH[3:0]	FWH I/Os	I/O		X	I/O Communications
CLK	Clock	I		X	To provide a clock input to the control unit
FWH4	FWH Input	I		X	Input Communications
RST#	Reset	I	X	X	To reset the operation of the device
WP#	Write Protect	I		X	When low, prevents programming to all but the highest addressable blocks. When WP# is high it disables hardware write protection for these blocks. This pin cannot be left unconnected.
R/C#	Row/Column Select	I	X		Select For the Programming interface, this pin determines whether the address pins are pointing to the row addresses, or to the column addresses.
RES	Reserved			X	These pins must be left unconnected.
V_{DD}	Power Supply	I	X	X	To provide power supply (3.0-3.6V)
V_{SS}	Ground	I	X	X	Circuit ground (OV reference) Every V_{SS} pin must be grounded.
NC	No Connection	I	X	X	Unconnected pins

T8.3 504

1. I = Input, O = Output

TABLE 9: OPERATION MODES SELECTION (PP MODE)

Mode	RST#	OE#	WE#	DQ	Address
Read	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Program	V_{IH}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Erase	V_{IH}	V_{IH}	V_{IL}	X[1]	Sector or Block address, XXH for Chip-Erase
Reset	V_{IL}	X	X	High Z	X
Write Inhibit	V_{IH} X	V_{IL} V_{IH}	X	High Z/D_{OUT} High Z/D_{OUT}	X X
Product Identification	V_{IH}	V_{IL}	V_{IH}	Manufacturer's ID (BFH) Device ID[2]	A_{18}-A_1=V_{IL}, A_0=V_{IL} A_{18}-A_1=V_{IL}, A_0=V_{IH}

T9.4 504

1. X can be V_{IL} or V_{IH}, but no other value.
2. Device ID 57H for SST49LF002A, 1BH for SST49LF003A, 60H for SST49LF004A, and 5AH for SST49LF008A

TABLE 10: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st[1] Write Cycle		2nd[1] Write Cycle		3rd[1] Write Cycle		4th[1] Write Cycle		5th[1] Write Cycle		6th[1] Write Cycle	
	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA[3]	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_X[4]	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA_X[5]	50H
Chip-Erase[6]	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry[7,8]	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit[9]	XXH	F0H										
Software ID Exit[9]	5555H	AAH	2AAAH	55H	5555H	F0H						

T10.5 504

1. FWH Mode uses consecutive Write cycles to complete a command sequence; PP Mode uses consecutive bus cycles to complete a command sequence.
2. Address format A_{14}-A_0 (Hex), Addresses A_{15}-A_{21} can be V_{IL} or V_{IH}, but no other value, for the Command sequence in PP Mode.
3. BA = Program Byte address
4. SA_X for Sector-Erase Address
5. BA_X for Block-Erase Address
6. Chip-Erase is supported in PP Mode only
7. SST Manufacturer's ID = BFH, is read with A_0=0,
   With A_{17}-A_1 = 0; 49LF002A Device ID = 57H, is read with A_0 = 1.
   With A_{18}-A = 0; 49LF003A Device ID = 1BH, is read with A_0 = 1.
   With A_{18}-A_1 = 0; 49LF004A Device ID = 60H, is read with A_0 = 1.
   With A_{19}-A_1 = 0; 49LF008A Device ID = 5AH, is read with A_0 = 1.
8. The device does not remain in Software Product ID mode if powered down.
9. Both Software ID Exit operations are equivalent

Advance Information

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential[1] . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (Ta=25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[2] . . . . . 50 mA

1. Do not violate processor or chipset limitations on the INIT# pin.
2. Outputs shorted for no more than one second. No more than one output shorted at a time. This note applies to non-PCI outputs.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +85°C	3.0-3.6V

AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	3 ns
Output Load	C_L = 30 pF
See Figures 24 and 25	

1. FWH interface signals use PCI load test conditions

TABLE 11: DC OPERATING CHARACTERISTICS (ALL INTERFACE)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input=V_{IL}/V_{IH}, at F=1/T_{RC} Min, V_{DD}=V_{DD} Max (PP Mode)
	Read		12	mA	OE#=V_{IH}, WE#=V_{IH}
	Write		24	mA	OE#=V_{IH}, WE#=V_{IL}, V_{DD}=V_{DD} Max (PP Mode)
I_{SB}	Standby V_{DD} Current (FWH Interface)		100	µA	FWH4=0.9V_{DD}, f=33 MHz V_{DD}=V_{DD} Max, All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_{RY}[1]	Ready Mode V_{DD} Current (FWH Interface)		10	mA	FWH4=V_{IL}, f=33 MHz V_{DD}=V_{DD} Max All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_I	Input Current for IC, ID [3:0] pins		200	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IHI}[2]	INIT# Input High Voltage	1.0	V_{DD}+0.5	V	V_{DD}=V_{DD} Max
V_{ILI}[2]	INIT# Input Low Voltage	-0.5	0.4	V	V_{DD}=V_{DD} Min
V_{IL}	Input Low Voltage	-0.5	0.3 V_{DD}	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.5 V_{DD}	V_{DD}+0.5	V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.1 V_{DD}	V	I_{OL}=1500µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	0.9 V_{DD}		V	I_{OH}=-500 µA, V_{DD}=V_{DD} Min

T11.8 504

1. The device is in Ready Mode when no activity is on the FWH bus.
2. Do not violate processor or chipset specification regarding INIT# voltage.

TABLE 12: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T12.2 504

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

TABLE 13: PIN IMPEDANCE (V_{DD}=3.3V, Ta=25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	12 pF
L_{PIN}[2]	Pin Inductance		20 nH

T13.4 504

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Refer to PCI spec.

TABLE 14: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

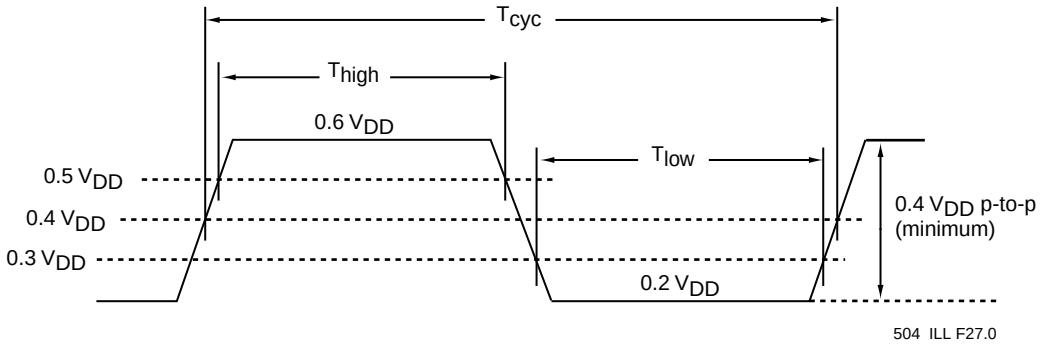
T14.3 504

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 15: CLOCK TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{CYC}	CLK Cycle Time	30		ns
T_{HIGH}	CLK High Time	11		ns
T_{LOW}	CLK Low Time	11		ns
-	CLK Slew Rate (peak-to-peak)	1	4	V/ns
-	RST# or INIT# Slew Rate	50		mV/ns

T15.1 504



504 ILL F27.0

FIGURE 9: CLK WAVEFORM

AC CHARACTERISTICS (FWH MODE)

TABLE 16: READ/WRITE CYCLE TIMING PARAMETERS (FWH MODE), V_{DD} =3.0-3.6V

Symbol	Parameter	Min	Max	Units
T_{CYC}	Clock Cycle Time	30		ns
T_{SU}	Data Set Up Time to Clock Rising	7		ns
T_{DH}	Clock Rising to Data Hold Time	0		ns
T_{VAL}[1]	Clock Rising to Data Valid	2	11	ns
T_{BP}	Byte Programming Time		20	µs
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms
T_{SCE}	Chip-Erase Time		100	ms
T_{ON}	Clock Rising to Active (Float to Active Delay)	2		ns
T_{OFF}	Clock Rising to Inactive (Active to Float Delay)		28	ns

T16.3 504

1. Minimum and maximum times have different loads. See PCI spec.

TABLE 17: AC INPUT/OUTPUT SPECIFICATIONS (FWH MODE)

Symbol	Parameter	Min	Max	Units	Conditions
I_{OH}(AC)	Switching Current High	-12 V_{DD} -17.1(V_{DD}-V_{OUT})	 Equation C[1]	mA mA	0 < V_{OUT} ≤ 0.3V_{DD} 0.3V_{DD} < V_{OUT} < 0.9V_{DD} 0.7V_{DD} < V_{OUT} <V_{DD}
	(Test Point)		-32 V_{DD}	mA	V_{OUT}=0.7V_{DD}
I_{OL}(AC)	Switching Current Low	16 V_{DD} 26.7 V_{OUT}	Equation D[1]	mA mA	V_{DD} >V_{OUT} ≥0.6V_{DD} 0.6V_{DD} > V_{OUT} > 0.1V_{DD} 0.18V_{DD} > V_{OUT} > 0
	(Test Point)		38 V_{DD}	mA	V_{OUT}=0.18V_{DD}
I_{CL}	Low Clamp Current	-25+(V_{IN}+1)/0.015		mA	-3 < V_{IN} ≤ -1
I_{CH}	High Clamp Current	25+(V_{IN}-V_{DD}-1)/0.015		mA	V_{DD}+4 > V_{IN} ≤ V_{DD}+1
slewr[2]	Output Rise Slew Rate	1	4	V/ns	0.2V_{DD}-0.6V_{DD} load
slewf[2]	Output Fall Slew Rate	1	4	V/ns	0.6V_{DD}-0.2V_{DD} load

T17.3 504

1. See PCI spec.
2. PCI specification output load is used.

TABLE 18: RESET TIMING PARAMETERS, V_{DD} =3.0-3.6V (FWH MODE)

Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} stable to Reset Low	1		ms
T_{KRST}	Clock Stable to Reset Low	100		µs
T_{RSTP}	RST# Pulse Width	100		ns
T_{RSTF}	RST# Low to Output Float		48	ns
T_{RST}[1]	RST# High to FWH4 Low	1		µs
T_{RSTE}	RST# Low to reset during Sector-/Block-Erase or Program		10	µs

T18.5 504

1. There will be a latency of T_{RSTE} if a reset procedure is performed during a Program or Erase operation.

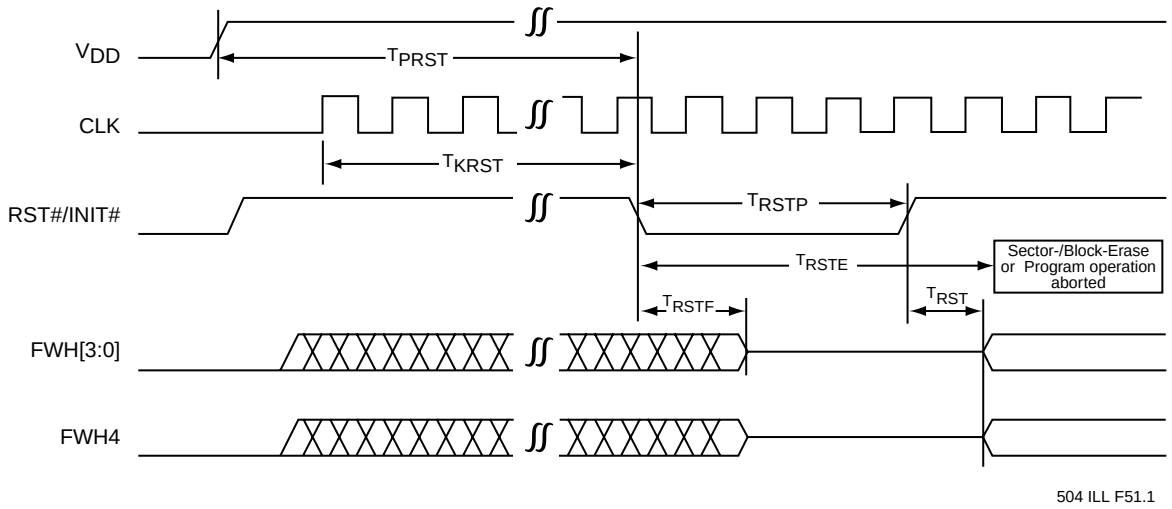


FIGURE 10: RESET TIMING DIAGRAM

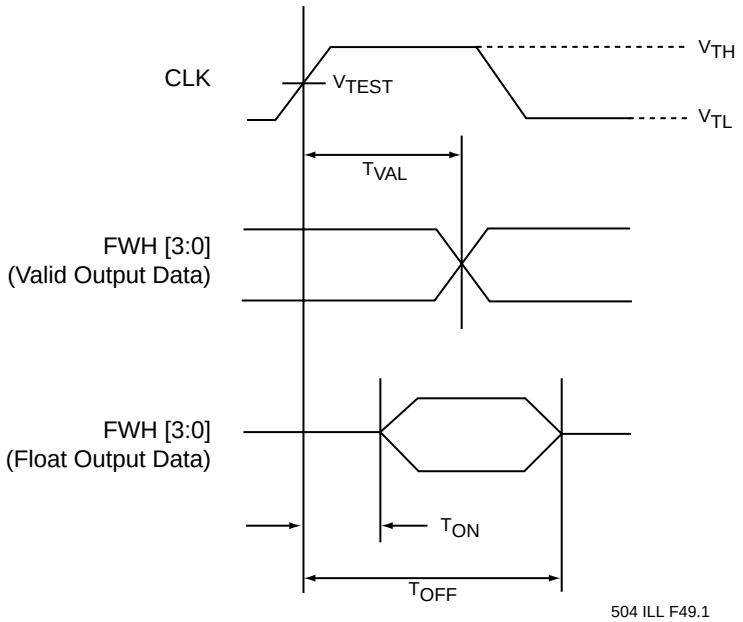


FIGURE 11: OUTPUT TIMING PARAMETERS

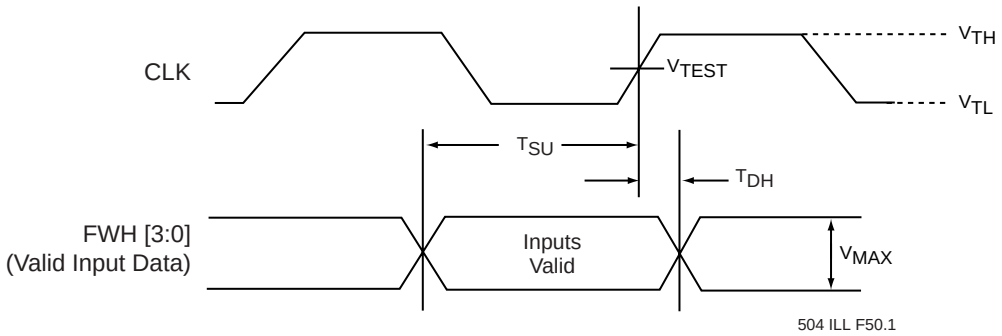


FIGURE 12: INPUT TIMING PARAMETERS

TABLE 19: INTERFACE MEASUREMENT CONDITION PARAMETERS

Symbol	Value	Units
V_{TH}[1]	0.6 V_{DD}	V
V_{TL}[1]	0.2 V_{DD}	V
V_{TEST}	0.4 V_{DD}	V
V_{MAX}[1]	0.4 V_{DD}	V
Input Signal Edge Rate	1 V/ns	

T19.3 504

1. The input test environment is done with 0.1 V_{DD} of overdrive over V_{IH} and V_{IL}. Timing parameters must be met with no more overdrive than this. V_{MAX} specified the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters.

AC CHARACTERISTICS (PP MODE)

TABLE 20: READ CYCLE TIMING PARAMETERS V_{DD} =3.0-3.6V (PP MODE)

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	270		ns
T_{RST}	RST# High to Row Address Setup	1		µs
T_{AS}	R/C# Address Set-up Time	45		ns
T_{AH}	R/C# Address Hold Time	45		ns
T_{AA}	Address Access Time		120	ns
T_{OE}	Output Enable Access Time		60	ns
T_{OLZ}	OE# Low to Active Output	0		ns
T_{OHZ}	OE# High to High-Z Output		35	ns
T_{OH}	Output Hold from Address Change	0		ns

T20.2 504

TABLE 21: PROGRAM/ERASE CYCLE TIMING PARAMETERS V_{DD} =3.0-3.6V (PP MODE)

Symbol	Parameter	Min	Max	Units
T_{RST}	RST# High to Row Address Setup	1		µs
T_{AS}	R/C# Address Setup Time	50		ns
T_{AH}	R/C# Address Hold Time	50		ns
T_{CWH}	R/C# to Write Enable High Time	50		ns
T_{OES}	OE# High Setup Time	20		ns
T_{OEH}	OE# High Hold Time	20		ns
T_{OEP}	OE# to Data# Polling Delay		40	ns
T_{OET}	OE# to Toggle Bit Delay		40	ns
T_{WP}	WE# Pulse Width	100		ns
T_{WPH}	WE# Pulse Width High	100		ns
T_{DS}	Data Setup Time	50		ns
T_{DH}	Data Hold Time	5		ns
T_{IDA}	Software ID Access and Exit Time		150	ns
T_{BP}	Byte Programming Time		20	µs
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms
T_{SCE}	Chip-Erase Time		100	ms

T21.2 504

TABLE 22: RESET TIMING PARAMETERS, V_{DD} =3.0-3.6V (PP MODE)

Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} stable to Reset Low	1		ms
T_{RSTP}	RST# Pulse Width	100		ns
T_{RSTF}	RST# Low to Output Float		48	ns
T_{RST}[1]	RST# High to Row Address Setup	1		µs
T_{RSTE}	RST# Low to reset during Sector-/Block-Erase or Program		10	µs
T_{RSTC}	RST# Low to reset during Chip-Erase		50	µs

T22.1 504

1. There will be a reset latency of T_{RSTE} or T_{RSTC} if a reset procedure is performed during a Program or Erase operation.

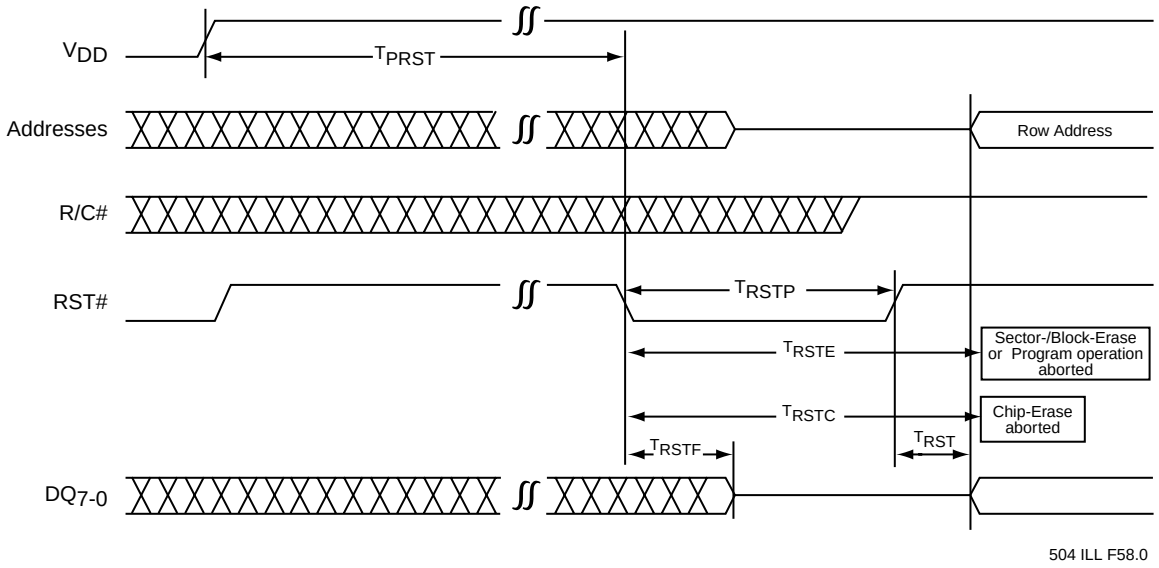


FIGURE 13: RESET TIMING DIAGRAM

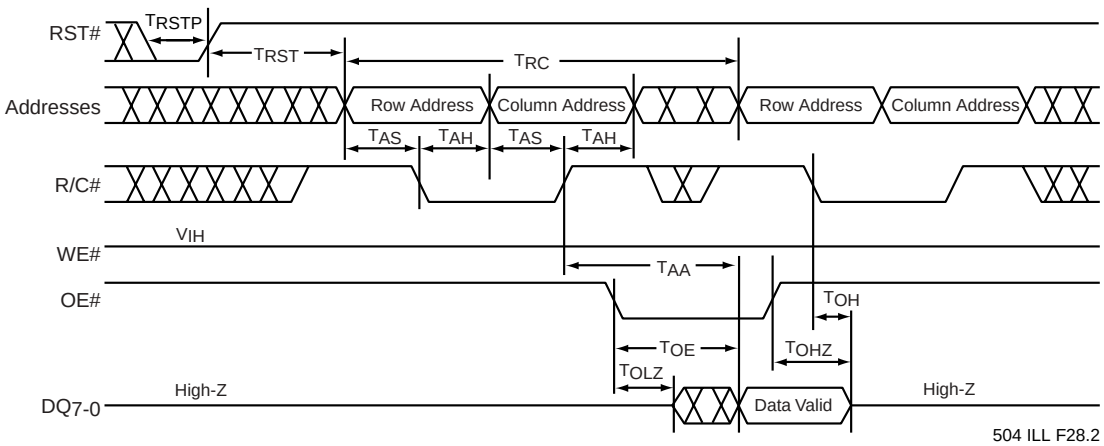


FIGURE 14: READ CYCLE TIMING DIAGRAM (PP MODE)

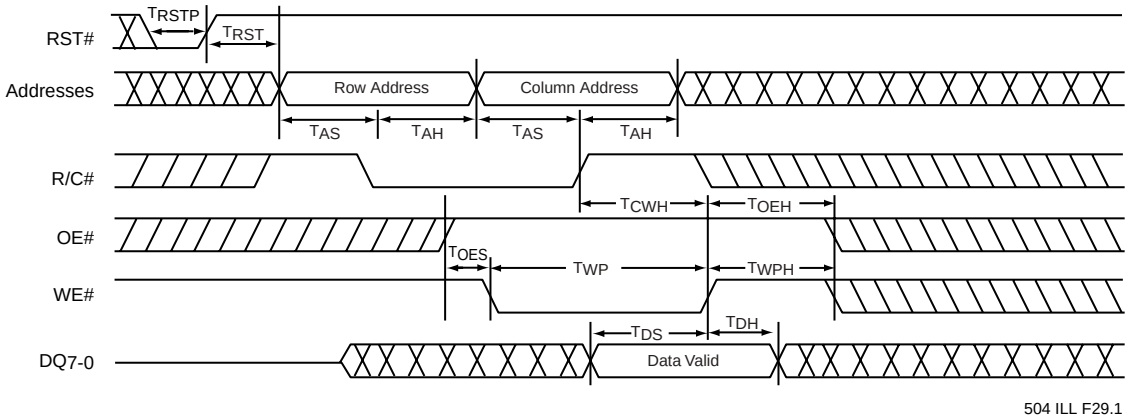


FIGURE 15: WRITE CYCLE TIMING DIAGRAM (PP MODE)

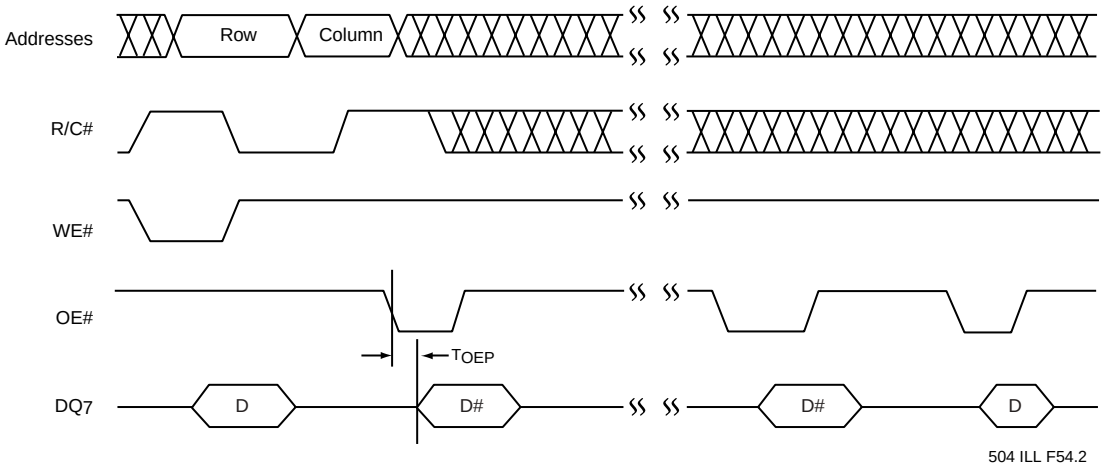


FIGURE 16: DATA# POLLING TIMING DIAGRAM (PP MODE)

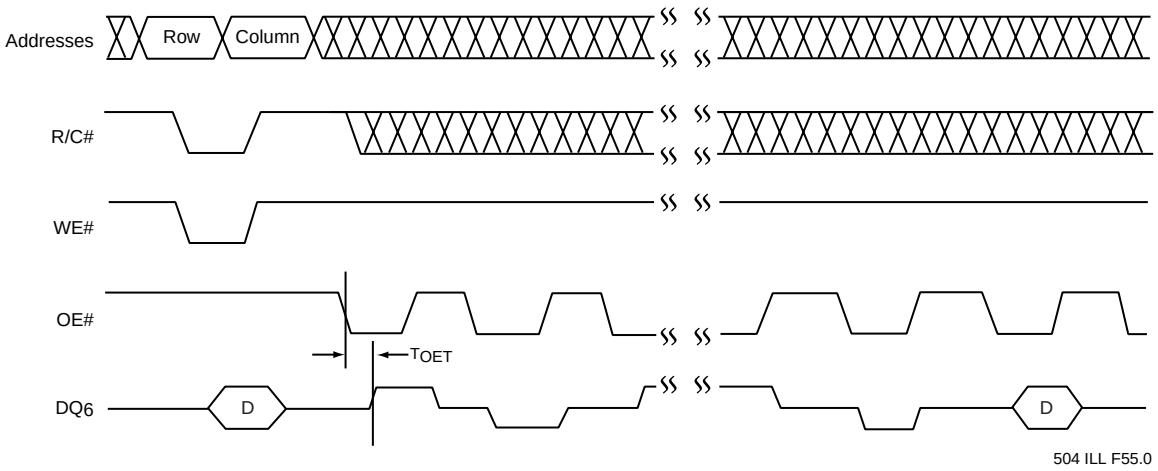


FIGURE 17: TOGGLE BIT TIMING DIAGRAM (PP MODE)

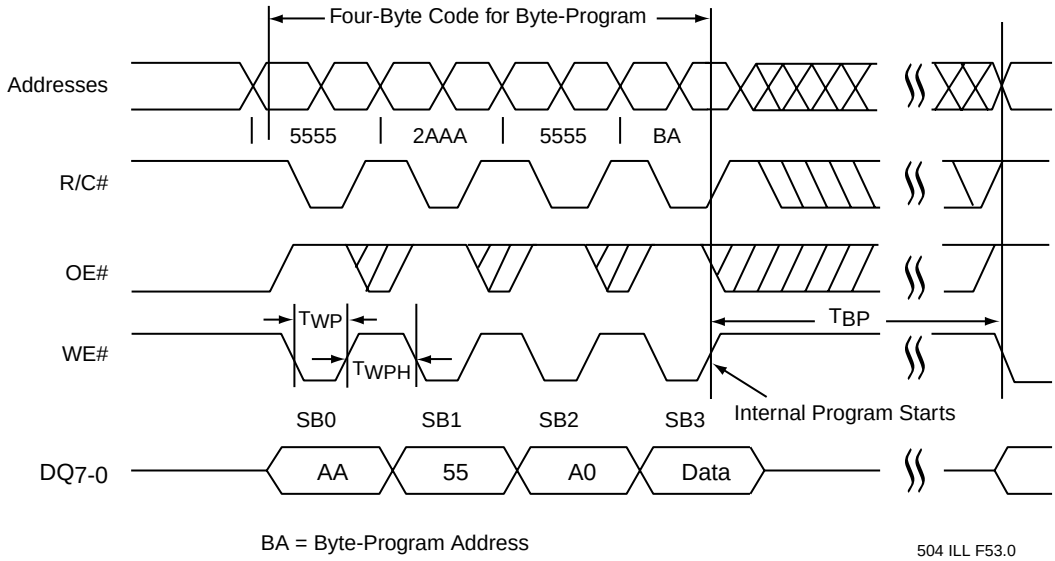


FIGURE 18: BYTE-PROGRAM TIMING DIAGRAM (PP MODE)

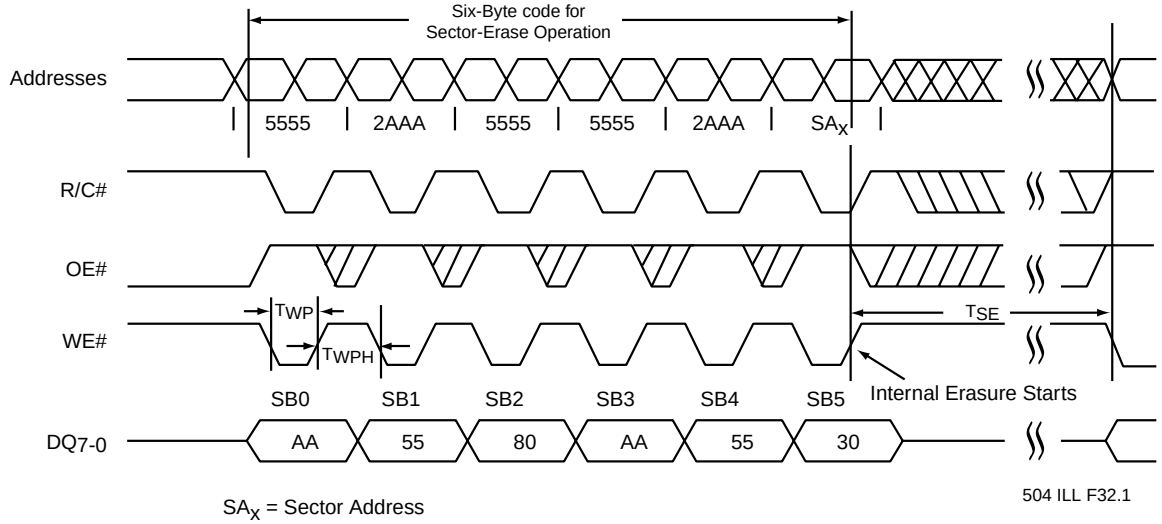


FIGURE 19: SECTOR-ERASE TIMING DIAGRAM (PP MODE)

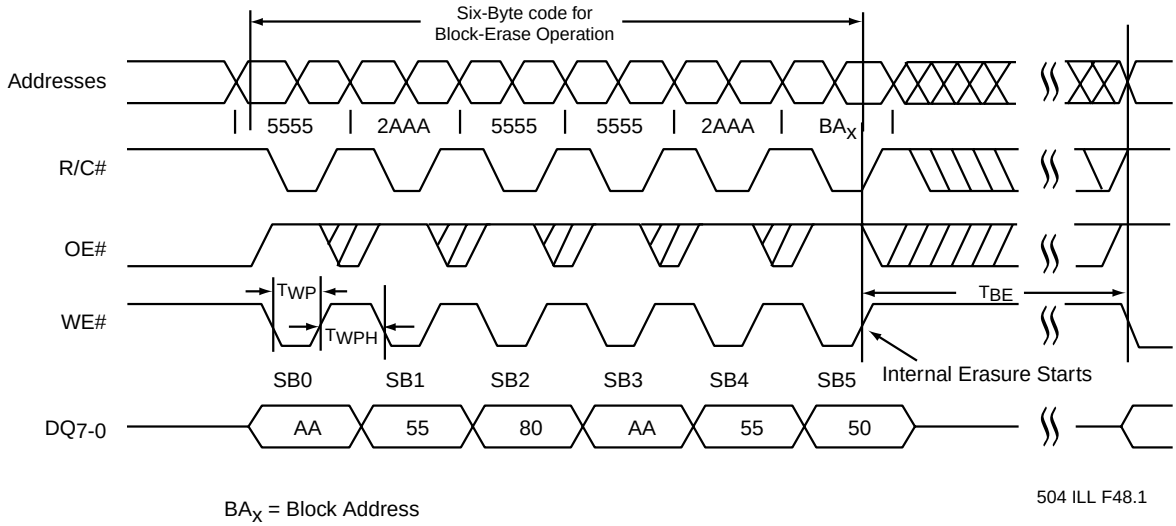


FIGURE 20: BLOCK-ERASE TIMING DIAGRAM (PP MODE)

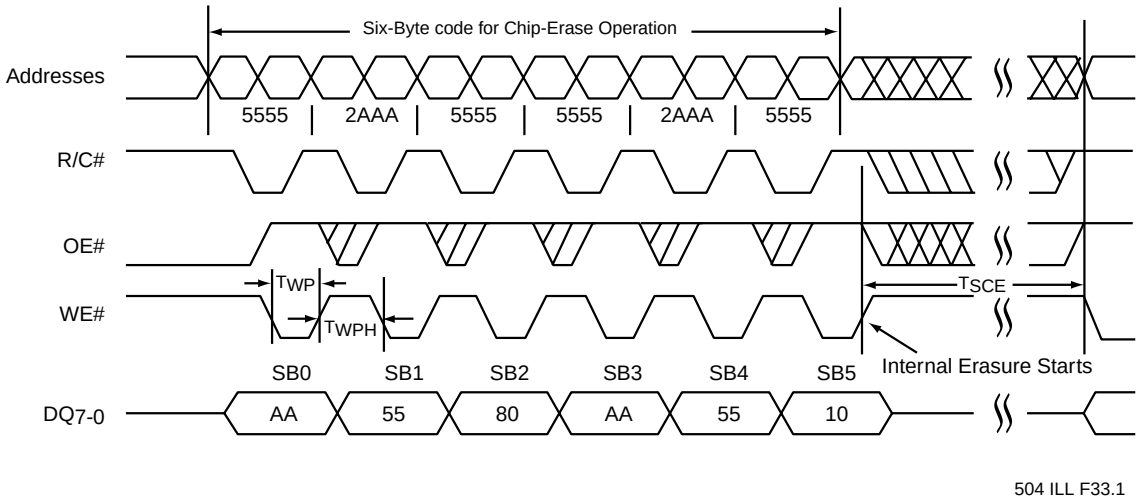
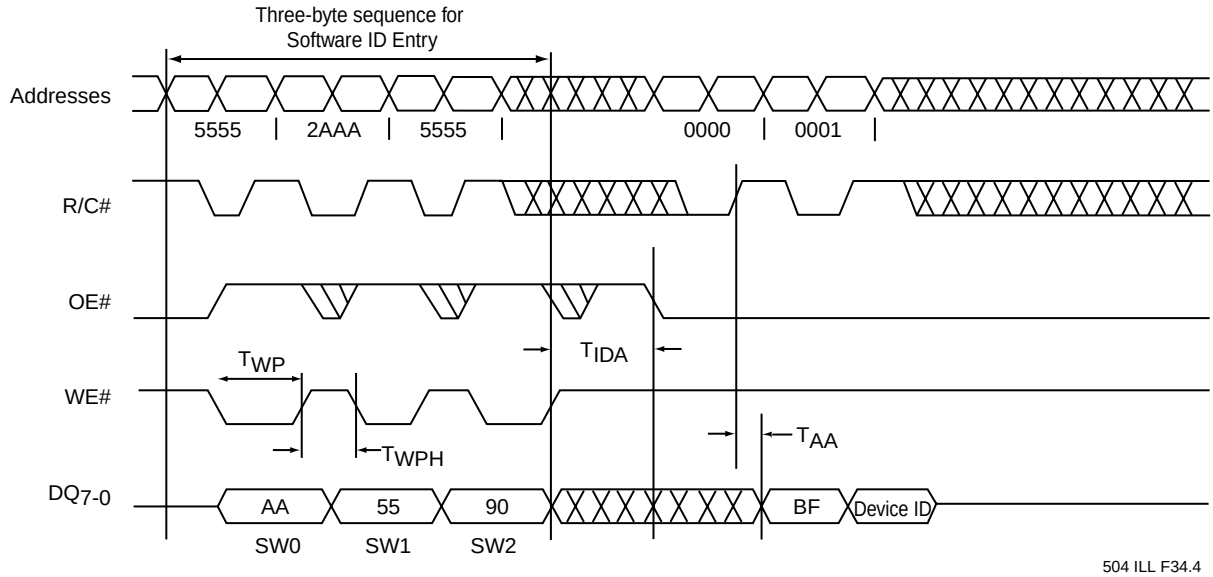


FIGURE 21: CHIP-ERASE TIMING DIAGRAM (PP MODE)



Device ID = 57H for SST49LF002A, 1BH for SST49LF003A,
60H for SST49LF004A, 5AH for SST49LF008A

FIGURE 22: SOFTWARE ID ENTRY AND READ (PP MODE)

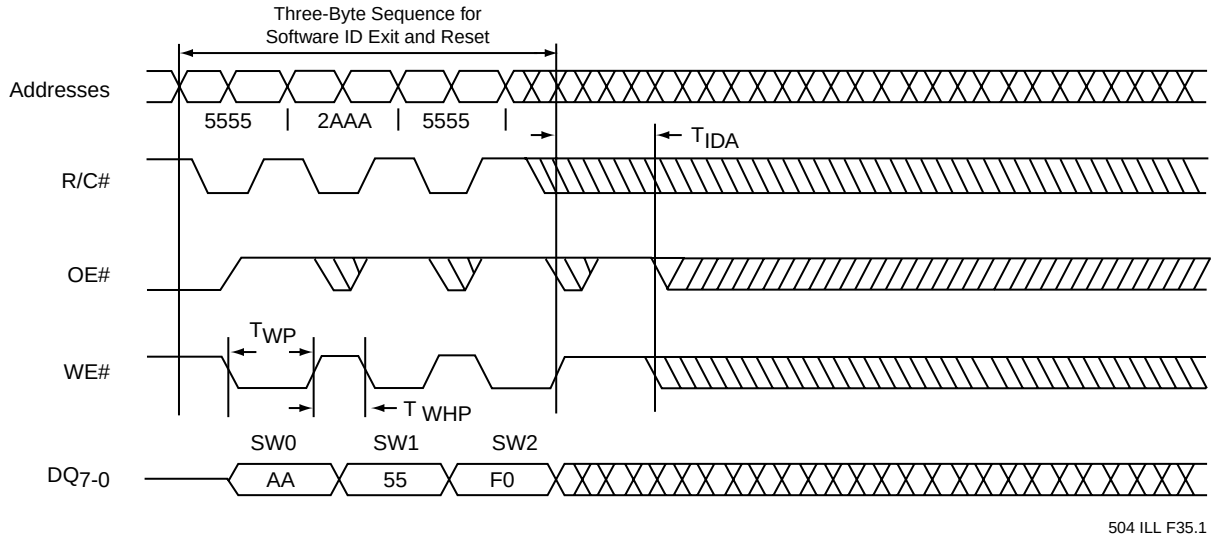
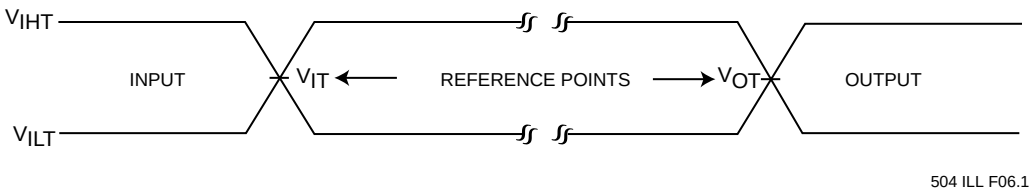


FIGURE 23: SOFTWARE ID EXIT AND RESET (PP MODE)



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 24: AC INPUT/OUTPUT REFERENCE WAVEFORMS (PP MODE)

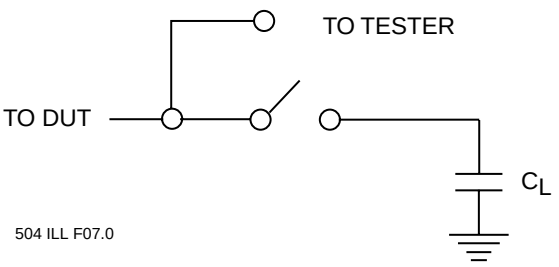


FIGURE 25: A TEST LOAD EXAMPLE (PP MODE)

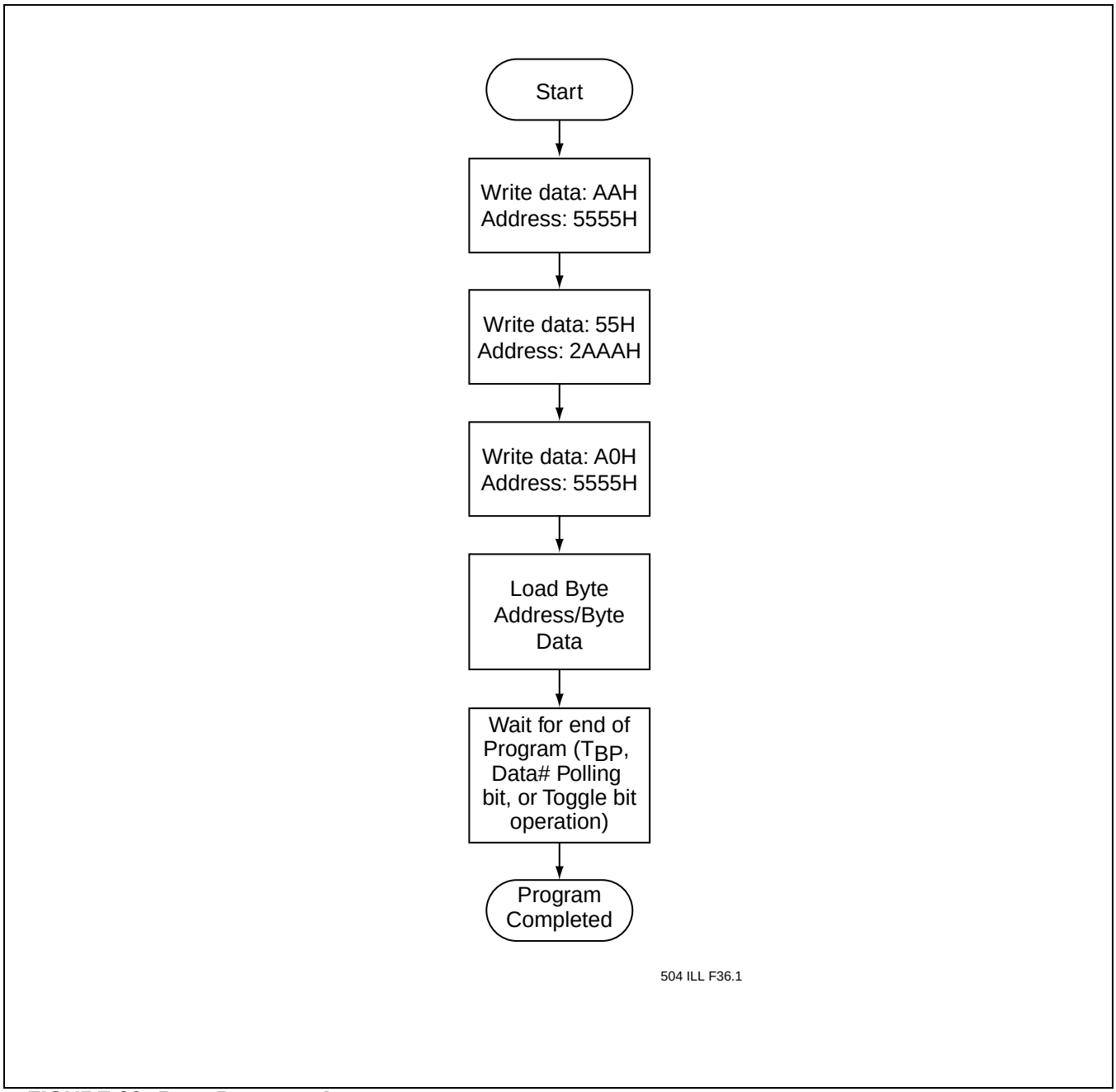


FIGURE 26: BYTE-PROGRAM ALGORITHM

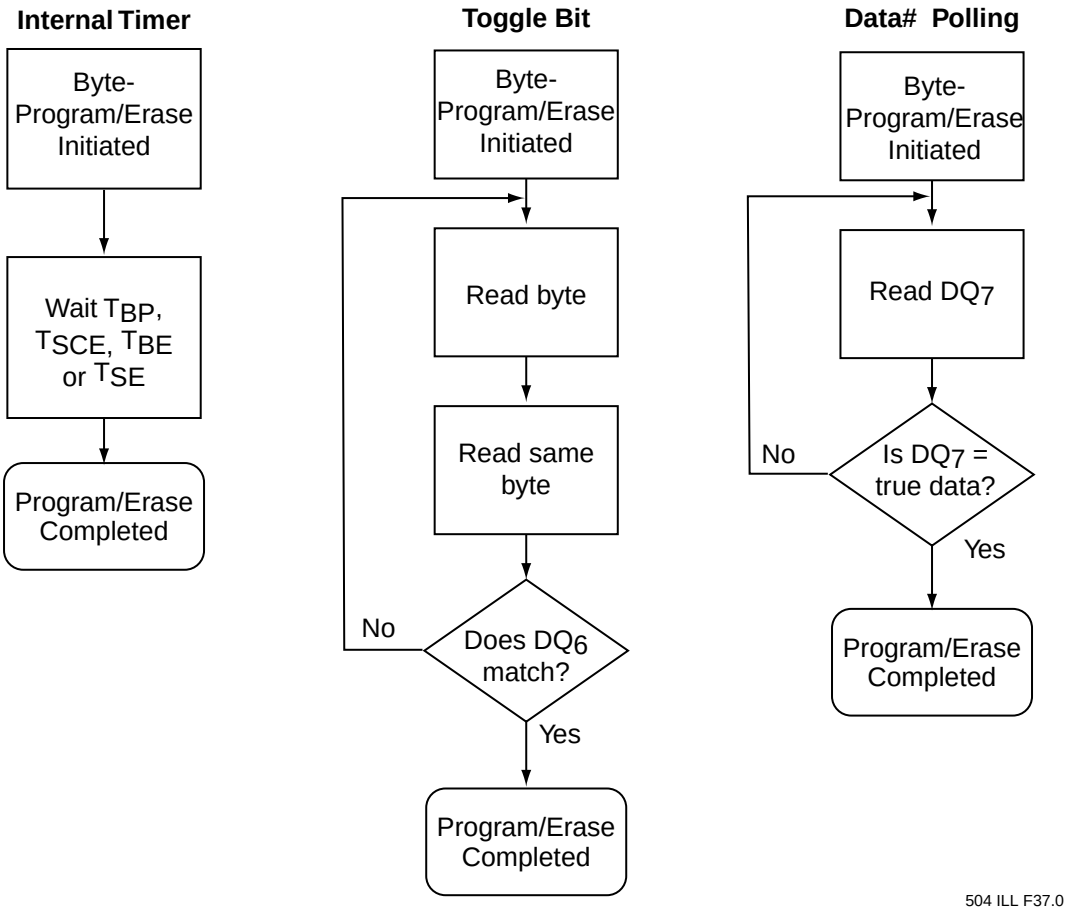


FIGURE 27: WAIT OPTIONS

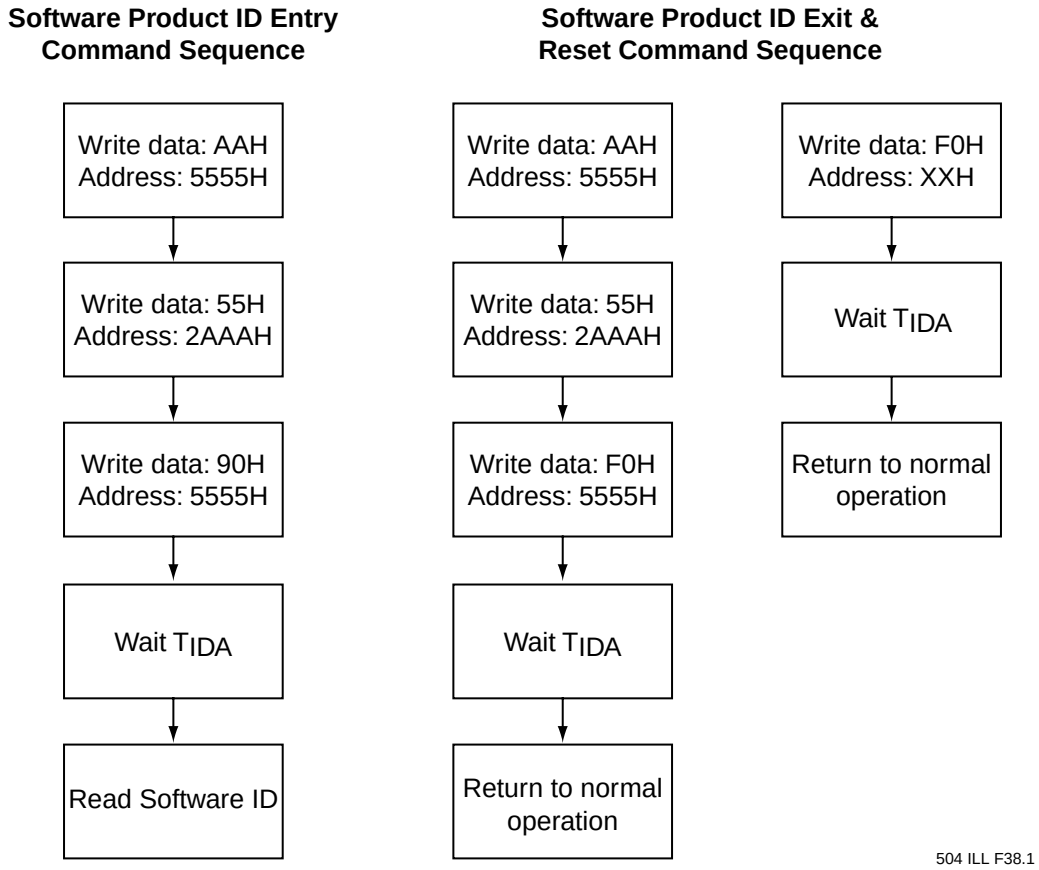


FIGURE 28: SOFTWARE PRODUCT COMMAND FLOWCHARTS

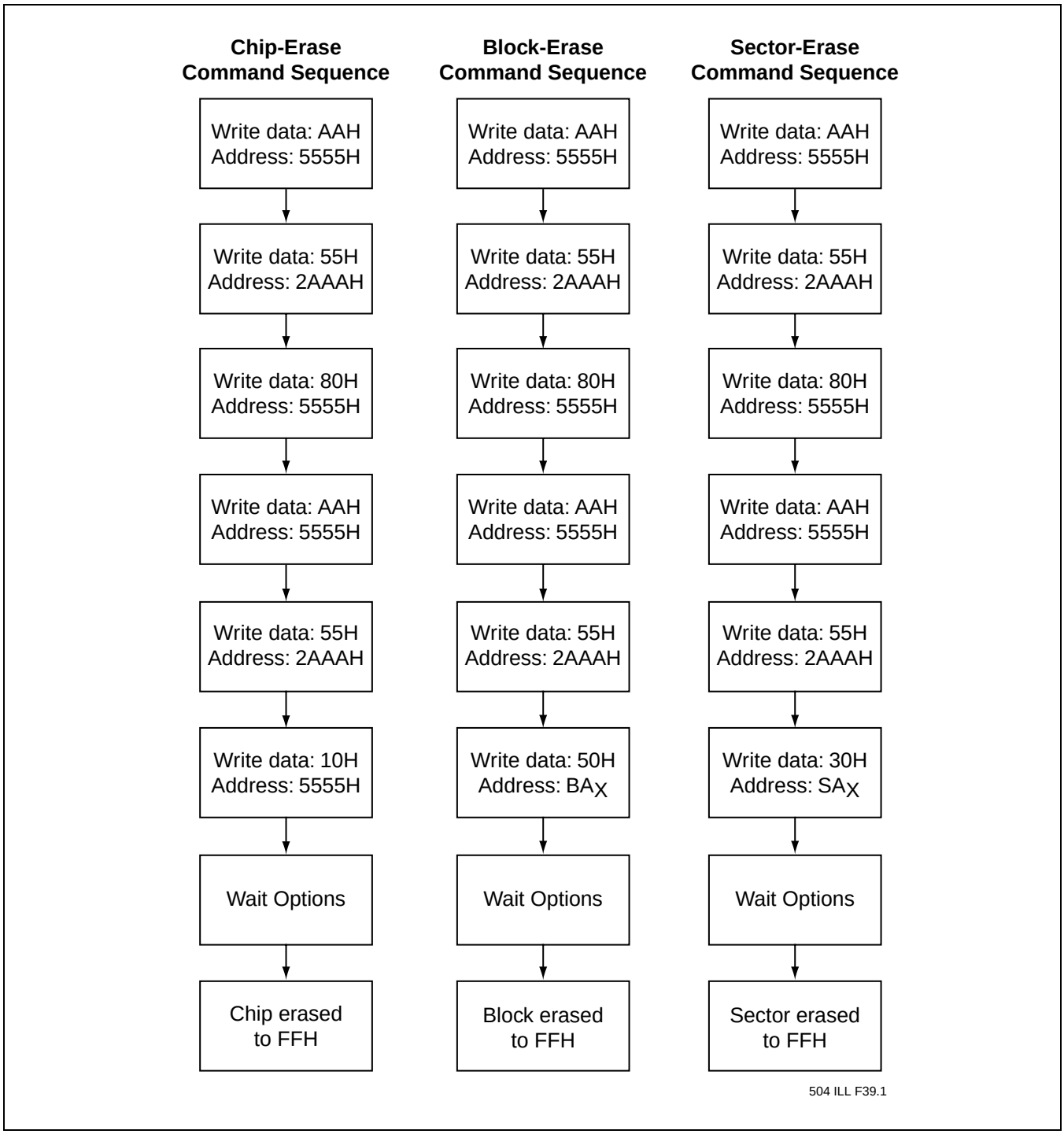
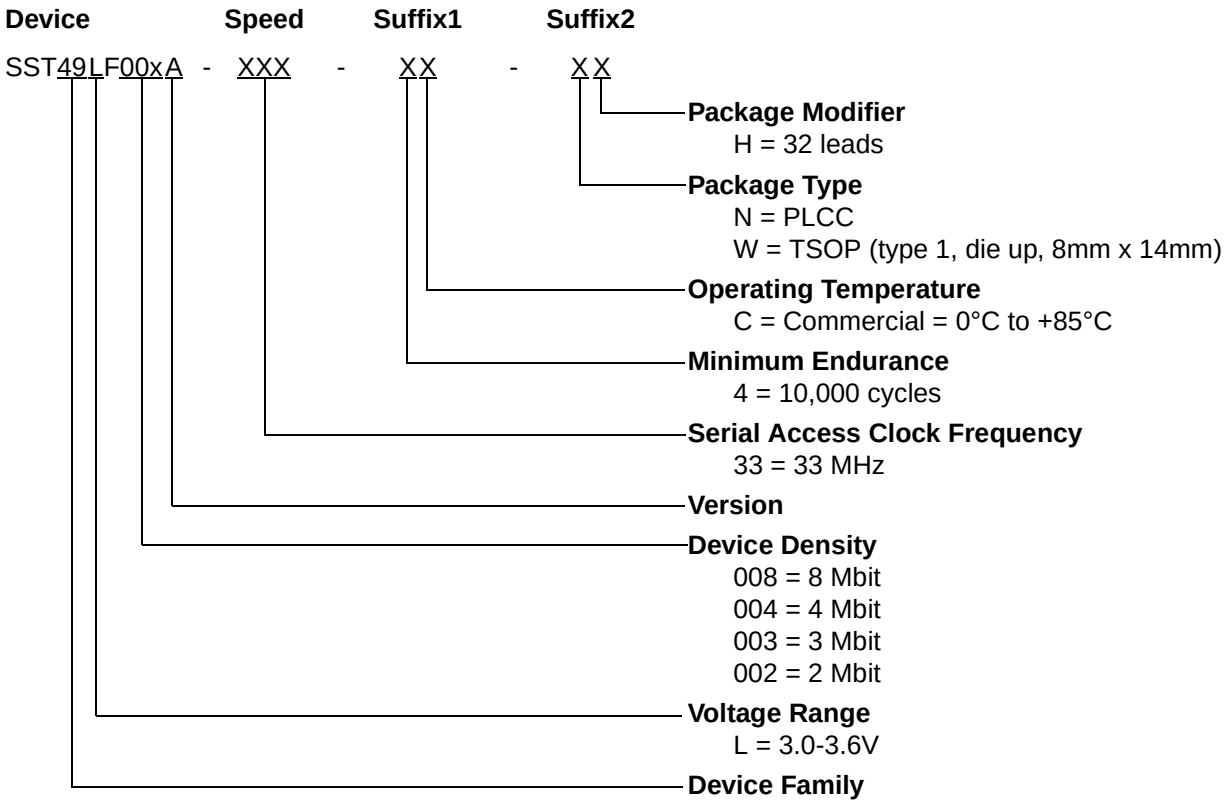


FIGURE 29: ERASE COMMAND SEQUENCE

Advance Information

PRODUCT ORDERING INFORMATION



Valid combinations for SST49LF002A

SST49LF002A-33-4C-WH SST49LF002A-33-4C-NH

Valid combinations for SST49LF003A

SST49LF003A-33-4C-WH SST49LF003A-33-4C-NH

Valid combinations for SST49LF004A

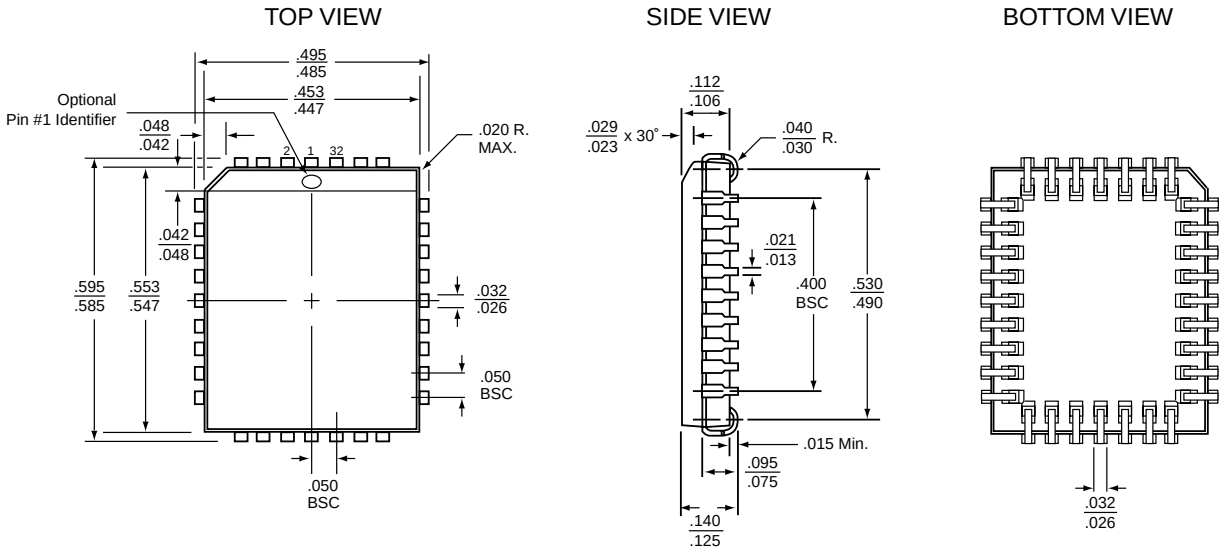
SST49LF004A-33-4C-WH SST49LF004A-33-4C-NH

Valid combinations for SST49LF008A

SST49LF008A-33-4C-WH SST49LF008A-33-4C-NH

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

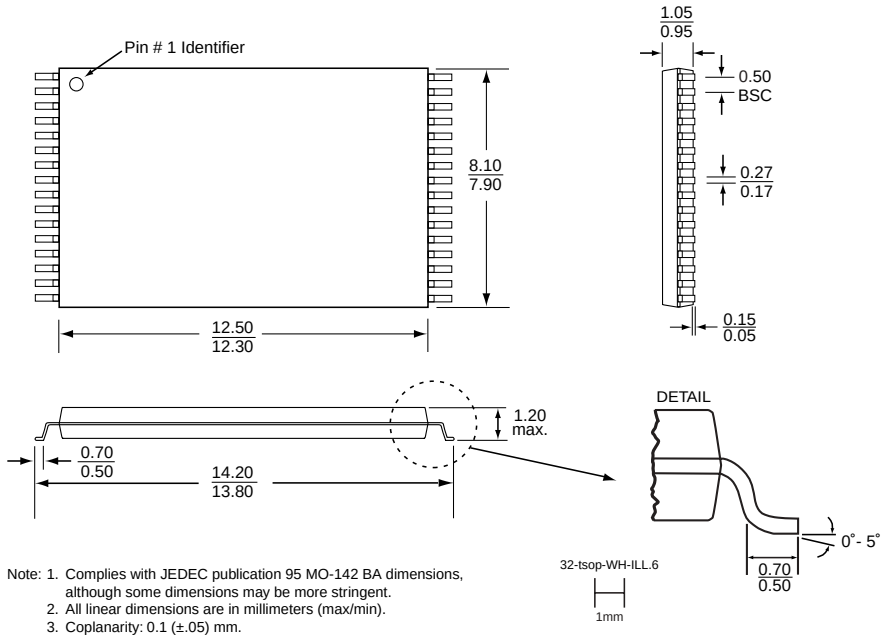
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

32-plcc-NH-ILL.2

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 (±.05) mm.
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH