CMOS 4-Bit Microcontroller

TMP47C620DF, TMP47C820DF

The 47C620/820 are high speed and high performance 4-bit single chip microcomputers based on the TLCS-470 series with a LCD driver and high speed timer / counters.

Part No.	ROM	RAM	Package	OTP Version
TMP47C620DF	6144 × 8-bit	384 × 4-bit	P-QFP80-1420-0.80B	TMP47P820VDF
TMP47C820DF	8192 × 8-bit	512 × 4-bit		

Features

◆4-bit single chip microcomputer

◆Instruction execution time:
1.3 μs (at 6 MHz), 244 μs (at 32.8 kHz)

◆92 basic instructions
- Table look-up instructions
- 5-bit to 8-bit data conversion instruction

◆Subroutine nesting: 15 levels max.

◆6 interrupt sources (External: 2, Internal: 4)
All sources have independent latches each, and multiple interrupt control is available.

◆I/O port (36 pins)
- Input 2 ports 5 pins
- Output 2 ports 8 pins
- I/O 6 ports 23 pins

◆Interval Timer

◆Two 12-bit Timer / Counters
Timer, event counter, and pulse width measurement mode

◆Two 8-bit High speed Timer / Counters
Timer, event counter, frequency measurement, and pulse output mode

◆Watchdog Timer

◆Serial Interface with 8-bit buffer
- Simultaneous transmission and reception capability.
- External / internal colck, leading / trailing edge, and 4/8-bit mode

◆High current outputs
LED direct drive capability (typ.10 mA × 8 bits)

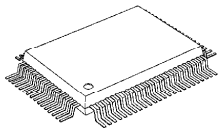
◆LCD driver
- LCD direct drive capability (max. 16-digit display at 1/4 duty LCD)
- 1/4, 1/3 1/2 duties or static drive are programmably selectable.

◆Dual-clock operation
High-speed / Low-power consumption operating mode

◆Hold function
Battery / Capacitor back-up

◆Real Time Emulator: BM47C820F0A

P-QFP80-1420-0.80B

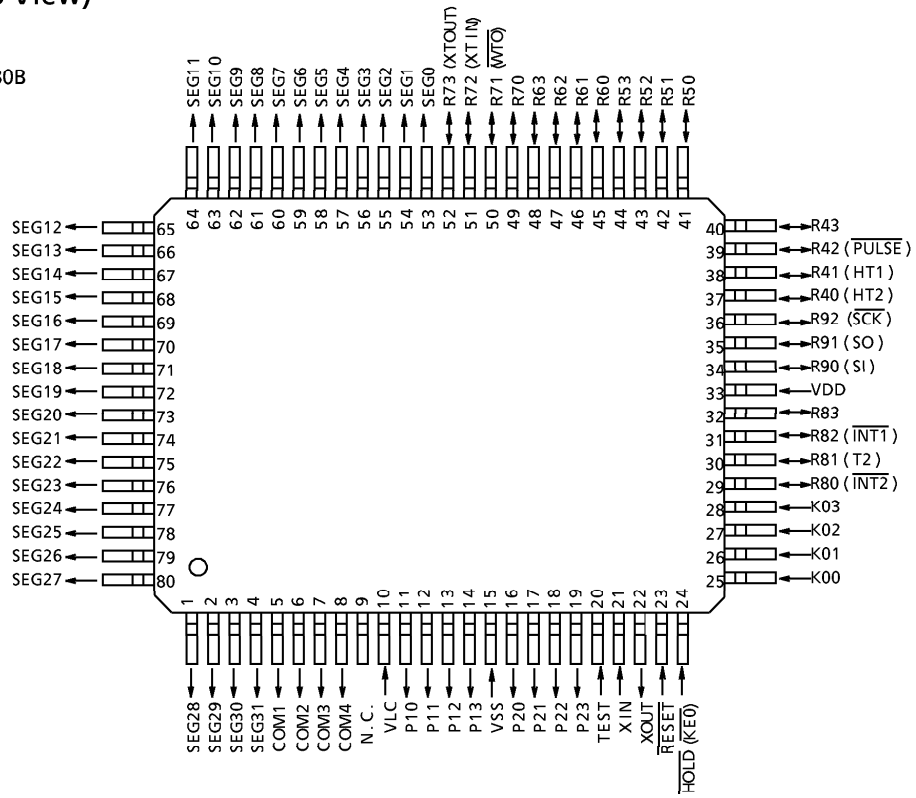


TMP47C620DF
TMP47C820DF
TMP47P820VDF

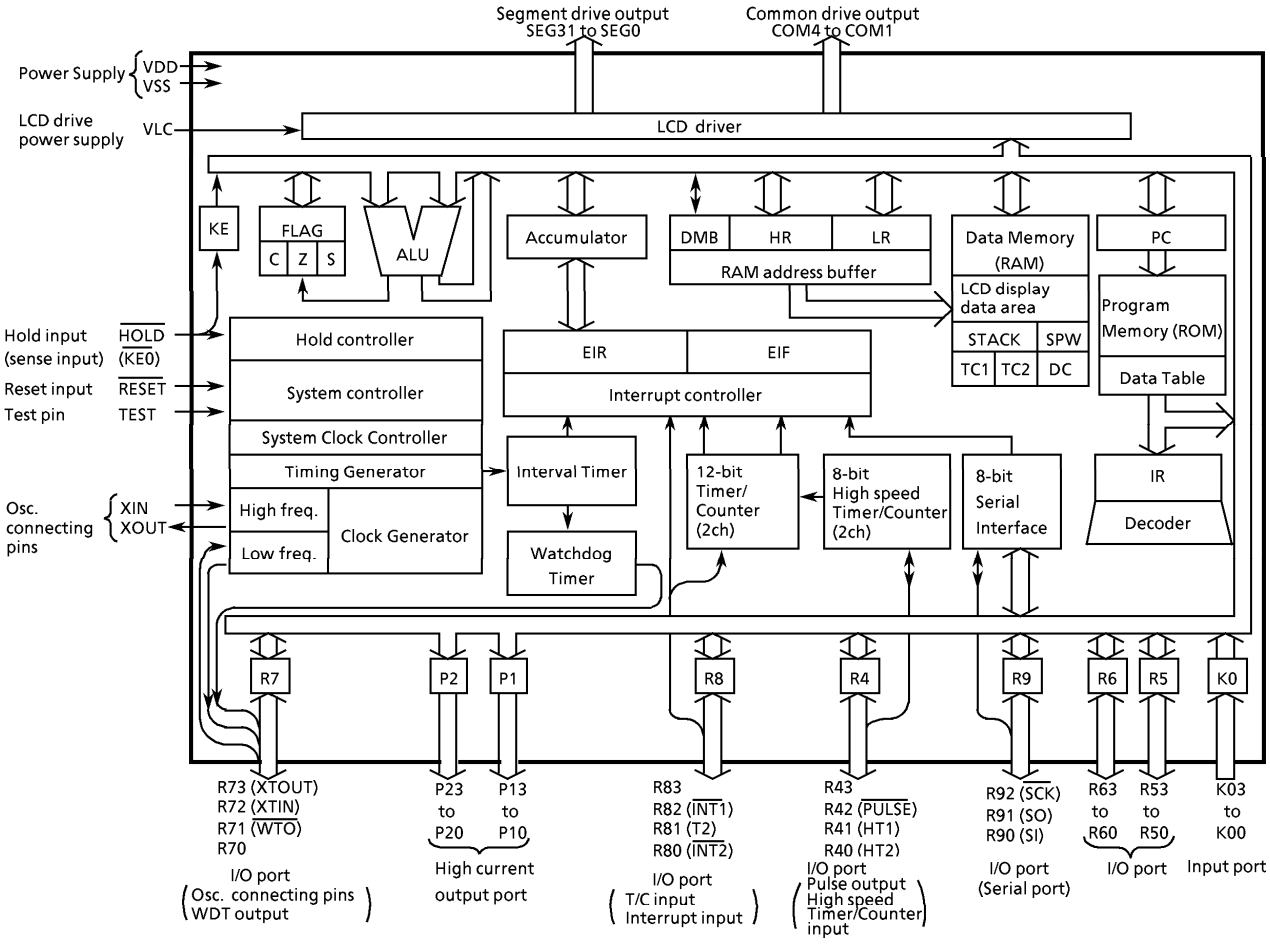
980901EBP2

Pin Assignment (Top View)

P-QFP80-1420-0.80B



Block Diagram



Pin Function

Pin Name	Input / Output	Functions	
K03 to K00	Input	4-bit input port	
P13 to P10	Output	4-bit output port with latch.	
P23 to P20		8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
R43	I/O	4-bit I/O port with latch.	
R42 ($\overline{\text{PULSE}}$)	I/O (Output)	When used as input port or high speed Time/Counter, the latch must be set to "1".	Pulse output (High speed T/C2)
R41 (HT1)	I/O (Input)		High speed Timer/Counter 1 input
R40 (HT2)			High speed Timer/Counter 2 input
R53 to R50	I/O	4-bit I/O port with latch.	
R63 to R60		When used as input port, the latch must be set to "1".	
R73 (XTOUT)	I/O (Output)	4-bit I/O port with latch.	Resonator connecting pins (low-frequency).
R72 (XTIN)	I/O (Input)		For inputting external clock, XIN is used and XOUT is opened.
R71 ($\overline{\text{WTO}}$)	I/O (Output)	When used as input port, watchdog timer output, the latch must be set to "1".	Watchdog timer output
R70	I/O		
R83	I/O	4-bit I/O port with latch.	
R82 ($\overline{\text{INT1}}$)	I/O (Input)	When used as input port, external interrupt input pin, or Timer/Counter external input pin, the latch must be set to "1".	External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{\text{INT2}}$)			External interrupt 2 input
R92 ($\overline{\text{SCK}}$)	I/O (I/O)	3-bit I/O port with latch.	Serial clock I/O
R91 (SO)	I/O (Output)	When used as input port, serial port the latch must be set to "1".	Serial data output
R90 (SI)	I/O (Input)		Serial data input
SEG31 to SEG0	Output	LCD Segment drive output	
COM4 to COM1		LCD Common drive output	
XIN	Input	Resonator connecting pins (high-frequency) .	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
$\overline{\text{RESET}}$	Input	Reset signal input	
$\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$)	Input (Input)	Hold request/ release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5 V	
VSS		0 V (GND)	
VLC		LCD drive power supply	

Operational Description

Concerning the 47C620/820 the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C660/860, the technical data sheets for the 47C660/860 shall also be referred to.

1. System Configuration

◆ Internal CPU Function

They are the same as those of the 47C660/860.

◆ Peripheral Hardware Function

① I/O Port
② Interval Timer
③ Timer / Counters (TC1, TC2)
④ Watchdog Timer
⑤ High speed Timer / Counter
⑥ LCD Driver
⑦ Serial Interface

The description has been provide with priority on functions (①, ⑤ and ⑥) added to and changed from the 47C660/860.

2. Peripheral Hardware Function

2.1 I/O Ports

The 47C620/820 have 10 I/O ports (36 pins) each as follows.

① K0 ; 4-bit input
② P1, P2 ; 4-bit output
③ R4 ; 4-bit input / output (shared with high speed timer / counter input and pulse output)
④ R5, R6 ; 4-bit input / output
⑤ R7 ; 4-bit input / output (shared with the Low-frequency reasonator connecting pin and the Watchdog timer output)
⑥ R8 ; 4-bit input / output (shared with external interrupt and timer / counter input)
⑦ R9 ; 3-bit input / output (shared with serial port)
⑧ KE ; 1-bit sense input (shared with hold request / release signal input)

As the description has been provide with priority on ports (③ and ⑥) changed from the 47C660/860. Table2-1 lists the port address assignments and the I/O instruction that can access the ports.

Port Address (**)	Port		Input/Output instructions								
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note 2)	○	○	–
02	P2 output latch	P2 output port	○	○	○	○ (Note 2)	○	○	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port (HTC input)	R4 output port (PULSE OUTPUT)	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	HTC1 counter	HTC1 register	○	○	○	–	–	–	–
0D	HTC2 counter	HTC2 register	○	○	○	–	–	–	–
0E	SIO, clock generator and Hold status (Note3)	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	——	–	–	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	Watchdog Timer control	–	○	–	–	–	–	–
16	Undefined	System clock control	–	○	–	–	–	–	–
17	Undefined	HTC1 control	–	○	–	–	–	–	–
18	Undefined	HTC2 control	–	○	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	LCD driver control 1	–	○	–	–	–	–	–
1B	Undefined	LCD driver control 2	–	○	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	Serial interface control 1	–	○	–	–	–	–	–
1F	Undefined	Serial interface control 2	–	○	–	–	–	–	–

Note1. "——" means the reserved state. unavailable for the user programs.
Note2. the 5-bit to 8-bit data conversion instruction [outb @hl], automatic access to ports p1 and p2.
Note3. the status input of serial interface, clock generator, and HOLD (KE0) pin.

Table 2-1. Port Address Assignments and Available I/O Instructions

(1) Port R4 (R43-R40)

Port R4 is a 4-bit I/O port with output latch. The latch should be set to "1" for use as an input port. During reset, the latch is initialized to "1".

The R4 port is shared with the high speed Timer/ Counter input pin and pulse output pin. The latches should be set to "1" when these pins are used for these functions. When used for normal I/O, the high speed Timer/Counter event counter mode, frequency measurement mode and pulse output mode should be disabled.

Port R4 (Port address OP04 / IP04)

3	2	1	0
R43	R42 ($\overline{\text{PULSE}}$)	R41 (HT1)	R40 (HT2)

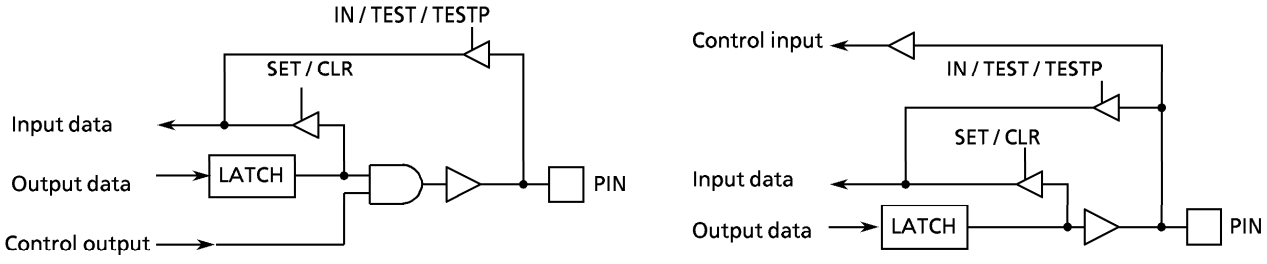


Figure 2-1. port R4

(2) Port R5 (R53-R50)

Port R5 is a 4-bit general-purpose I/O port with output latch.

(3) R83 pin

Port R8 is shared with external interrupt input and Timer/Counter input. Timer/Counter 1 is connected to HTC1 ; therefore, there is no Timer/Counter 1 external input pin (TC1).

2.2 High Speed Timer/Counter (HTC1, HTC2)

The 47C620/820 have two 8-bit high speed timer/counters for counting times or events. The event counter mode, timer mode, frequency measurement mode, and pulse output mode can be selected for the high speed timer/counters (HTC1 and HTC2).

The HTC1 can also be operated in conjunction with TC1 as a 20-bit counter. HTC2 can also output pulses. External input pins HT1 and HT2 are shared with ports R41 and R40. Pulse output pin ($\overline{PULSE}$) is shared with port R42, the corresponding R4 output latch should be set to "1" when used as external input pins and pulse output pin. R41 can be used as the normal input/output pin when HTC1 is used in the timer mode, and R40 can be used as the normal input/output pin when HTC2 is used in the pulse output mode.

2.2.1 Circuit configuration

The high speed timer/counter consists of 8-bit binary counter, preset register and clock source selector.

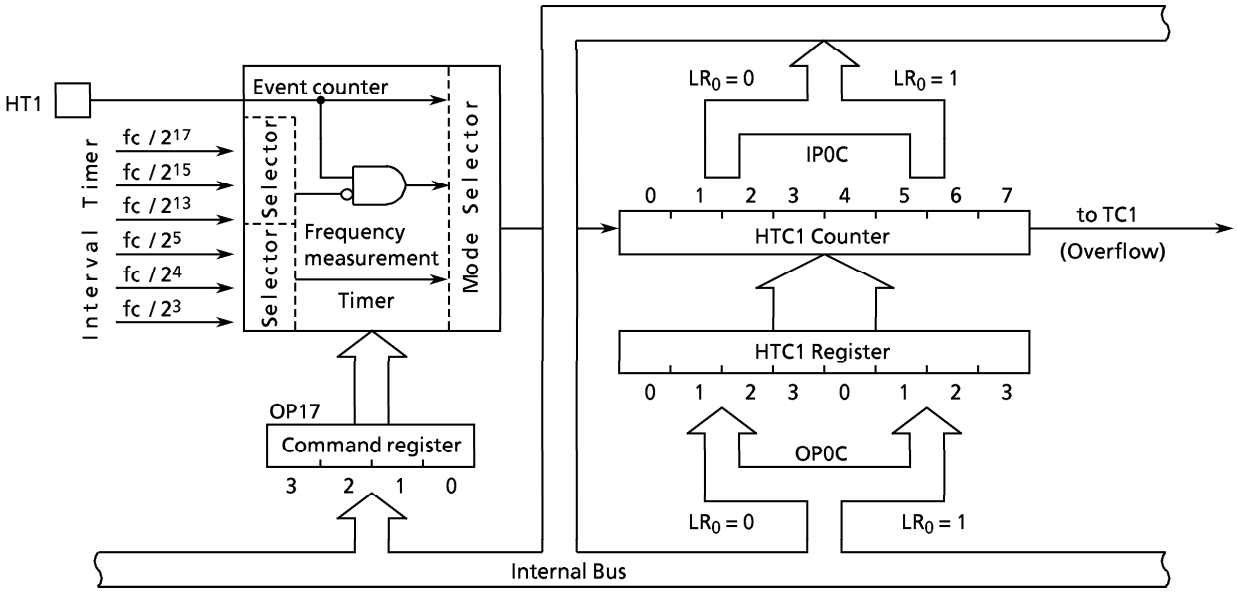


Figure 2.2. High Speed Timer/Counter 1

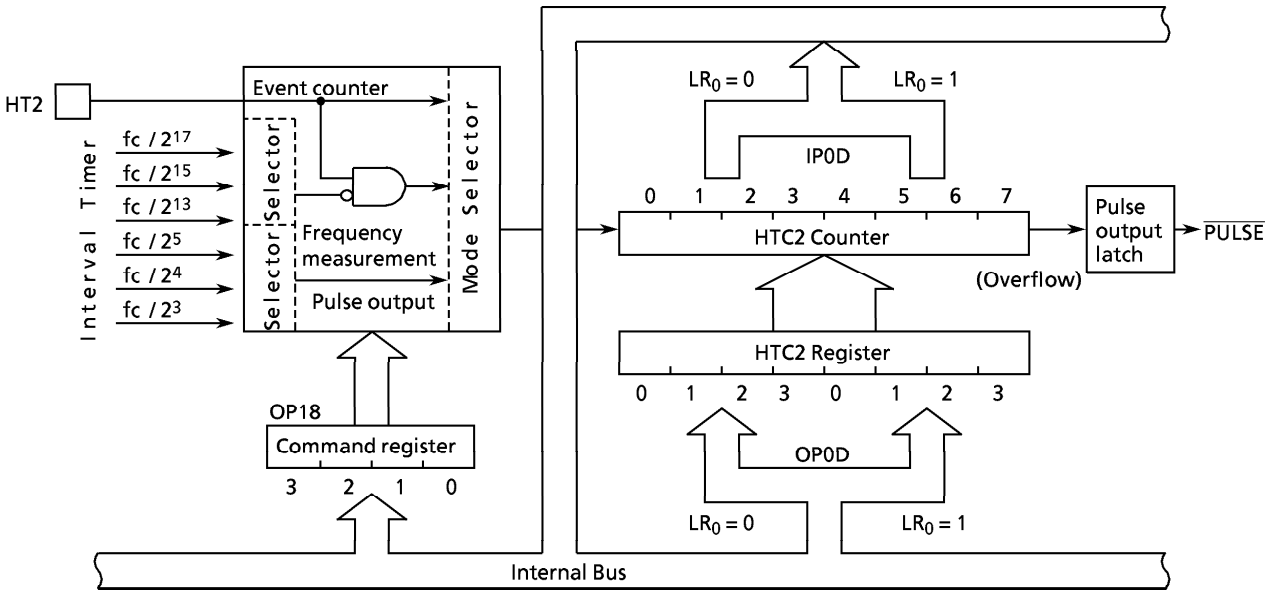


Figure 2.3. High Speed Timer/Counter 2

2.2.2 Control of High Speed Timer/Counter

The High Speed Timer/Counter is controlled by the command registers (OP17, OP18). These registers are initialized to "0" during reset.

HTC1 control command register
(Port address : OP17) (Initial value : 0000)

3	2	1	0
MODE1		EHTC1	

MODE1	Selection of count mode

00 : Frequency measurement mode
01 : Event counter mode
10 : Timer mode
11 : Reserved

EHTC1	Internal pulse rate (interval timer output) select/count start request

00 : HTC1 Disable state

	Frequency measurement mode window gate width	Timer mode Internal pulse rate
01 :	$fc/2^{13}$ or $fs/2^{3}$ [Hz]	$fc/2^{3}$ [Hz]
10 :	$fc/2^{15}$ or $fs/2^{8}$	$fc/2^{4}$
11 :	$fc/2^{17}$ or $fs/2^{10}$	$fc/2^{5}$

HTC2 control command register
(Port address : OP18) (Initial value : 0000)

3	2	1	0
MODE2		EHTC2	

MODE2	Selection of count mode

00 : Frequency measurement mode
01 : Event counter mode
10 : Reserved
11 : Pulse output mode

EHTC2	Internal pulse rate (interval timer output) select/count start request

00 : HTC2 Disable state

	Frequency measurement mode window gate width	Pulse output mode Internal pulse rate
01 :	$fc/2^{13}$ or $fs/2^{3}$ [Hz]	$fc/2^{3}$ [Hz]
10 :	$fc/2^{15}$ or $fs/2^{8}$	$fc/2^{4}$
11 :	$fc/2^{17}$ or $fs/2^{10}$	$fc/2^{5}$

Note . fc ; High-frequency clock [Hz]
fs ; Low-frequency clock [Hz]

Figure 2-4. HTC1, HTC2 control Command register

2.2.3 Function of High Speed Timer/Counter

The High Speed Timer/Counters (HTC1 and HTC2) consist of presettable 8-bit binary counters and clock source selectors. Either internal or external pulses can be selected by command register as the clock source for the event counter, timer, frequency measurement and pulse output modes. HTC1 and HTC2 increment at the rising edges of the clock pulses. Counting starts at the first rise of the clock pulse after a command is loaded into the command register.

(1) Setting of preset value

Values can be preset in the 8-bit binary counter. Values can be loaded to the binary counter when counting starts or when an overflow occurs by writing them to the HTC1 and HTC2 registers. Thus, preset values can be changed when the next overflow occurs by writing them during counting. Port addresses OP0C and OP0D are used for writing preset values as shown in Table 2-2. Preset values are written to the lower 4 bits when LR_0 (bit 0 of L register) = 0 and to the upper 4 bits when LR_0 = 1. The register is initialized to "0" during reset.

Port address	LR_0	Access register
OP0C	0	The Lower 4-bits of HTC1 register
	1	The upper 4-bits of HTC1 register
OP0D	0	The Lower 4-bits of HTC2 register
	1	The upper 4-bits of HTC2 register

Table 2-2. Writing of preset value

(2) Reading of Count Value

Count values of the 8-bit binary counter are read out from port addresses IP0C and IP0D as shown in Table 2-3. The lower 4 bits are read out when LR_0 = 0 and the upper 4 bits are read out when LR_0 = 1. Read out is unstable during counting, so stop counting before reading out. The counter is initialized to "0" during reset.

Port address	LR_0	Reading count values
IP0C	0	The Lower 4-bits of HTC1 counter
	1	The upper 4-bits of HTC1 counter
IP0D	0	The Lower 4-bits of HTC2 counter
	1	The upper 4-bits of HTC2 counter

Table 2-3. Reading of count value

(3) 20-bit Counter Function

The HTC1 counter is connected to TC1 (12-bit Timer/Counter) and can operate as 20-bit counter when TC1 is set to the event counter mode. In this case, TC1 increments when HTC1 overflows. The TC1 input (T1) is connected to HTC1 and can only be used as an event counter when set to the event counter mode (linked to HTC1) or a timer when set to the timer mode.

When used as a 20-bit counter in the timer, event counter and frequency measurement mode described later, the HTC1 tends to overflow more often when applied frequencies are high and preset values are large; therefore, there may be counting errors. Consequently, it is necessary to set the applied frequency and preset value so that HTC1 overflows occur at the rate of no more than once per 8 instruction cycles.

2.2.4 Function of High Speed Timer/Counter

(1) Event counter mode

The counter increments for each rising edge of the external pin (HT1, HT2) input. The maximum applied frequency for HT1 and HT2 is fc [Hz].

Example : Reading count values and Enable of Event Count mode

```
LD      A, #0100B       ; Sets the Event count mode of HTC2
OUT     A, %OP18
 ⋮                      ; Counting
LD      A, #0000B       ; Stops the Event counter mode of HTC2
OUT     A, %OP18
LD      HL, #50H        ; RAM [50H] ← Lower 4-bit by HTC2 register
IN      %IP0D, @HL
INC     L               ; RAM [51H] ← Upper 4-bit by HTC2 register
IN      %IP0D, @HL
```

(2) Timer mode (HTC1)

The counter increments at the rising edges of internal pulses generated by the interval timer. Three differnt internal pulse rates can be selected using the command register. HTC1 is connected to TC1; therefore, optional high-resolution times can be obtained by loading the initial values into the HTC1 register (OP0C) or TC1 counter register (addresses F4-F6$_H$ of DMB0) and generating overflow interrupt of TC1.

Example : After setting preset value, sets the timer mode of HTC1 and the Event Counter mode of TC1.

```
LD      L, #0000B       ; LR0 ← 0
OUT     #5H, %OP0C      ; Sets "5" in Lower 4-bit of HTC1 register
LD      L, #0001B       ; LR0 ← 1
OUT     #0AH, %OP0C     ; Sets "A" in Upper 4-bit of HTC1 register
CLR     DMB             ; Sets "000H" in HTC1 register
ST      #0H, @HL+
ST      #0H, @HL+
ST      #0H, @HL+
LD      A, #0100B       ; Sets the Event counter mode of TC1
OUT     A, %OP1C
LD      A, #1001B       ; Sets the Timer mode of HTC1
OUT     A, %OP17
 ⋮                      ; Counting
```

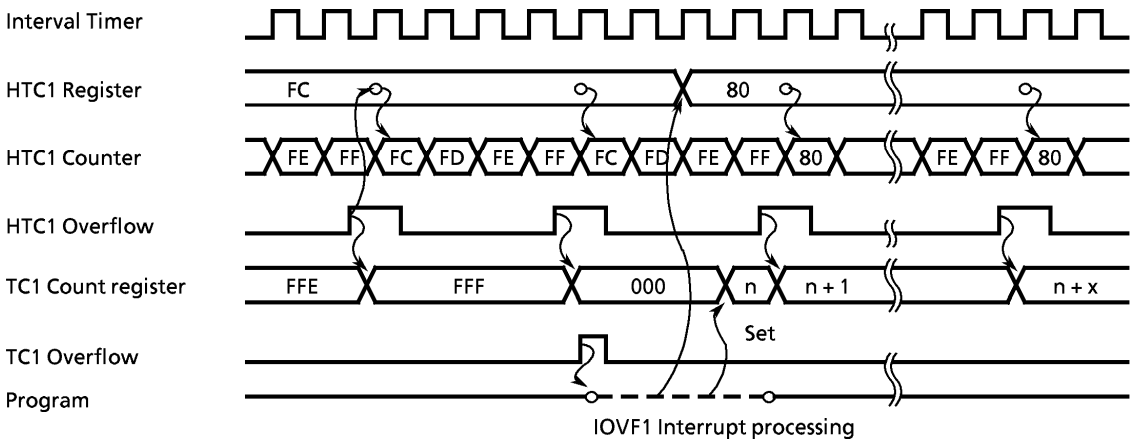


Figure 2-5. Timer mode

(3) Frequency measurement mode

The window gate width (from interval timer output fall to rise) interval specified by the command register and the rising edges of pulses applied to HT1 and HT2 are counted in this mode. The value of the window gate width setting is the same as the interval timer interrupt frequency; therefore, by enabling interval timer interrupt, an ITMR interrupt request can be generated when counting ends. Normally, the content of the HTC counter is read and initialized in the ITMR interrupt service routine in preparation for the next count.

Maximam input frequency of HT1, HT2 are fc [Hz].

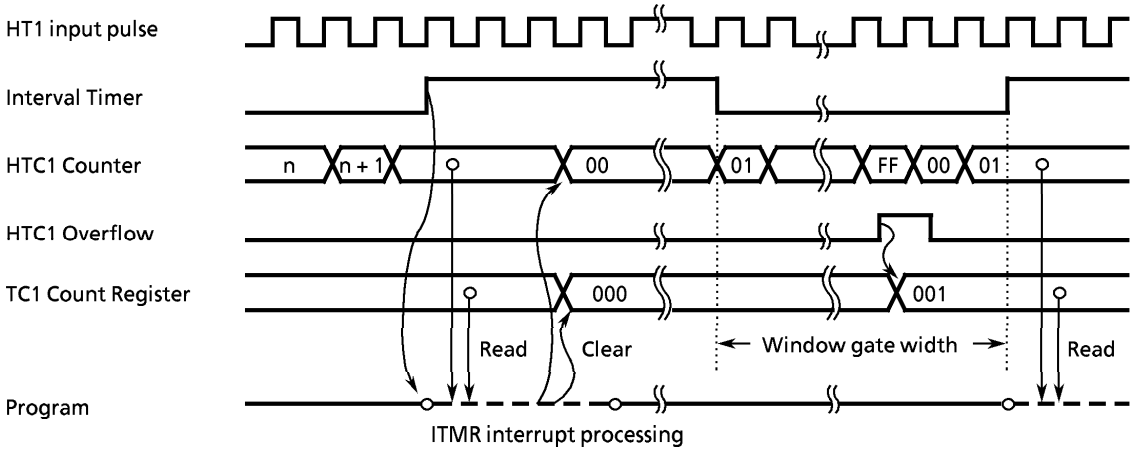


Figure 2-6. Frequency measurement mode

(4) Pulse output mode (HTC2)

Pulses of optional frequency are output to the $\overline{\text{PULSE}}$ pin in this mode. HTC2 counter overflows repeatedly set and clear the pulse output latch. The $\overline{\text{PULSE}}$ output pin is shared by the R42 output pin, in which case the R42 output latch should be set to "1". The pulse output latch is initialized to "0" and the $\overline{\text{PULSE}}$ output becomes "H" during reset.

A total of 765 different output frequencies (fo) can be set using clock sources (3 can be selected with the command register) and preset values. One pulse output cycle (1/fo) is expressed with the follwing formula.

$$\frac{1}{fo} = 2 \times \frac{1}{(\text{Internal pulse rate})} \times \{256 - (\text{preset value})\}$$

(Preset value = 0 to 254)

Example: Calculating maximum output frequency (at fc = 4MHz)

$$fo\ \text{max.} = \frac{1}{2} \times \frac{fc}{2^3} \times \frac{1}{256 - 254} = \frac{4 \times 10^6}{32} = 125\ [\text{kHz}]$$

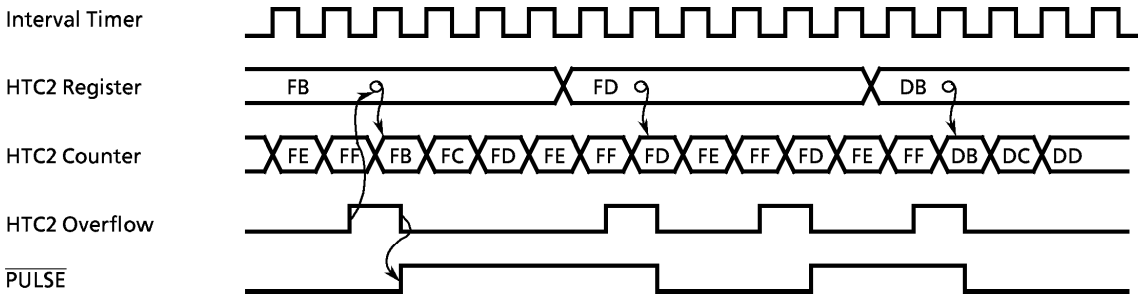


Figure 2-7. Pulse output mode

2.3 LCD Driver

The 47C620/820 have the circuit that directly drives the liquid crystal display (LCD) and its control circuit.

The 47C620/820 have the following connecting pins with LCD.

① Segment output port 32 pins (SEG31-SEG0)
② Common output port 4 pins (COM4-COM1)

In addition, VLC pin is provided as the drive power pin.

The devices that can be directly driven is selectable from LCD of the following drive methods.

① 1 / 4 Duty (1 / 3 Bias) LCD ····· Max. 128 Segment (16 digits × 8 segments)
② 1 / 3 Duty (1 / 3 Bias) LCD ····· Max. 96 Segment (12 digits × 8 segments)
③ 1 / 3 Duty (1 / 2 Bias) LCD ····· Max. 96 Segment (12 digits × 8 segments)
④ 1 / 2Duty (1 / 2 Bias) LCD ····· Max. 64 Segment (8 digits × 8 segments)
⑤ Static LCD ····· Max. 32 Segment (4 digits × 8 segments)

2.3.1 Configuration of LCD driver

Figure 2-8 shows the configuration of the LCD driver.

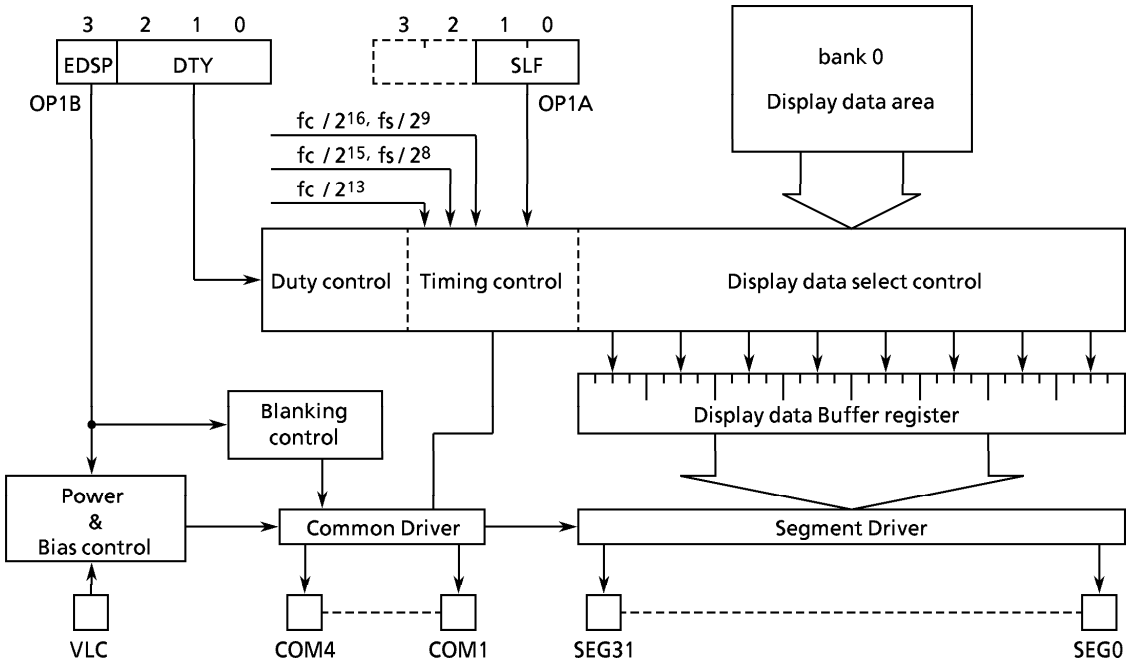


Figure 2-8. LCD Driver

2.3.2 Control of LCD driver circuit

The LCD driver is controlled by the command register 1,2 (OP1A, OP1B). Further, when the command register 1 is accessed, the most significant bit of the command register 2 must be set to "0" (Blanking).

LCD Driver control command register 1
(Port address : OP1A Initial value : 0000)

3	2	1	0
		SLF	

SLF	Selection of LCD drive frequency	
	Single Clock Mode	Dual Clock Mode
00:	fc / 2^{13} [Hz]	Unused
01:	fc / 2^{15}	fs / 2^{8} [Hz]
10:	fc / 2^{16}	fs / 2^{9}
11:	Reserved	Reserved

Note. *fc ; High-frequency clock [Hz]*
fs ; Low-frequency clock [Hz]
** ; don't care*

LCD Driver control command register 2
(Port address : OP1B Initial value : 0000)

3	2	1	0
EDSP	DTY		

EDSP	LCD Display Control
0 :	Blanking
1 :	Enables LCD display (Blanking is released)

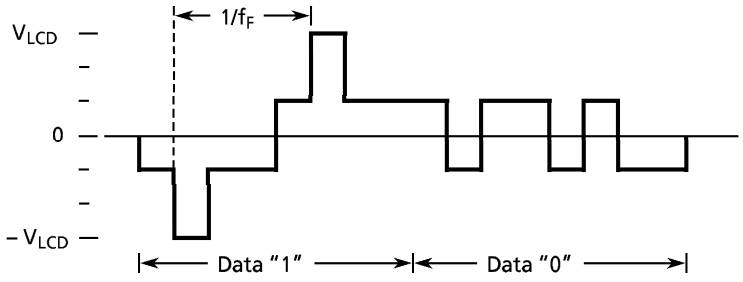
DTY	Selection of driving methods	
000:	1 / 4 Duty	(1 / 3 Bias)
001:	1 / 3 Duty	(1 / 3 Bias)
010:	1 / 3 Duty	(1 / 2 Bias)
011:	1 / 2 Duty	(1 / 2 Bias)
100:	Static	
101:	Reserved	
11*:	Reserved	

Figure 2-9. LCD Driver control Command Register

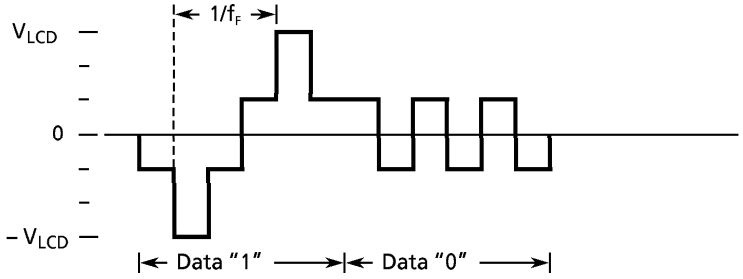
(1) Driving methods of LCD driver

Driving methods of LCD is selected 5 kind of DTY (bit 2-0 of command register 2). The drive method is initialized according to LCD used in the initial program.
Example of LCD and their drive waveform are shown in Figure 2-10.

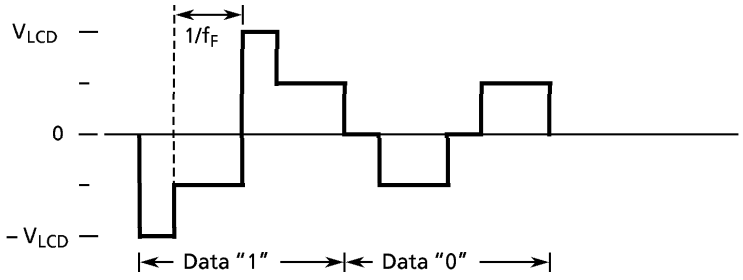
① 1 / 4 Duty (1 / 3 Bias)



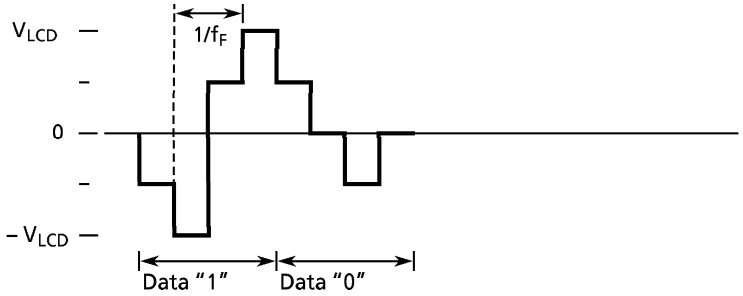
② 1 / 3 Duty (1 / 3 Bias)



③ 1 / 3 Duty (1 / 2 Bias)



④ 1 / 2 Duty (1 / 2 Bias)



⑤ Static

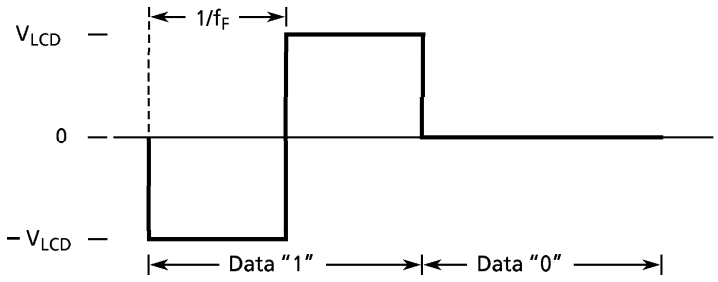


Figure 2-10. LCD drive waveform (COM-SEG pins)

(2) Frame frequency

Frame frequency (f_F) is set according to the drive method and base frequency as shown in the following table 2-4.

The base frequency is selected by SLF (the lower 2 bits of the command register) according to the reference clock frequency fc and fs.

a. At the single clock mode

SLF	BASE FREQUENCY [Hz]	FRAME FREQUENCY [Hz]			
		1 / 4 DUTY	1 / 3 DUTY	1 / 2 DUTY	STATIC
10	$\frac{fc}{2^{16}}$	$\frac{fc}{2^{16}}$	$\frac{4}{3} \cdot \frac{fc}{2^{16}}$	$\frac{4}{2} \cdot \frac{fc}{2^{16}}$	$\frac{fc}{2^{16}}$
	fc = 4MHz	61	81	122	61
01	$\frac{fc}{2^{15}}$	$\frac{fc}{2^{15}}$	$\frac{4}{3} \cdot \frac{fc}{2^{15}}$	$\frac{4}{2} \cdot \frac{fc}{2^{15}}$	$\frac{fc}{2^{15}}$
	fc = 4MHz	122	163	244	122
00	$\frac{fc}{2^{13}}$	$\frac{fc}{2^{13}}$	$\frac{4}{3} \cdot \frac{fc}{2^{13}}$	$\frac{4}{2} \cdot \frac{fc}{2^{13}}$	$\frac{fc}{2^{13}}$
	fc = 1MHz	122	163	244	122

Note . fc ; High-frequency clock [Hz]

b. At the dual clock mode

SLF	BASE FREQUENCY [Hz]	FRAME FREQUENCY [Hz]			
		1 / 4 DUTY	1 / 3 DUTY	1 / 2 DUTY	STATIC
10	$\frac{fs}{2^{9}}$	$\frac{fs}{2^{9}}$	$\frac{4}{3} \cdot \frac{fs}{2^{9}}$	$\frac{4}{2} \cdot \frac{fs}{2^{9}}$	$\frac{fs}{2^{9}}$
	fs = 32kHz	61	83	125	61
01	$\frac{fs}{2^{8}}$	$\frac{fs}{2^{8}}$	$\frac{4}{3} \cdot \frac{fs}{2^{8}}$	$\frac{4}{2} \cdot \frac{fs}{2^{8}}$	$\frac{fs}{2^{8}}$
	fs = 32kHz	125	167	250	125

Note . fs ; Low-frequency clock [Hz]

Table 2-4. Setting of LCD Frame Frequency

(3) LCD drive voltage

The LCD drive voltage (V_{LCD}) is given by the difference in potential (V_{DD}-V_{LC}) between pins VDD and VLC. Therefore, when the CPU operating voltage and LCD drive voltage are the same, the VLC pin is connected to the VSS pin.

The LCDs light only when the difference in potential between the segment output and common output is $\pm V_{LCD}$, and turn off at all other times.

During reset, the power switch of the LCD driver is turned off automatically, shutting off the VLC voltage.

Both the segment output and common output become V_{DD} level at this time and the LCDs turn off.

The power switch is turned on to supply VLC voltage to the LCD driver by setting EDSP (bit 3 of the command register 2) to "1_B". After that, the power switch will not turn off even during blanking (setting EDSP to "01_B") and the VLC voltage continues to flow.

The power switch is turned off during hold operation low power consumption by turning off the LCD. When hold operation is released the status in effect immediately before the hold operation is reinstated.

2.3.3 LCD display operation

(1) Display data setting

Display data are stored to the display data area (Max 32 words) in the data memory (bank0).

The display data stored to the display data area (address 20-3F$_H$) are read automatically and sent to the LCD driver by the hardware.

The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display data area with a program. The table look up instruction is mainly used for this overwriting.

Figure 2-11 shows the correspondence between the display data area and the SEG/COM pins. The LCD light when the display data is "1" and turn off when "0".

The number of segment which can be driven differs depending on the LCD drive method therefore, the number of display data area bits used to store the data also differs. Consequently, data memory not used to store display data and data memory for which the addresses are not connected to LCD can be used to store ordinary user's processing data.

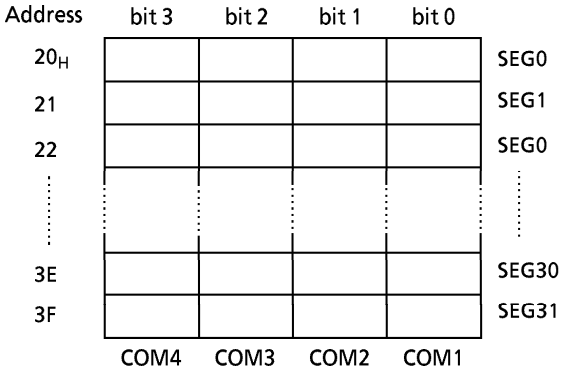


Figure 2-11. LCD Display Data Area (Bank 0)

Driving methods	bit 3	bit 2	bit 1	bit 0
1 / 4 Duty	COM4	COM3	COM2	COM1
1 / 3 Duty	–	COM3	COM2	COM1
1 / 2 Duty	–	–	COM2	COM1
Static	–	–	–	COM1

Note. – ; This bit is not used for display data.

Table 2-5. Drivinig Method and Bit for Display Data

(2) Blanking

Blanking is applied by setting EDSP to "0" and turns off the LCD by outputting the non light operation level to the COM pin.

The SEG pin continuously outputs the signal level in accordance with the display data and drive method.

With static drive, no voltage is applied between the COM and SEG pins when the LCD is turned off by data (display data cleared to "0"), but the COM pin output becomes constant at the $V_{LCD}/2$ level when turning off the LCD by blanking, so the COM and SEG pins are then driven by $V_{LCD}/2$.

2.3.4 Control method of LCD driver

(1) Initial Setting

Flow chart of intial setting are as shown in Figure 2-12.

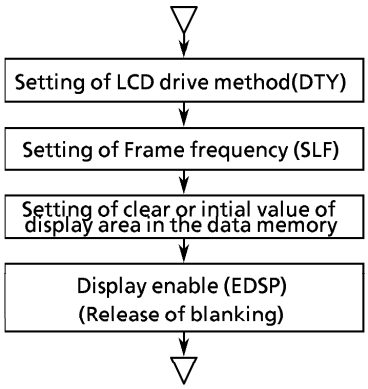


Figure 2-12. Intial setting of LCD driver

Example : When operating the 47C820 with 1/4 duty LCD using a from frequency of fc/2^{16} [Hz] .

```
LD      A,  #0000B      ; Sets the 1/4 duty drive
OUT     A,  %OP1B
LD      A,  #0010B      ; Setting of base frequency
OUT     A,  %OP1A
 ⋮                      ; Setting of clear or intial value of
 ⋮                        display area in the data memory
LD      A,  #1000B      ; Display enable
OUT     A,  %OP1B
 ⋮
```

(2) Store of display data

Normally, display data are kept permanently in the program memory and are then stored to the display data area by the table look-up instruction.

This can be explained using numerical display with 1/4 duty LCD as an example. The COM and SEG connections to the LCD are the same as those shown in Figure 2-13 and the display data are as shown in Table 2-6. Programming example for displaying numerals corresponding to BCD data stored at address 10H in the data memory is shown below.

```
        LD      HL,  #0FCH          ; To set the DC
        LD      A,     10H
        ST      A,     @HL+
        ST      #DTBL / 16,  @HL+
        ST      #DTBL / 256,  @HL+
        LD      HL,  #20H           ; Store of display data
        LDL     A,  @DC
        ST      A,  @HL+
        LDH     A,  @DC+
        ST      A,  @HL+

DTBL : DATA     11011111B,  00000110B,
               11100011B,  10100111B,
               00110110B,  10110101B,
               11110101B,  00010111B,
               11110111B,  10110111B
```

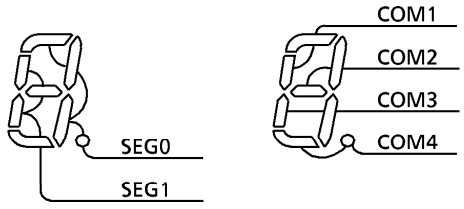


Figure 2-13. Example of COM and SEG connections

Numeric	Display	Display data		Numeric	Display	Display data	
		High order address	Low order address			High order address	Low order address
0	0.	1101	1111	5	5	1011	0101
1	1	0000	0110	6	6	1111	0101
2	2	1110	0011	7	7	0001	0111
3	3	1010	0111	8	8	1111	0111
4	4	0011	0110	9	9	1011	0111

Table 2-6. Example of display data (1/4 Duty LCD)

Table 2-6 shows the same numerical display used in Table 2-7, but using 1/2 duty LCD. The connections of the COM and SEG pins to the LCD are the same as those shown in Figure 2-14.

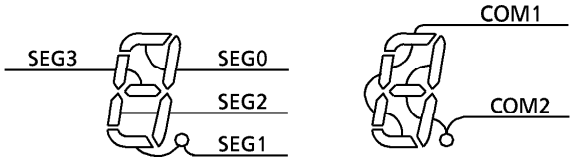


Figure 2-14. Example of COM and SEG connections

Numeral	Display data				Numeral	Display data			
	Upper			Lower		Upper			Lower
0	**01	**11	**01	**11	5	**11	**10	**01	**01
1	**00	**10	**00	**10	6	**11	**11	**01	**01
2	**10	**01	**01	**11	7	**01	**10	**00	**11
3	**10	**10	**01	**11	8	**11	**11	**01	**11
4	**11	**10	**00	**10	9	**11	**10	**01	**11

Note. * : *don't care*

Table 2-7. Example of display data (1/2 Duty LCD)

(3) Example of drive output

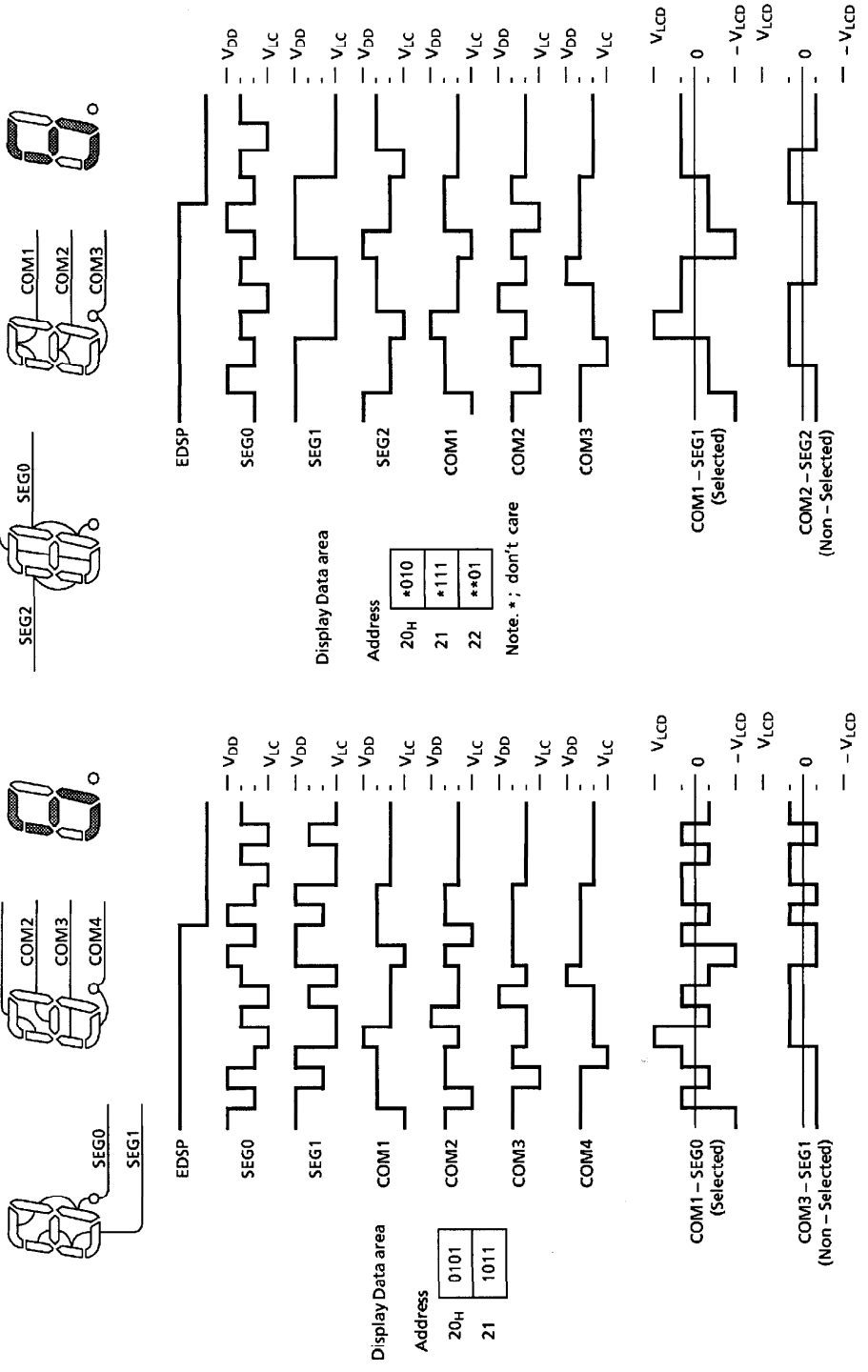


Figure 2-15. 1/4 Duty (1/3 Bias) Drive

Figure 2-16. 1/3 Duty (1/3 Bias) Drive

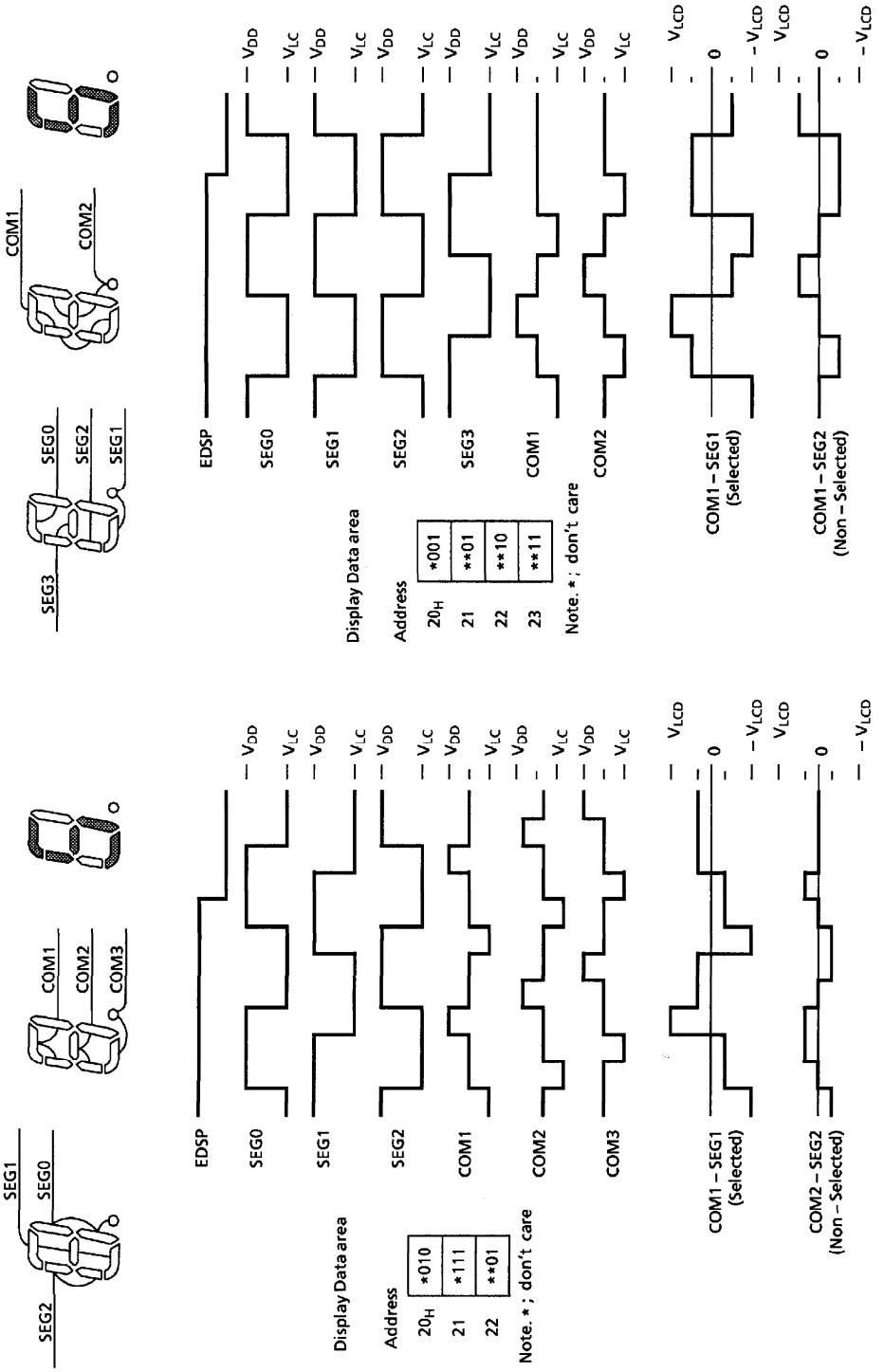


Figure 2-18. 1/2 Duty (1/2 Bias) Drive

Figure 2-17. 1/3 Duty (1/2 Bias) Drive

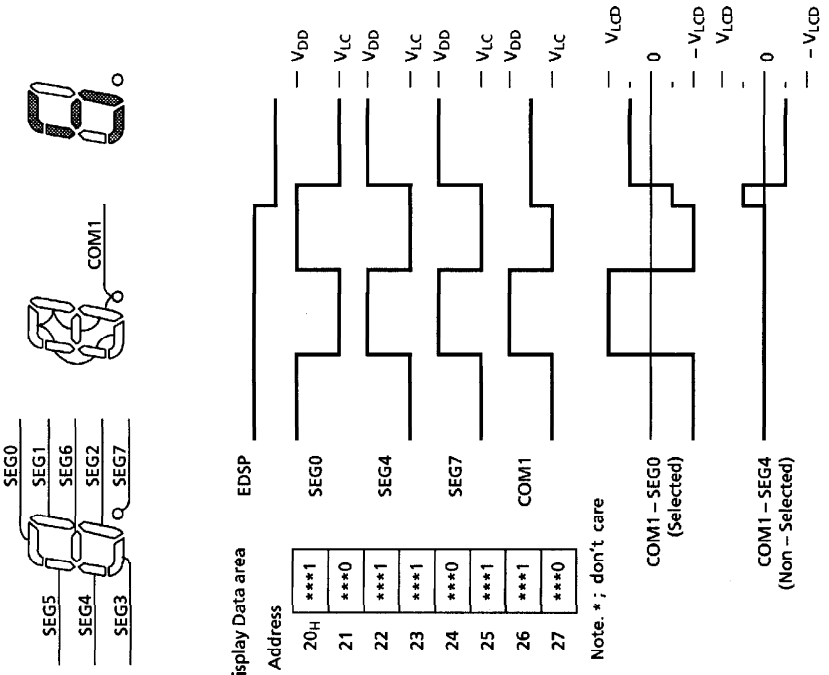


Figure 2-19. Static Drive

Port Condition by RESET Operation

The transition of Port condition by RESET operation is shown as below.

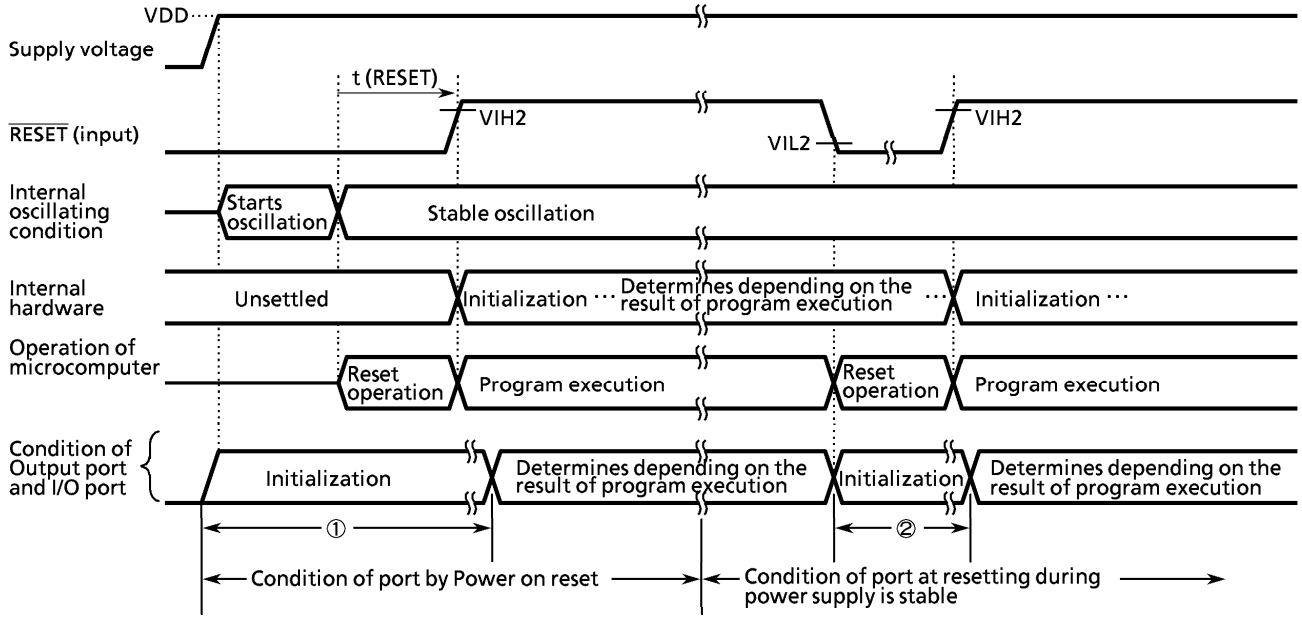


Figure 2-20. Port condition by Reset operation

Note 1: t (RESET) > 24/fc

Note 2: VIL2 : Stands for low level input voltage of $\overline{\text{RESET}}$ *pin.*
VIH2 : Stands for high level input voltage of $\overline{\text{RESET}}$ *pin.*

Note 3: The term from power on reset to the time program is executed (above ①) and also the term starting from reset operation during power supply is stable to the program is executed (above ②), the port is on the initial condition. The initial condition of Port differs from I/O circuit by each port, refer to the section of "INPUT/OUTPUT CIRCUITRY". Thus, when using Port as an output pin, in the term of the above ① and ②, the voltage level on the signal that connects with the output pin of Port to the input pin of external application circuit should be determined by the external circuitry such as pull-up resistor and / or pull-down resistor.

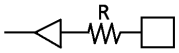
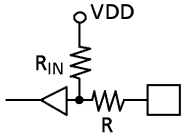
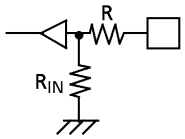
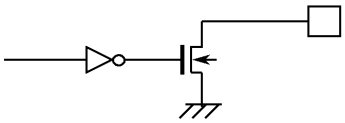
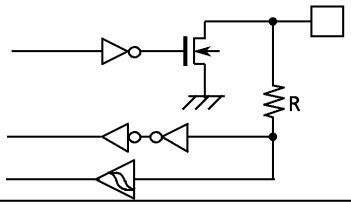
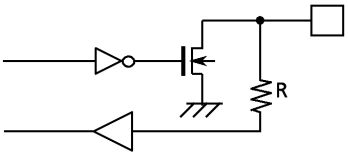
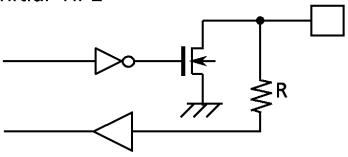
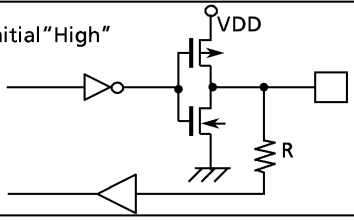
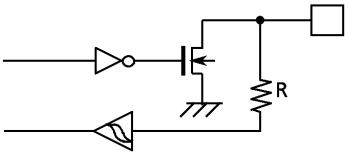
Input / Output Circuitry

(1) Control pins

The input/output circuitries of the 47C620/820 control pins are similar to those of the 47C660/860.

(2) I/O Ports

The input/output circuitries of the 47C620/820 I/O ports are shown as belows, any one of the circuitries can be chosen by a code (GA to GF) as a mask option.

Port	I/O	Input / Output Circuitry and Code			Remarks
		GA, GD	GB, GE	GC, GF	
K0	Input				Pull-up/pull-down resistor R_{IN} = 70 kΩ (typ.) R = 1 kΩ (typ.)
P1 P2	Output				Sink open drain output Initial "Hi-Z" High current I_{OL} = 10 mA (typ.)
R40 R41	I/O				Sink open darin output Initial "Hi-Z" (Hysteresis) = Input (HTC) R = 1 kΩ (typ.)
R42 R43 R7	I/O				Sink open drain output Initial "Hi-Z" R = 1 kΩ (typ.)
R6 R5	I/O	GA, GB, GC Initial "Hi-Z" 	GD, GE, GF Initial "High" 		Sink open drain output or Push-pull output R = 1 kΩ (typ.)
R8 R9	I/O				Sink open drain output Initial "Hi-Z" Hysteresis input R = 1 kΩ (typ.)

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 7	V
Supply Voltage (LCD drive)	V_{LC}		– 0.3 to V_{DD} + 0.3	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin without port R7	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin without port R7	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	15	mA
	I_{OUT2}	Ports R4 to R9	3.2	
Output Current (Total)	ΣI_{OUT}	Ports P1, P2	60	mA
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Opeating Conditions (V_{SS} = 0 V, Topr = – 40 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Input voltage V_{IH3}, V_{IL3}: In the SLOW or HOLD mode.

D.C. Characteristics (V_{SS} = 0V, Topr = – 40 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V,	–	–	± 2	μA
	I_{IN2}	Open drain R port	V_{IN} = 5.5 V / 0 V				
Input Low Current	I_{IL}	Push-pull R port	V_{DD} = 5.5 V, V_{IN} = 0.4 V	–	–	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down resistor		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Open drain R port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
Output High Voltage	V_{OH}	Push-pull R port	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and ports P1, P2	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output Low Current	I_{OL}	Ports P1, P2	V_{DD} = 4.5 V, I_{OL} = 1.0 V	–	10	–	mA
Segment Output Low Resistance	R_{OS1}	SEG pin	V_{DD} = 5 V, V_{DD} – V_{LC} = 3 V	–	20	–	kΩ
Common Output Low Resistance	R_{OC1}	COM pin					
Segment Output High Resistance	R_{OS2}	SEG pin		–	200	–	
Common Output High Resistance	R_{OC2}	COM pin					
Segment / Common Output Voltage	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V, V_{LC} = V_{SS} fc = 4 MHz	–	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0 V, V_{LC} = V_{SS} fs = 32.768 kHz	–	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	–	0.5	10	μA

Note1: Typ. values show those at Topr = 25°C, V_{DD} = 5 V.

Note2: Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up / pull-down) is contained.

Note3: Output Resistance R_{OS}, R_{OC} ; Shows on-resistance at the level switching.

Note4: $V_{O2/3}$; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note5: $V_{O1/2}$; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.

Note6: $V_{O1/3}$; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note7: Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3 V / 0.2 V
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.
Supply Current I_{DDS} ; VIN = 2.8 V / 0.2 V Only low frequency clock is only oscillated (connecting XTIN, XTOUT).

Note8: When using LCD, it is necessary to consider values of $R_{OS1/2}$ and $R_{OC1/2}$.

Note9: Times for SEG / COM output switching on ; R_{OS1}, R_{OC1}: 2/fs (s)
R_{OS2}, R_{OC2}: 1/(n · f_F)
(1/n: duty, f_F: frame frequency)

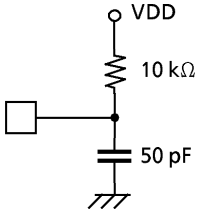
A.C. Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, Topr = – 40 to 70°C)

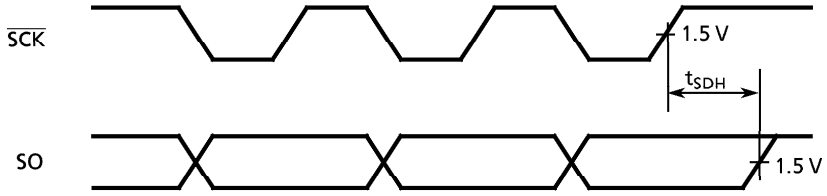
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Instruction Cycle Time	tcy	In the Normal mode	1.3	—	20	μs
		In the SLOW mode	235	—	267	μs
High Level Clock Pulse Width	t_{WCH}	For external clock operation	80	—	—	ns
Low Level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		0.5 tcy – 300	—	—	ns
High Speed Timer / Counter input frequency	f_{HT}		—	—	fc	MHz

Note: Shift data Hold time:

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)

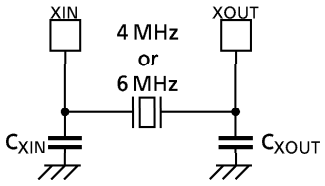


Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 40 to 70°C)

(1) 6 MHz
Ceramic Resonator

CSA6.00MGU	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-6.00MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF

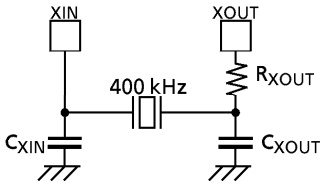


(2) 4 MHz
Ceramic Resonator

CSA4.00MG	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4.00MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF

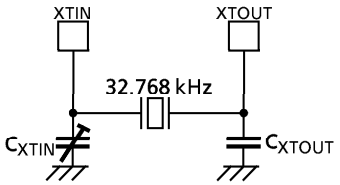
Crystal Oscillator

204B-6F 4.0000	(TOYOCOM)	$C_{XIN} = C_{XOUT}$ = 20 pF



(3) 400 kHz
Ceramic Resonator

CSB400B	(MURATA)	$C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ
KBR-400B	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ



(4) 32.768 kHz (V_{SS} = 0V, V_{DD} = 2.7 to 6.0 V, T_{opr} = – 40 to 70°C)
Crystal Oscillator C_{XTIN}, C_{XTOUT} ; 10 to 33 pF

Note: In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.

Typical Characteristics