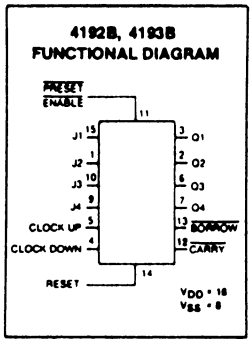
CMOS PRESETTABLE UP-DOWN COUNTERS
(Dual Clock with Reset)

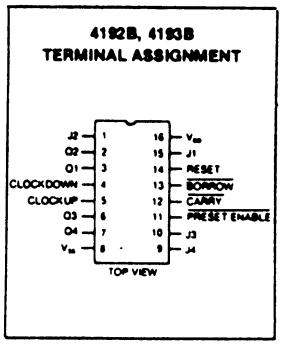
FEATURES:

- **Individual clock lines for counting up or counting down**
- **Synchronous high-speed carry and borrow propagation delays for cascading**
- **Asynchronous reset and preset capability**
- **Medium-speed operation—f_{CL} = 8 MHz (typ.) @ 10 V**

APPLICATIONS:

- **Up/down difference counting**
- **Multistage ripple counting**
- **Synchronous frequency dividers**
- **A/D and D/A conversion**
- **Programmable binary or BCD counting**





DESCRIPTION:

The 4192B Presettable BCD Up/Down Counter and the 4193B Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a PRESET ENABLE control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as CARRY and BORROW outputs for multiple-stage counting schemes are provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the PRESET ENABLE control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

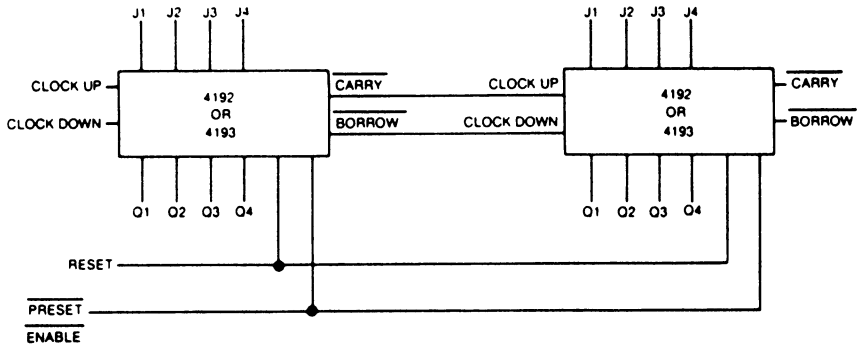
The CARRY and BORROW signals are high when the counter is counting up or down. The CARRY signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The BORROW signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the BORROW and CARRY outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

The 4192B and 4193B types are supplied in 16-lead hermetic dual-in-line ceramic packages (C and D suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (F suffix), and in chip form (H suffix).

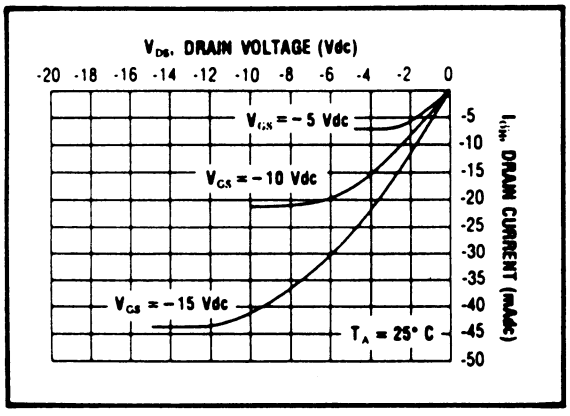
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.04	5	–	150	μAdc
		10	All valid input	–	10	–	0.04	10	–	300	
		15	combinations	–	20	–	0.04	20	–	600	

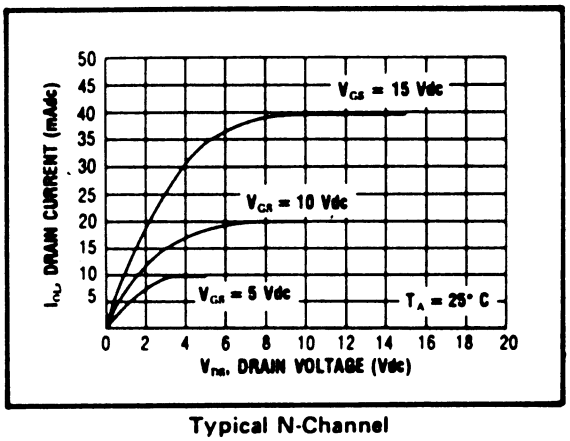
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E



Cascaded counter packages.



Typical P-Channel
Source Current Characteristics

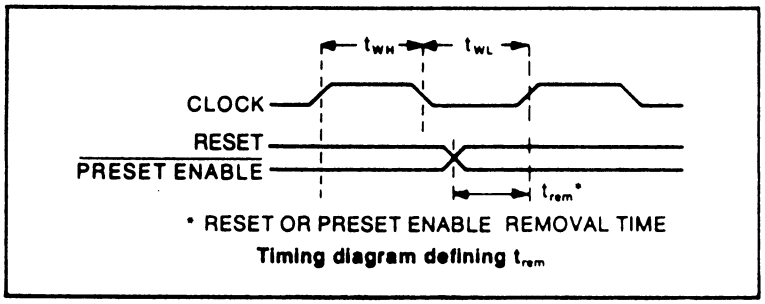


Typical N-Channel
Sink Current Characteristics

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		−55 to +125	°C
E		−40 to +85	°C



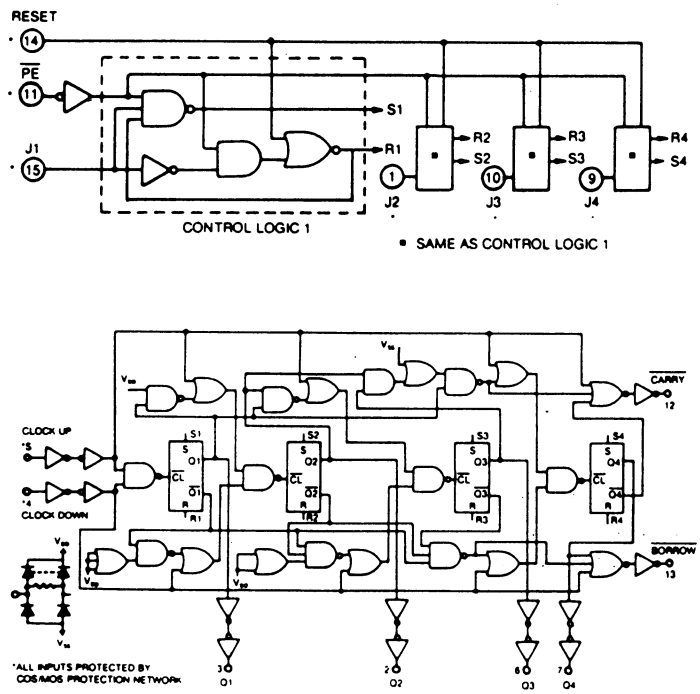
Timing diagram defining t_{rem}

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

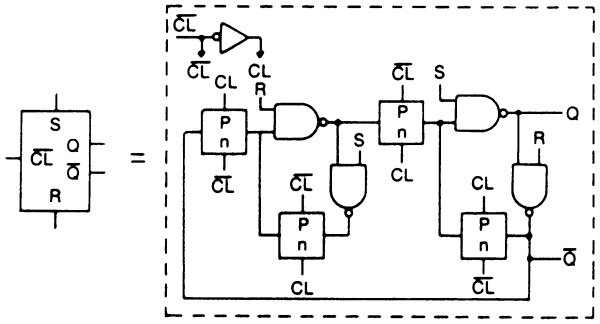
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time t_{PHL}, t_{PLH}: CLOCK UP or CLOCK DOWN to Q, RESET to Q	5	—	250	500	ns
	10	—	120	240	
	15	—	90	180	
$\overline{PE}$ to Q	5	—	200	400	ns
	10	—	100	200	
	15	—	70	140	
CLOCK UP to $\overline{CARRY}$, CLOCK DOWN to $\overline{BORROW}$	5	—	160	320	ns
	10	—	80	160	
	15	—	60	120	
$\overline{RESET}$ or $\overline{PE}$ to $\overline{BORROW}$ or $\overline{CARRY}$	5	—	300	600	ns
	10	—	150	300	
	15	—	110	220	
Transition Time, t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Min. Removal Time, t_{rem}* RESET or PE	5	—	40	80	ns
	10	—	20	40	
	15	—	15	30	
Min. Pulse Width, t_W RESET	5	—	240	480	ns
	10	—	150	300	
	15	—	130	260	
$\overline{PE}$	5	—	120	240	ns
	10	—	85	170	
	15	—	70	140	
CLOCK	5	—	90	180	ns
	10	—	45	90	
	15	—	30	60	
Max. Clock Input Frequency, f_{CL}	5	2	4	—	MHz
	10	4	8	—	
	15	5.5	11	—	
Clock Rise & Fall time, t_r, t_f	5	—	—	15	µs
	10	—	—	15	
	15	—	—	5	
Input Capacitance, C_{IN}: RESET	—	—	10	15	pF
All Other Inputs	—	—	5	7.5	pF

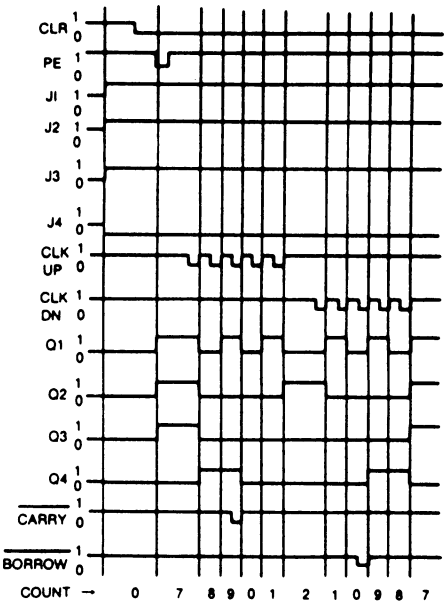
*The time required for RESET or PRESET ENABLE control to be removed before clocking (see timing diagram).



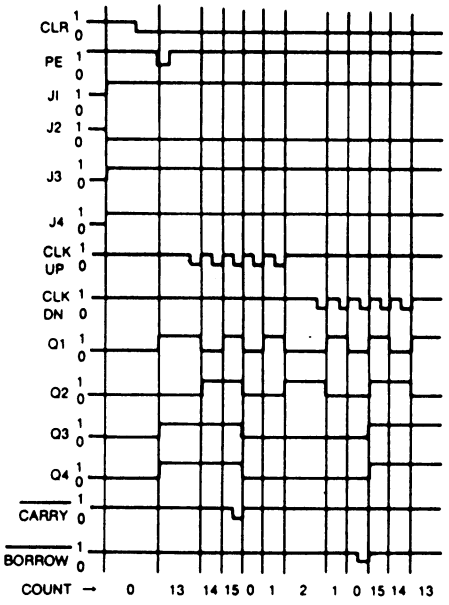
4193B logic diagram (binary).



Internal logic of Flip-flop.



4192B timing diagram.

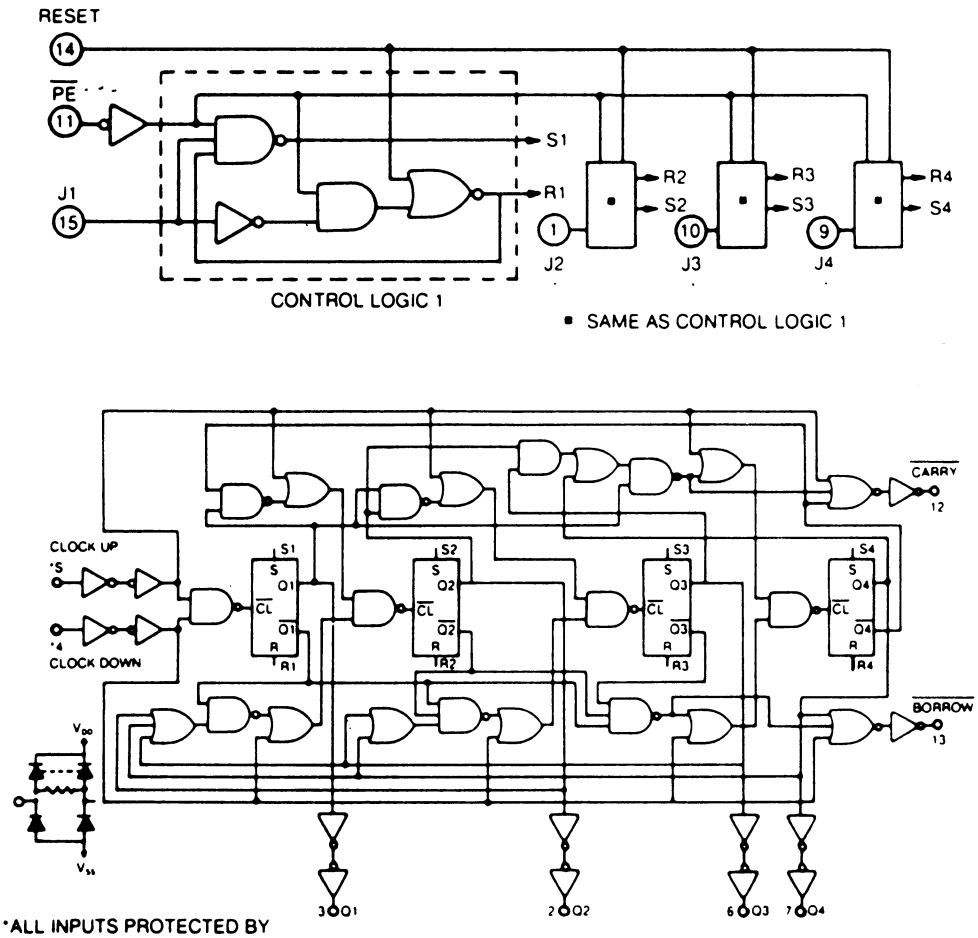


4193B timing diagram.

TRUTH TABLE

CLOCK UP	CLOCK DOWN	$\overline{\text{PRESET}}$ $\overline{\text{ENABLE}}$	RESET	ACTION
⌐¬	1	1	0	COUNT UP
¬⌐	1	1	0	NO COUNT
1	⌐¬	1	0	COUNT DOWN
1	¬⌐	1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	RESET

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE



4192B logic diagram (BCD).