Phase Control Thyristors

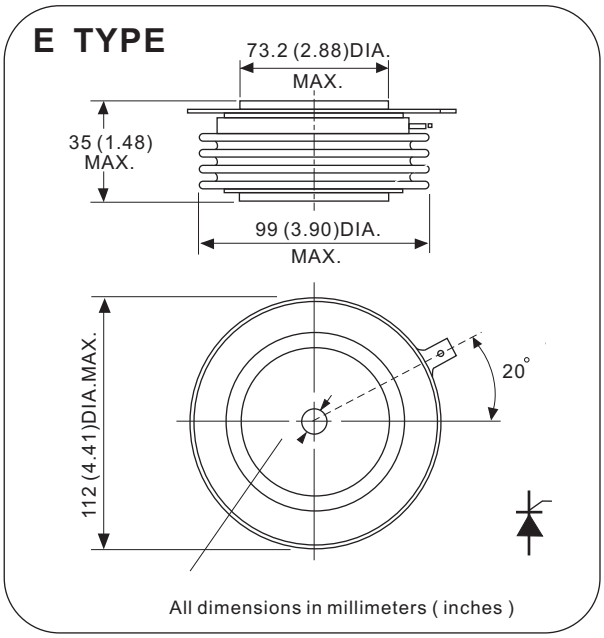
Features

1. Center amplifying gate.
2. Metal Case With Ceramic insulator.
3. Typical application
   - DC motor control
   - Controlled DC power supplies
   - AC controllers

Ordering code

4100	PT	12	E	0
(1)	(2)	(3)	(4)	(5)

(1) Maximum average on-state current , A
(2) For Phase Control Thyristor
(3) Voltage code , code x 100 = VRRM / VDRM
(4) package style : A , B , C , D ,E ,EX for Disc Type
(5) Terminal types
0 - for eyelet



Electrical Characteristics

Symbol	Parameter	Condition	Value			Unit
			Min.	Type	Max.	
$I_{T(AV)}$	Mean on-state current	180° half sine wave , 50Hz Double side cooled , T_{hs} = 55°C			4100	A
$I_{T(RMS)}$	Max. RMS on-state current	Double side cooled , T_{hs}=25°C			8161	A
V_{RRM} V_{DRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM} & V_{RRM} t_p=10ms V_{DsM} & V_{RsM} = V_{DRM} & V_{RRM} + 100V	800		1200	V
I_{TSM}	Surge on-state current	10 ms half sine wave V_R = 0.6V_{RRM}			60	KA
I^2t	For fusing coordination				20.5	A^2sx10^6
V_O	Threshold voltage				0.85	V
r_t	On-state slope resistance				0.07	mΩ
V_{TM}	Max. Forward voltage drop	ITM=3000A			1.55	V
I_H	Holding current	T_j=25°C			1000	mA
$d_{iT/dt}$	Cirtical rate of rise of turned-on current				150	A/μs
I_{RRM} I_{DRM}	Repetitive peak reverse current	V_R=V_{RRM} V_D=V_{DRM}			200	mA
$d_{v/dt}$	Cirtical rate of rise of off-state voltage	V_{DM}=0.67 V_{DRM}	1000			V/μs
P_G	Mean forward gate power				5	W
I_{GT}	Gate trigger current	V_A=12V , I_A=1A			300	mA
V_{GT}	Gate trigger voltage				3.0	V
V_{GD}	DC voltage notto trigger	At76% V_{DRM} , T_j=T_j MAX			0.25	V
T_j	Max.operating temperaturerange		- 40		125	°C
T_{stg}	Storage temperature		- 40		150	°C
$R_{th(c-h)}$	Thermal resistance(junction to heatsink)	Double side cooled , clamping force 8.0 KN			0.011	K/ W
Fm	Mounting force		35		47	KN
w_t	Approximate weight			1600		g

Figure 1 - On-state characteristics of Limit device

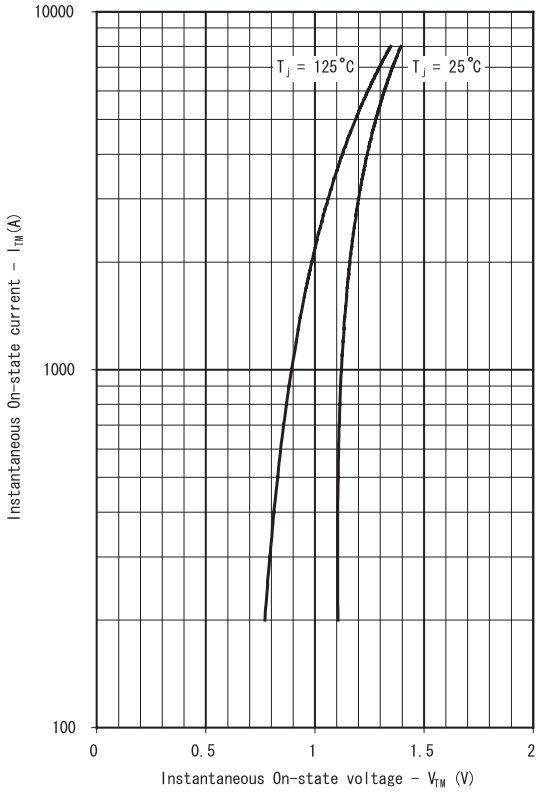


Figure 2 - Transient thermal impedance

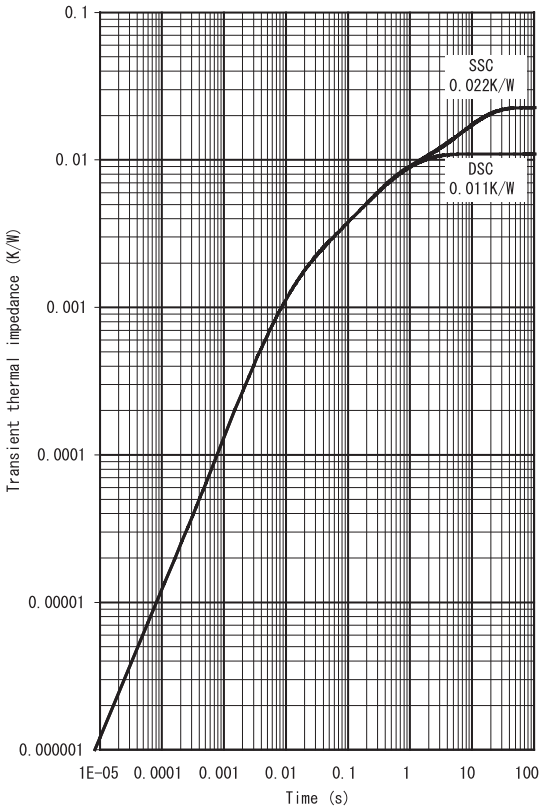


Figure 3 - Gate characteristics - Trigger limits

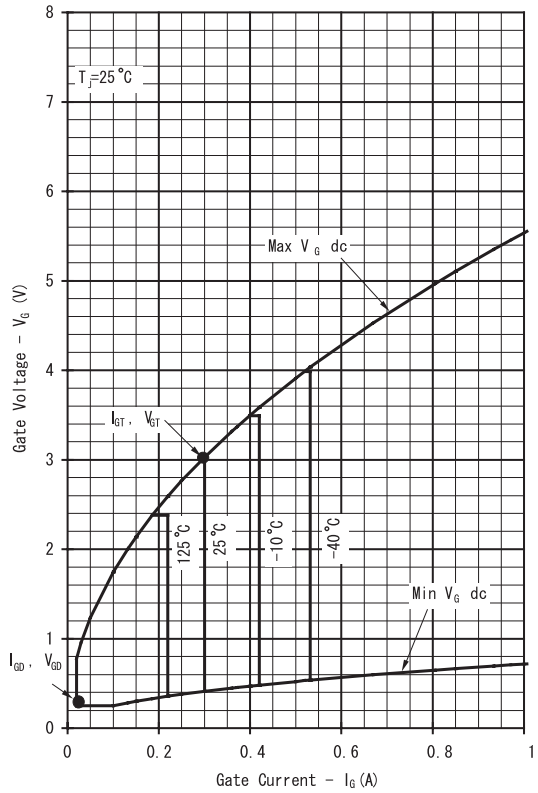


Figure 4 - Gate characteristics - Power curves

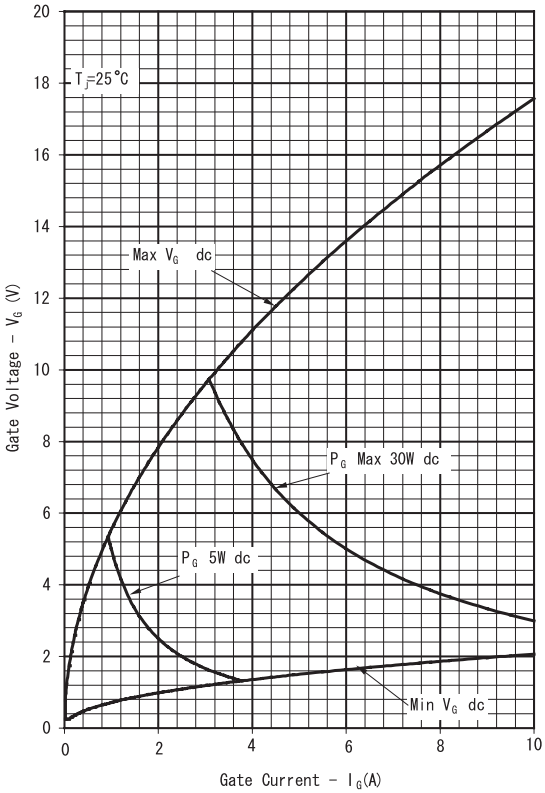


Figure 5 - Total recovered charge, Q_{rr}

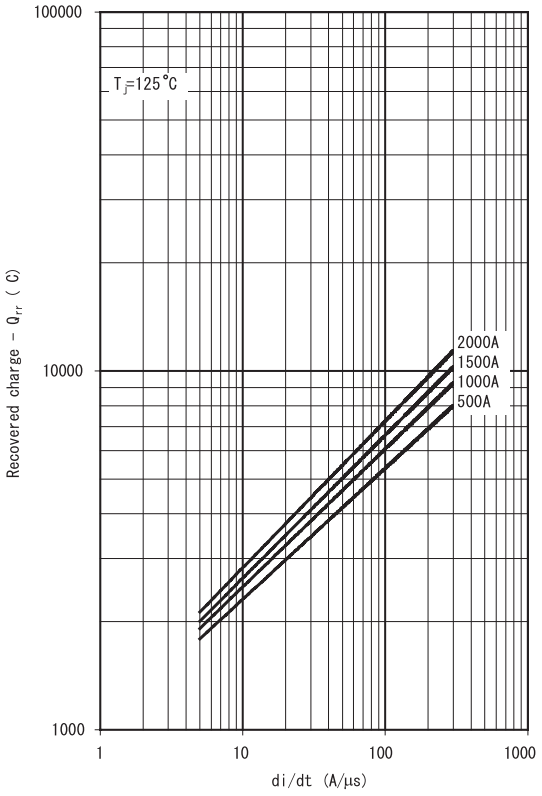


Figure 6 - Recovered charge, Q_{ra} (50% chord)

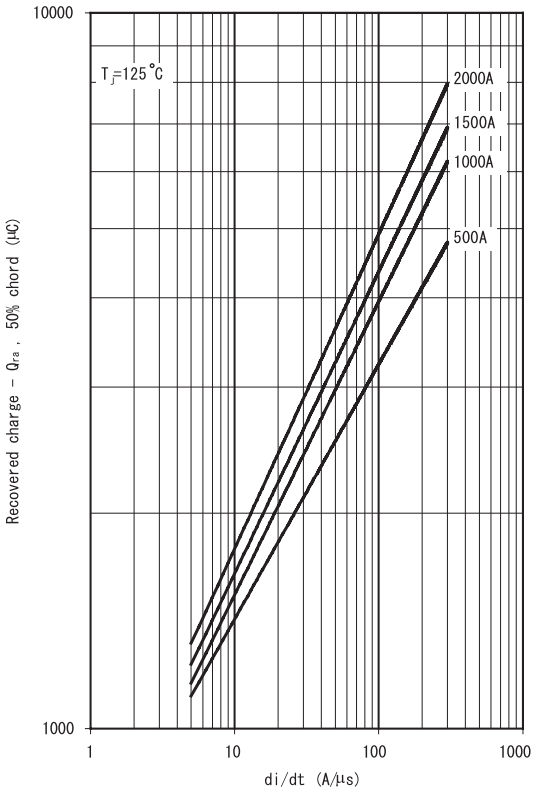


Figure 7 - Peak reverse recovery current, I_{rm}

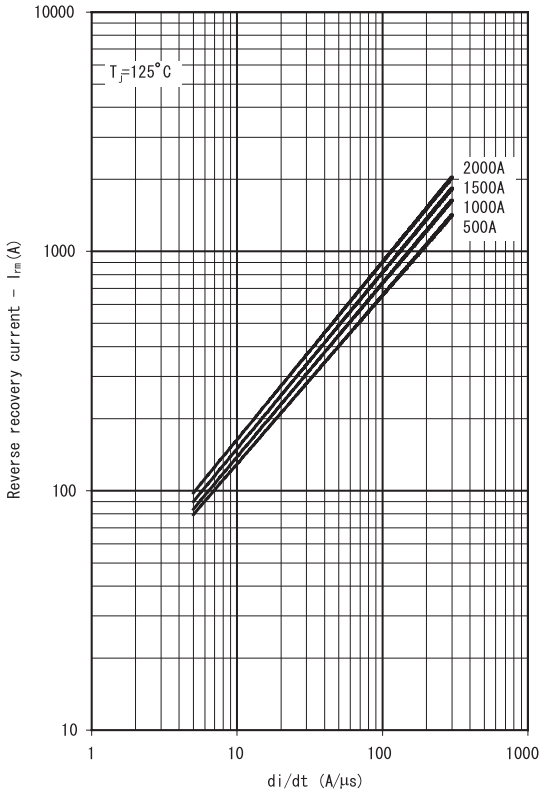


Figure 8 - Maximum recovery time, t_{rr} (50% chord)

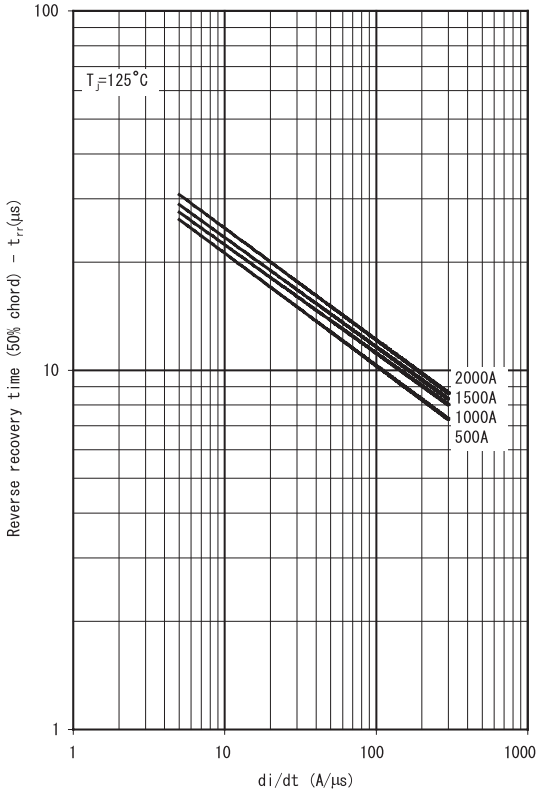


Figure 9 -n-state current vs. Power dissipation - Double Side Cooled (Sine wave)

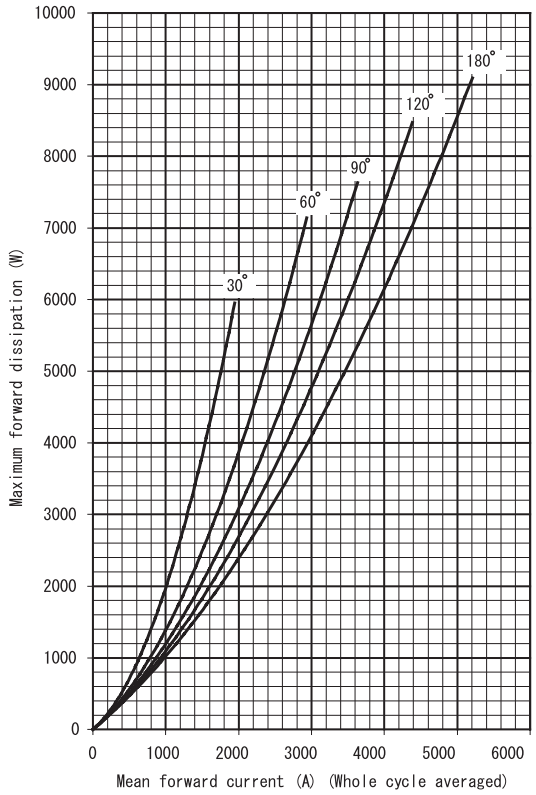


Figure 10 -On-state current vs. Heatsink temperature - Double Side Cooled (Sine wave)

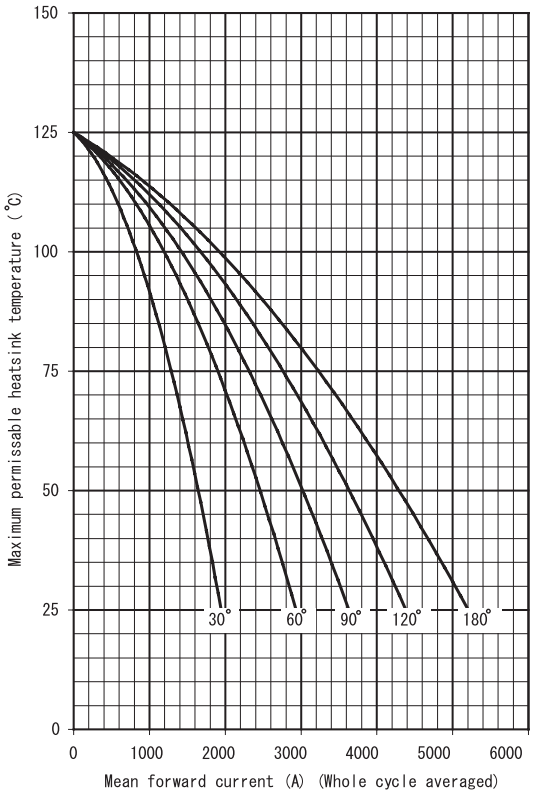


Figure 11 -On-state current vs. Power dissipation -Double Side Cooled (Square wave)

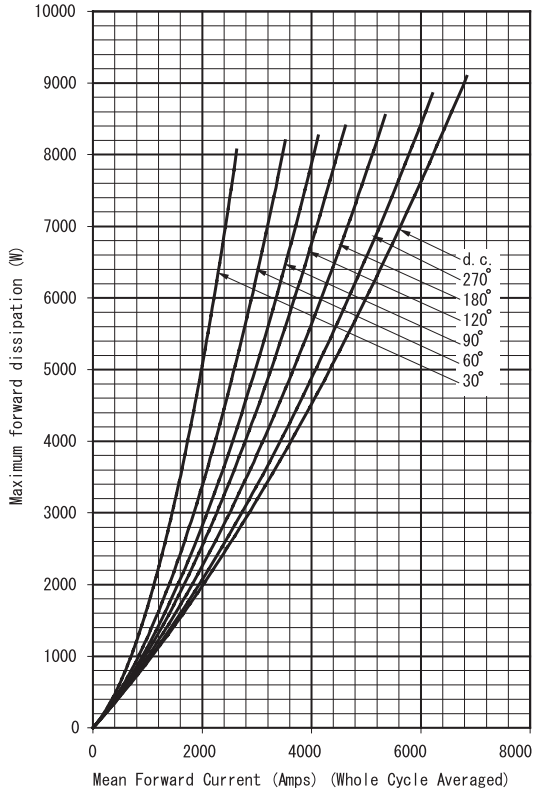


Figure 12 -On-state current vs. Heatsink

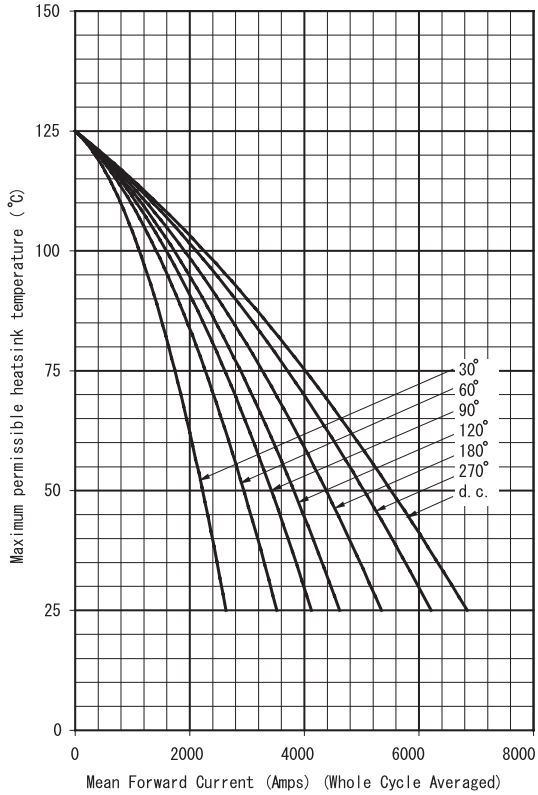


Figure 13 -On-state current vs. Power dissipation -Single Side Cooled (Sine wave)

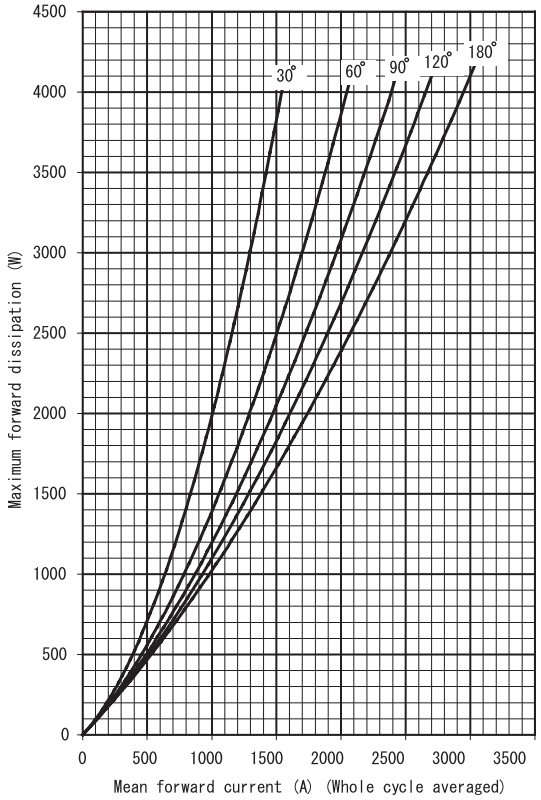


Figure 14 -On-state current vs. Heatsink temperature -Single Side Cooled (Sine wave)

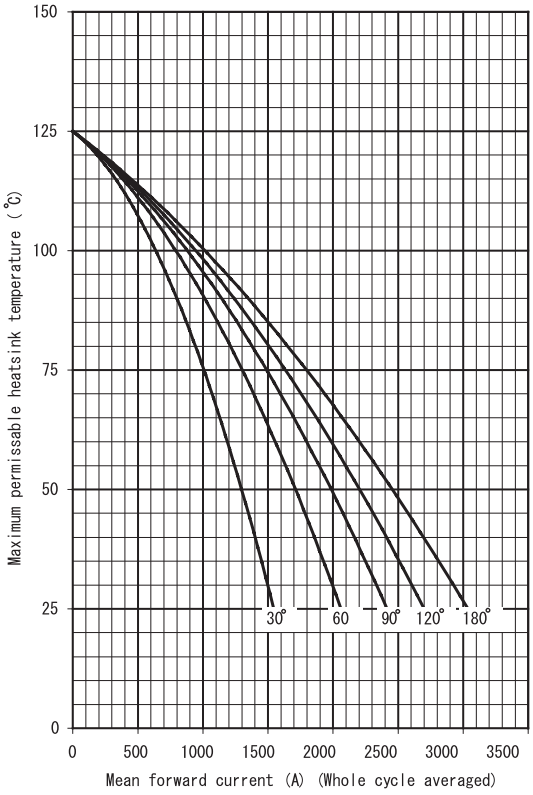


Figure 15 -On-state current vs. Power dissipation -Single Side Cooled (Square wave)

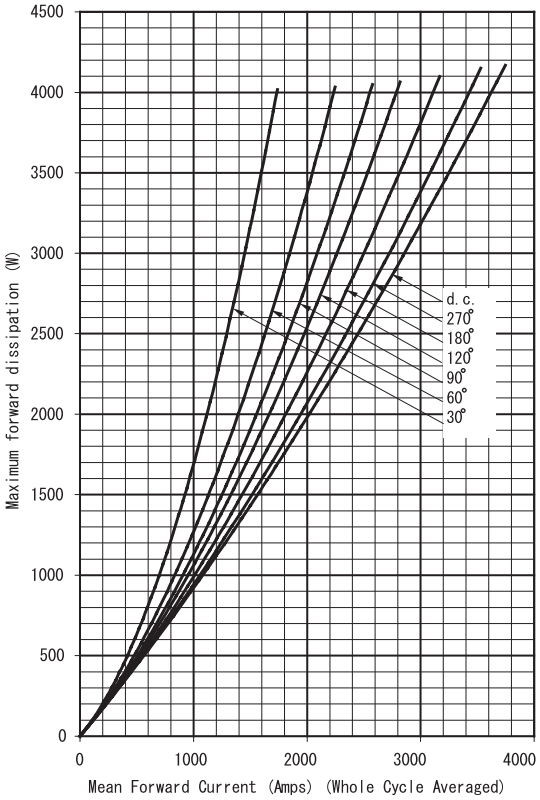


Figure 16 -On-state current vs. Heatsink

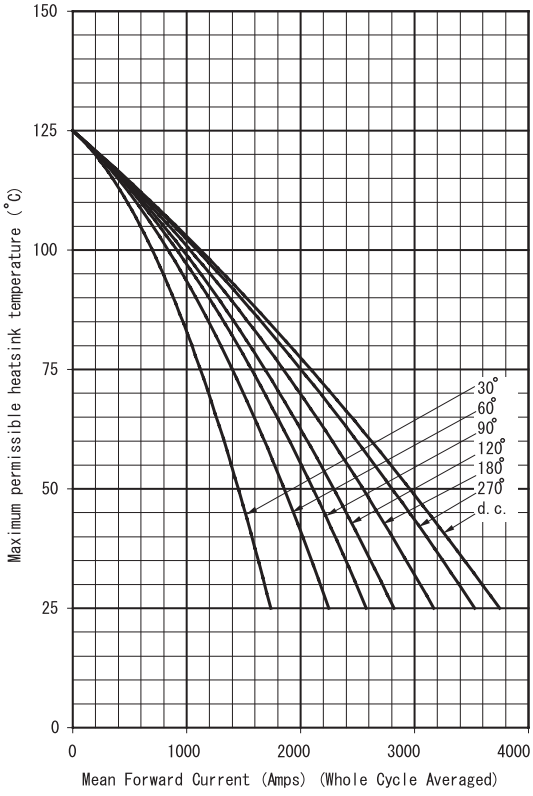


Figure 17 - Maximum surge and I^2t Ratings