

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary

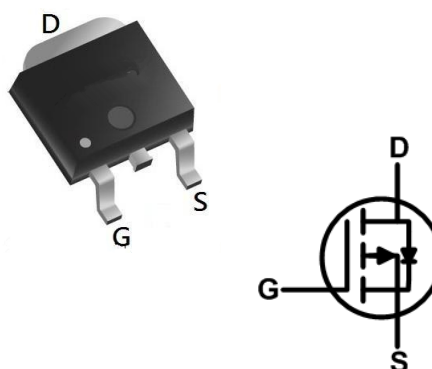
BVDSS	RDSON	ID
-30V	16mΩ	-40A

Description

The 40P03 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The 40P03 meet the RoHS and Green Product requirement , 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V _{DS}	Drain-Source Voltage	-30		V
V _{GS}	Gate-Source Voltage	± 20		V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ -10V ¹	-40		A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ -10V ¹	-25		A
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ -10V ¹	-13.4	-8.5	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ -10V ¹	-10.7	-6.8	A
I _{DM}	Pulsed Drain Current ²	-70		A
EAS	Single Pulse Avalanche Energy ³	72.2		mJ
I _{AS}	Avalanche Current	-38		A
P _D @T _C =25°C	Total Power Dissipation ⁴	34.7		W
P _D @T _A =25°C	Total Power Dissipation ⁴	5	2	W
T _{STG}	Storage Temperature Range	-55 to 150		°C
T _J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
R _{θJA}	Thermal Resistance Junction-Ambient ¹ (t ≤ 10s)	---	25	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	3.6	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1mA$	---	-0.022	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-15A$	---	16	20	$m\Omega$
		$V_{GS}=-4.5V, I_D=-10A$	---	20	25	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	---	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.6	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-10A$	---	5	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	13	---	Ω
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-15A$	---	12.5	---	nC
Q_{gs}	Gate-Source Charge		---	5.4	---	
Q_{gd}	Gate-Drain Charge		---	5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-15A$	---	4.4	---	ns
T_r	Rise Time		---	11.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	34	---	
T_f	Fall Time		---	18	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$	---	1345	---	pF
C_{oss}	Output Capacitance		---	194	---	
C_{rss}	Reverse Transfer Capacitance		---	158	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	-40	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	-75	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F=-15A, dI/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	12.4	---	nS
Q_{rr}	Reverse Recovery Charge		---	5	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-38A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

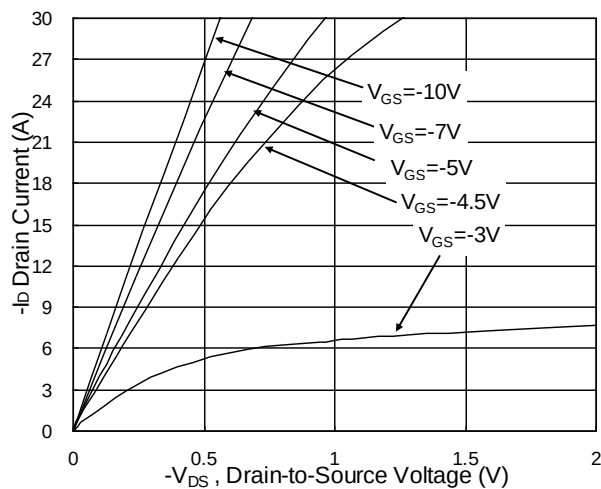


Fig.1 Typical Output Characteristics

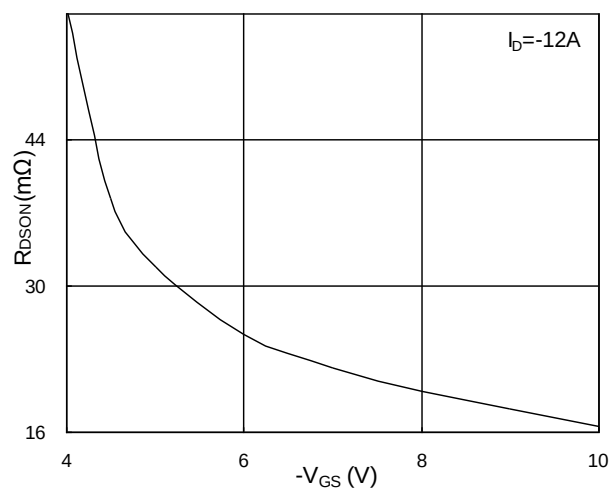


Fig.2 On-Resistance v.s Gate-Source

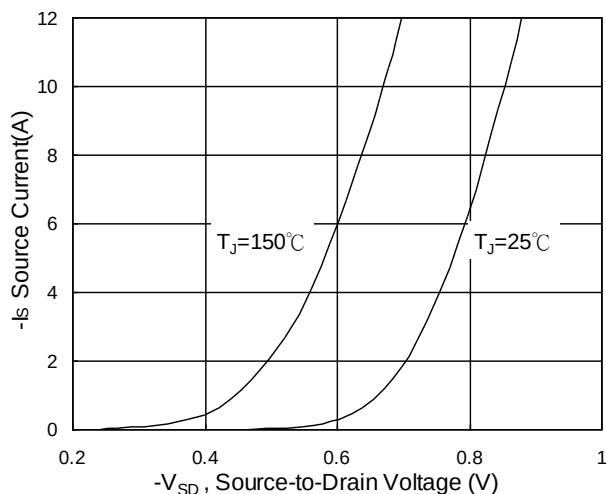


Fig.3 Forward Characteristics of Reverse

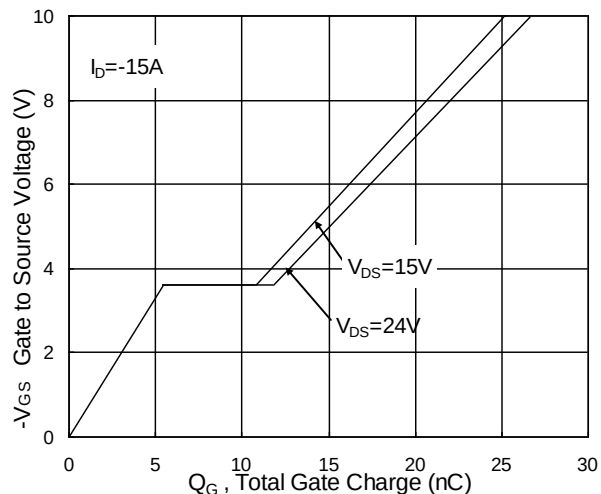


Fig.4 Gate-Charge Characteristics

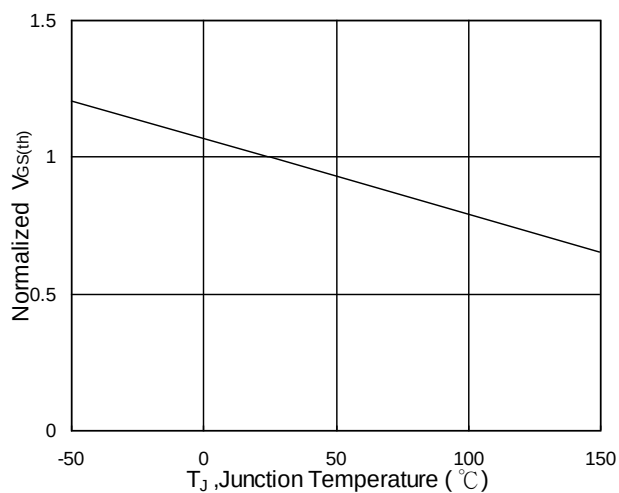


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

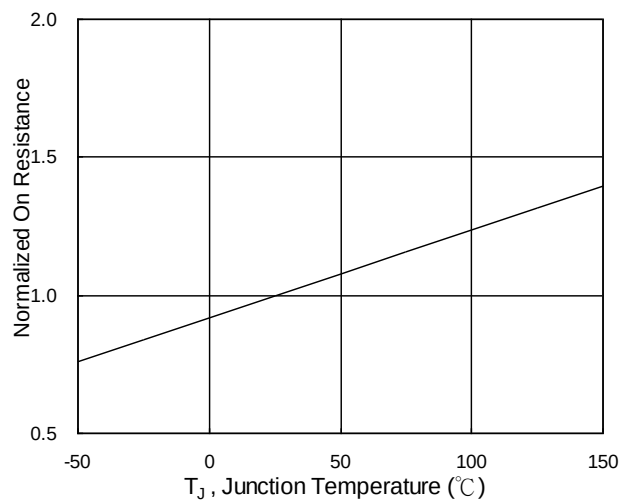


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

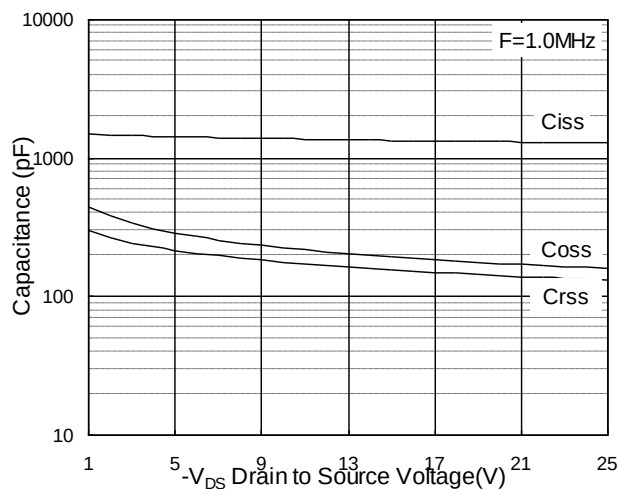


Fig.7 Capacitance

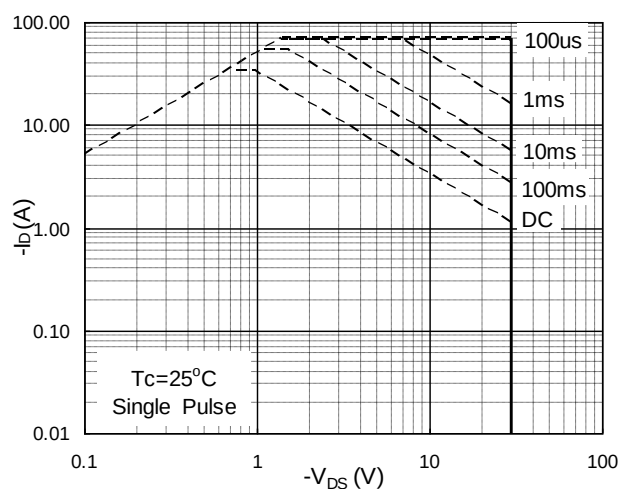


Fig.8 Safe Operating Area

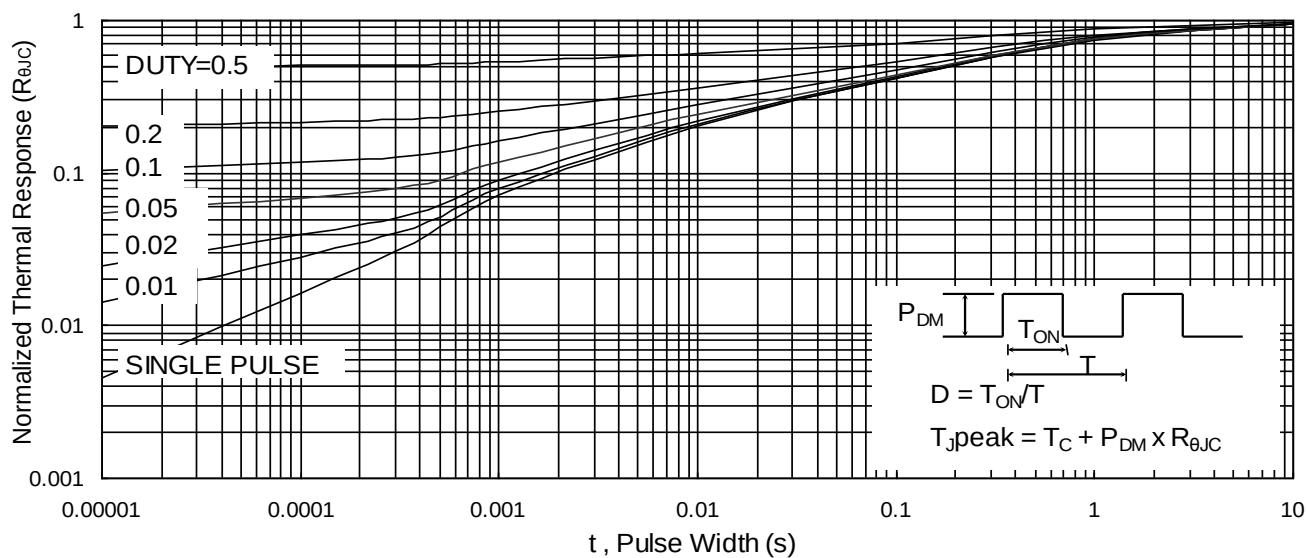


Fig.9 Normalized Maximum Transient Thermal Impedance

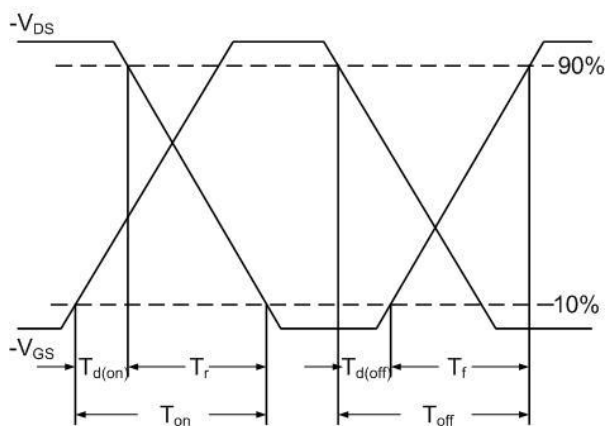


Fig.10 Switching Time Waveform

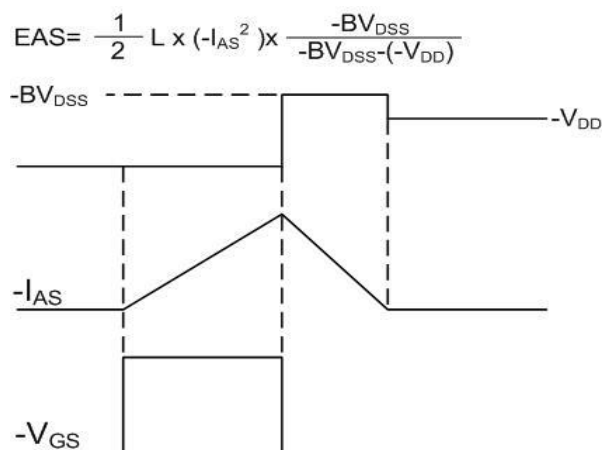


Fig.11 Unclamped Inductive Switching Waveform