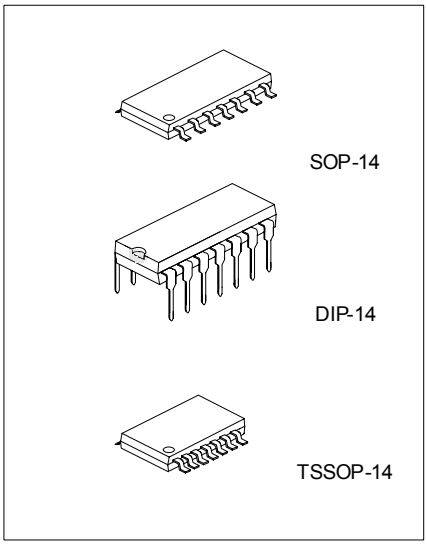
4066

CMOS IC

QUAD BILATERAL SWITCH



*Pb-free plating product number: 4066L

■ DESCRIPTION

The UTC **4066** is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals.

■ FEATURES

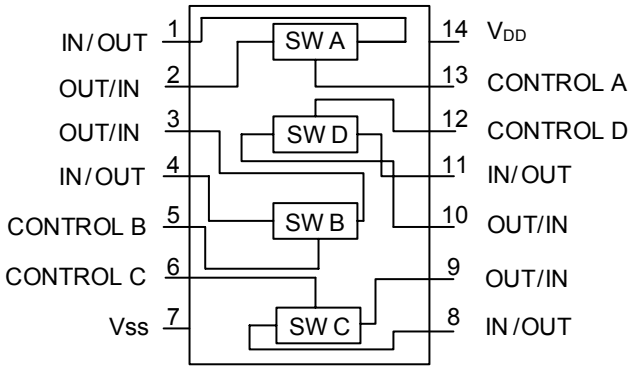
* Wide supply voltage range: 3V ~ 15V.
* High noise immunity : $0.45V_{DD}$ (typ.)
* Wide range of digital and ± $7.5V_{PEAK}$ analog switching
* "ON" resistance for 15V operation : 80Ω
* Matched "ON" resistance : $\triangle R_{ON}$=5Ω (typ.)
  over 15V signal input
* "ON" resistance flat over peak-to-peak signal range
* High "ON" / "OFF" : 65 dB (typ.)
  output voltage ratio @ f_{IS}=10kHz, R_L=10kΩ
* High degree linearity: 0.1% distortion (typ.).
  @ f_{IS}=1kHz, V_{IS}=5Vp-p.
  V_{DD}-V_{SS}=10V, R_L=10kΩ
* Extremely low "OFF" : 0.1nA (typ.)
  switch leakage @V_{DD}-V_{SS}=10V, Ta=25℃
* Extremely high control input impedance : 10^{12}Ω (typ.)
* Low crosstalk : -50dB (typ.)
  between switches @ f_{IS}=0.9MHz, R_L=1kΩ
* Frequency response, switch "ON" : 40MHz (typ.)

■ ORDERING INFORMATION

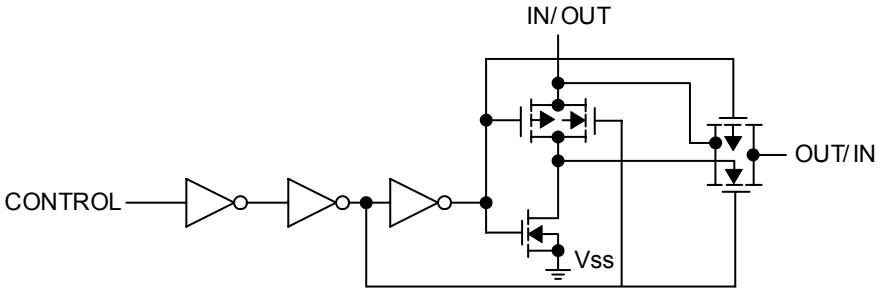
Ordering Number		Package	Packing
Normal	Lead Free Plating		
4066-D14-T	4066L-D14-T	DIP-14	Tube
4066-S14-R	4066L-S14-R	SOP-14	Tape Reel
4066-S14-T	4066L-S14-T	SOP-14	Tube
4066-P14-R	4066L-P14-R	TSSOP-14	Tape Reel
4066-P14-T	4066L-P14-T	TSSOP-14	Tube

4066L-D14-T (1)Packing Type (2)Package Type (3)Lead Plating	(1) R: Tape Reel, T: Tube (2) D14: DIP-14, S14: SOP-14, P14: TSSOP-14 (3) L: Lead Free Plating Blank: Pb/Sn

■ PIN CONFIGURATION



■ SCHEMATIC DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (V_{SS}=0V, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{DD}	-0.5 ~ +18	V
Input Voltage		V_{IN}	-0.5 ~ Vcc+0.5	V
Power Dissipation	DIP-14	P_D	700	mW
	SOP-14		500	mW
	TSSOP-14		500	mW
Junction Temperature		T_J	+125	°C
Storage Temperature		T_{STG}	-40 ~ +150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	3 ~ 15	V
Input Voltage	V_{IN}	0 ~ V_{DD}	V
Operating Temperature Range	T_{OPR}	-40 ~ +85	°C

■ DC ELECTRICAL CHARACTERISTICS (V_{SS}=0V, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	-40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Quiescent Device Current	I_{DD}	V_{DD}=5V		1.0		0.01	1.0		7.5	μA
		V_{DD}=10V		2.0		0.01	2.0		15	μA
		V_{DD}=15V		4.0		0.01	4.0		30	μA
SIGNAL INPUTS AND OUTPUTS										
Input or Output Leakage Switch "OFF"	I_{IS}	Vc=0		±50		±0.1	±50		±200	nA
"ON" Resistance	R_{ON}	R_L=10kΩ ~ (V_{DD}-V_{SS}/2) Vc=V_{DD}, V_{SS} ~ V_{DD} V_{DD}=5V		850		270	1050		1200	Ω
		V_{DD}=10V		330		120	400		520	Ω
		V_{DD}=15V		210		80	240		300	Ω
△"ON" Resistance Between Any 2 of 4 Switches	$\triangle R_{ON}$	R_L=10kΩ ~ (V_{DD}-V_{SS}/2) Vc=V_{DD}, V_{IS}=V_{SS} ~V_{DD} V_{DD}=10V				10				Ω
		V_{DD}=15V				5				Ω
CONTROL INPUTS										
Low Level Input Voltage	V_{ILC}	V_{IS}= V_{SS} and V_{DD} Vos=V_{DD} and V_{SS} I_{IS}= ±10μA V_{DD}=5V		1.5		2.25	1.5		1.5	V
		V_{DD}=10V		3.0		4.5	3.0		3.0	V
		V_{DD}=15V		4.0		6.75	4.0		4.0	V
HIGH Level Input Voltage	V_{IHC}	V_{DD}=5V	3.5		3.5	2.75		3.5		V
		V_{DD}=10V (Note 4)	7.0		7.0	5.5		7.0		V
		V_{DD}=15V	11.0		11.0	8.25		11.0		V
Input Current	I_{IN}	V_{DD}-V_{SS}=15V V_{DD}≧V_{IS}≧V_{SS} V_{DD}≧Vc≧V_{SS}		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

■ AC ELECTRICAL CHARACTERISTICS (AC Parameters are guaranteed by DC correlated testing)

(Ta=25°C, tr=tf=20 ns and Vss=0V unless otherwise)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Time Signal Input to Signal Output	T_{PHL}, T_{PLH}	Vc=V_{DD}, C_L=50pF, (Figure1) R_L=200k	V_{DD}=5V		25	55	ns
			V_{DD}=10V		15	35	ns
			V_{DD}=15V		10	25	ns
Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	t_{PZH}, t_{PLZ}	R_L=1.0kΩ, C_L=50pF (Figure 2, Figure3)	V_{DD}=5V			125	ns
			V_{DD}=10V			60	ns
			V_{DD}=15V			50	ns
Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	t_{PHZ}, t_{PLZ}	R_L=1.0kΩ, C_L=50pF, (Figure 2, Figure3)					
		V_{DD}=5V				125	ns
		V_{DD}=10V				60	ns
		V_{DD}=15V				50	ns
Sine Wave Distortion		Vc=V_{DD}=5V, Vss= -5V R_L=10kΩ, V_{IS}=5V_{P-P}, f=1kHz, (Figure 4)			0.1		%
Frequency Response -Switch “ON” (Frequency at-3dB)		Vc=V_{DD}=5V, Vss= -5V R_L=1kΩ, V_{IS}=5Vp-p 20 Log10 V_{OS}/V_{OS} (1kHz)-dB (Figure 4)			40		MHz
Feedthrough - Switch “OFF” (Frequency at –50 dB)		V_{DD}=5.0V, Vcc=Vss= -5.0V, R_L=1kΩ, V_{IS}=5.0V_{P-P}, 20Log_{10}, V_{OS}/V_{IS}= -50dB, (Figure 4)			1.25		
Crosstalk Between Any Two Switches(Frequency at-50dB)		V_{DD}=V_C(A)=5.0V; Vss=Vc (B)=5.0V, R_L=1kΩ, V_{IS}(A)=5.0V_{P-P}, 20Log_{10}, V_{OS}(B)/V_{IS} (A)= -50dB (Figure 5)			0.9		MHz
Crosstalk; Control Input to Signal Output		V_{DD}=10V, R_L=10kΩ, R_{IN}=1.0kΩ Vcc=10V Square Wave, C_L=50pF (Figure 6)			150		mV_{p-p}
Maximum Control Input		R_L=1.0kΩ, C_L=50pF, (Figure 7) Vos (f) =1/2Vos (1.0kHz)					
		V_{DD}=5.0V			6.0		MHz
		V_{DD}=10V			8.0		MHz
		V_{DD}=15V			8.5		MHz
Signal Input Capacitance	C_{IS}				8.0		pF
Signal Output Capacitance	C_{OS}	V_{DD}=10V			8.0		pF
Feedthrough Capacitance	C_{IOS}	V_C=0V			0.5		pF
Control Input Capacitance	C_{IN}				5.0	7.5	pF

Note 1: These devices should not be connected to circuits with the power ”ON”

Note 2: In all cases, these is approximately 5pF of probe and jig capacitance in the output; however, this capacitance is included in C_L wherever it is specified.

Note 3: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. Vc is the voltage at the control input.

Note 4: Conditions for V_{IHC}: (a) V_{IS}=V_{DD}, Ios=standard B series I_{OH}. (b) V_{IS}=0V, I_{OL}=standard B series I_{OL}

■ SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L=effective external load of the UTC **4066** bilateral switches).This provision avoids any permanent current flow or clamp action of the V_{DD} supply when power is applied or removed from UTC 4066.

In certain applications, the external load-resistor current may include both V_{DD} and Signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1,4,8 or 11,the voltage drop across the bidirectional swith must not exceed 0.6V at Ta ≤ 25℃, or 0.4V at Ta >25℃ (calculated from R_{ON} values shown).

NO V_{DD} current will flow through R_L if the switch current flows into terminals2, 3, 9 or 10.

■ AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS

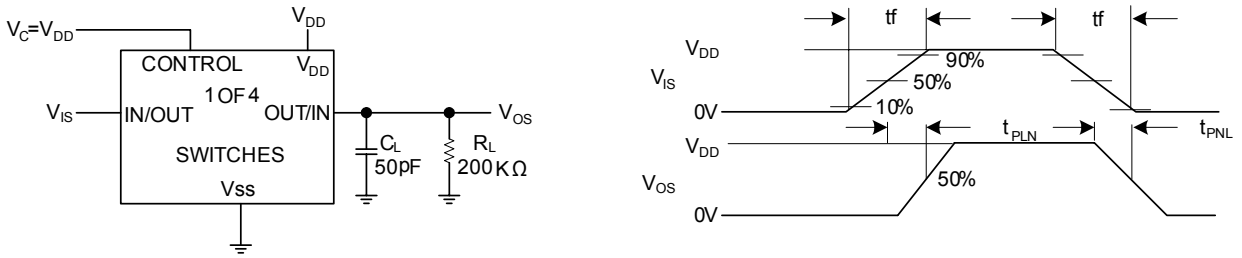


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

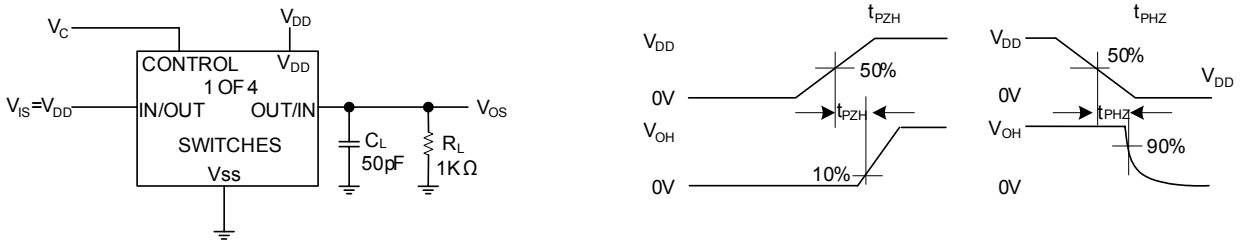


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

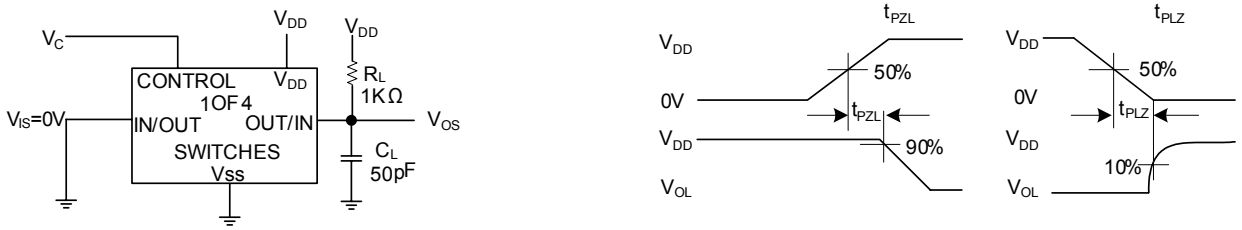
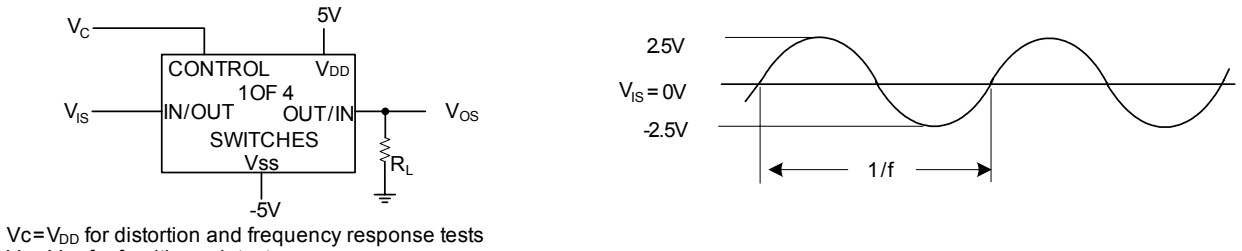


FIGURE 3. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output



Vc=V_{DD} for distortion and frequency response tests
Vc= Vss for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

■ AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS(Cont.)

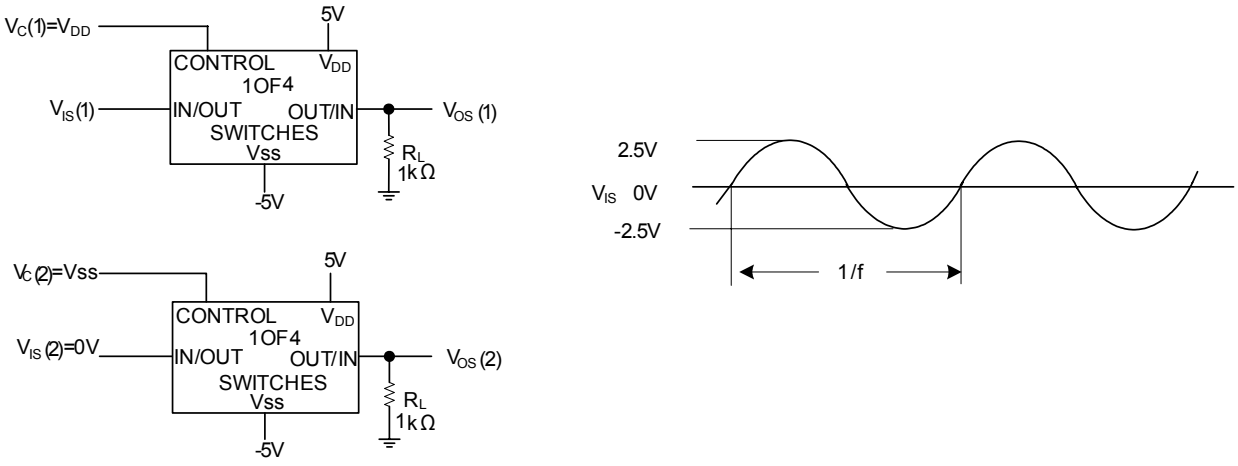


FIGURE 5. Crosstalk Between Any Two Switches

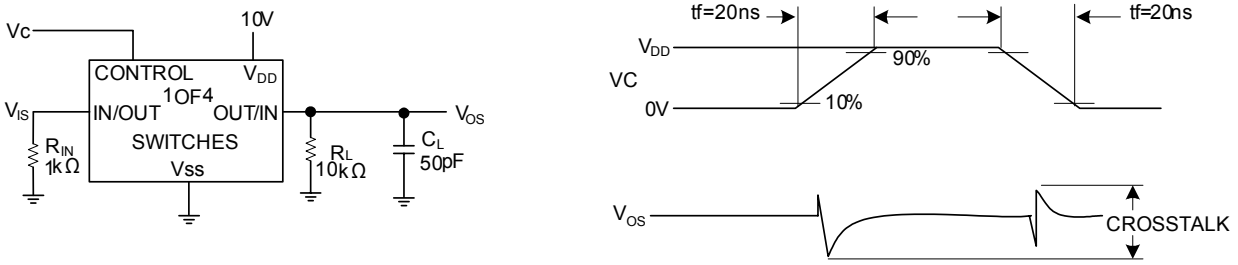


FIGURE 6. Crosstalk: Control Input to Signal Output

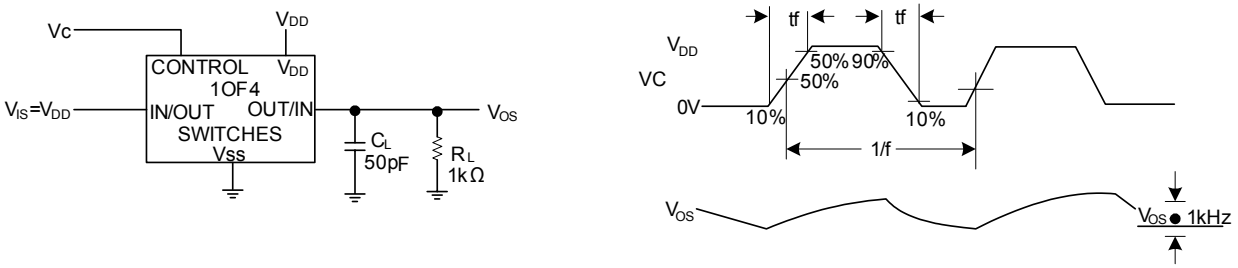
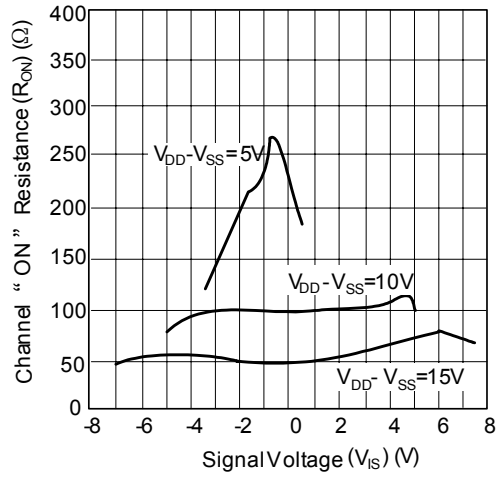


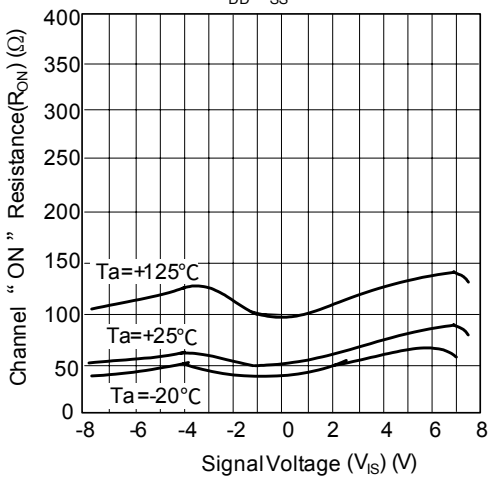
FIGURE 7. Maximum Control Input Frequency

■ TYPICAL PERFORMANCE CHARACTERISTICS

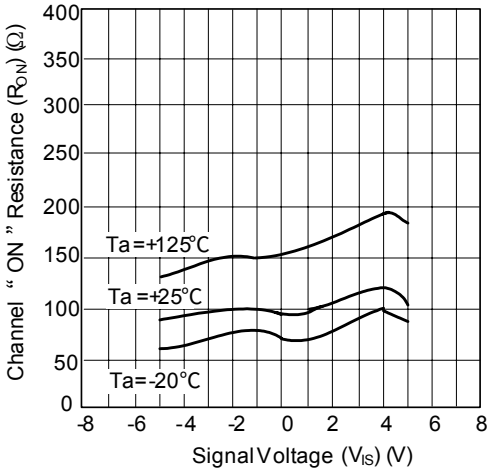
" ON " Resistance vs Signal Voltage for Ta=25°C



" ON " Resistance as a Function of emperature for V_{DD}-V_{SS}=15V



"ON" Resistance as a Function of Temperaturefor V_{DD}-V_{SS}=10V



"ON" Resistance as a Function of Temperature for V_{DD}-V_{SS}=15V