3N163 SERIES

Siliconix incorporated

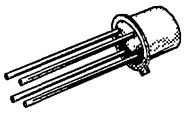
P-Channel Enhancement-Mode MOS Transistors

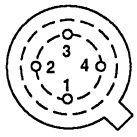
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (mA)	PACKAGE
3N163	–40	250	–50	TO-72
3N164	–30	300	–50	TO-72

Performance Curves: **MRA** (See Section 7)

TO-72 **BOTTOM VIEW**





1 DRAIN
2 GATE
3 SUBSTRATE, CASE
4 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	3N163	3N164	UNITS
Drain-Source Voltage	V_{DS}	–40	–30	V
Gate-Source Voltage	V_{GS}	±40	±30	
Transient Gate-Source Voltage		±125	±125	
Continuous Drain Current	I_D	–50	–50	mA
Power Dissipation	P_D	375	375	mW
Power Derating		3	3	
Operating Junction	T_J	–55 to 150		°C
Storage Temperature	T_{stg}	–65 to 200		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				3N163		3N164		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-40		-30		V
Source-Drain Breakdown Voltage	$V_{(BR)SDS}$	$V_{GD} = V_{BD}$ = 0 V, I_S = -10 µA	-70	-40		-30		V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = -10 µA	-2.5	-2	-5	-2	-5	V
Gate-Source Voltage	V_{GS}	V_{DS} = -15 V, I_D = -0.5 mA	-3.5	-3	-6.5	-2.5	-6.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = -40 V	<-1		-10			pA
		T_A = 125°C	-1		-25			pA
		V_{DS} = 0 V, V_{GS} = -30 V	<-1				-10	pA
		T_A = 125°C	-1				-25	pA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -15 V, V_{GS} = 0 V	-8		-200		-400	pA
		T_A = 125°C	-20					nA
Zero-Gate Voltage Source Current	I_{SDS}	V_{SD} = -20 V, $V_{GD} = V_{DB}$ = 0 V	-10		-400		-800	pA
		T_A = 125°C	-25					nA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -15 V, V_{GS} = -10 V	-10	-5	-30	-3	-30	mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -20 V, I_D = -100 µA	180		250		300	Ω
		T_A = 125°C	270					Ω
DYNAMIC								
Forward Transconductance[3]	g_{fs}	V_{DS} = -15 V, I_D = -10 mA, f = 1 kHz	2.7	2	4	1	4	mS
Common Source Output Conductance[3]	g_{os}	V_{DS} = -15 V, I_D = -10 mA, f = 1 kHz	150		250		250	µS
Input Capacitance	C_{iss}	V_{DS} = -15 V, I_D = -10 mA, f = 1 MHz	2.4		2.5		2.5	pF
Output Capacitance	C_{oss}	V_{DS} = -15 V, I_D = -10 mA, f = 1 MHz	2.5		3		3	pF
Reverse Transfer Capacitance	C_{rss}	V_{DS} = -15 V, I_D = -10 mA, f = 1 MHz	0.5		0.7		0.7	pF
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = -15 V, R_L = 1500 Ω, I_D = -10 mA, V_{GEN} = 12 V, R_G = 50 Ω (Switching time is essentially independent of operating temperature)	5		12		12	ns
	t_r		13		24		24	ns
Turn-Off Time	t_{OFF}		25		50		50	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

6