

# MOS FIELD EFFECT TRANSISTOR **2SK3659**

# SWITCHING N-CHANNEL POWER MOS FET

#### **DESCRIPTION**

The 2SK3659 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3659	Isolated TO-220

#### **FEATURES**

- •4.5V drive available.
- •Low on-state resistance,

 $R_{DS(on)1} = 5.7 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 10 \text{ V, ID} = 40 \text{ A)}$ 

·Low gate charge,

 $Q_G = 32 \text{ nC TYP.}$  (VDD = 16 V, VGS = 10 V, ID = 65 A)

- •Built-in gate protection diode.
- •Avalanche capability ratings.
- •Isolated TO-220 package.

#### ABSOLUTE MAXIMUM RATING (TA = 25°C)

Drain to source voltage (Vgs = 0 V)	VDSS	20	V
Gate to source voltage (V <sub>DS</sub> = 0 V)	Vgss	±20	V
Drain current (DC) (Tc = 25°C)	I <sub>D(DC)</sub>	I <sub>D(DC)</sub> ±65	
Drain current (pulse) Note1	ID(pulse)	±260	Α
Total power dissipation (T <sub>A</sub> = 25°C)	P <sub>T1</sub>	2.0	W
Total power dissipation (Tc = 25°C)	P <sub>T2</sub>	25	W
Channel temperature	Tch	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Single Avalanche Current Note2	IAS	35	Α
Single Avalanche Energy Note2	Eas	122	mJ

**Note 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

2. Starting  $T_{ch}$  = 25°C,  $V_{DD}$  = 10 V,  $R_G$  = 25  $\Omega$ ,  $V_{GS}$  = 20  $\rightarrow$  0 V

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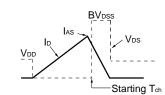


**ELECTRICAL CHARACTERISTICS (TA = 25°C)** 

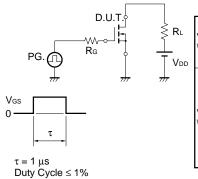
Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			10	μΑ
Gate Leakage Current	Igss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5		2.5	V
Forward Transfer Admittance	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 40 A	15			S
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, ID = 40 A		4.6	5.7	mΩ
	RDS(on)2	Vgs = 4.5 V, ID = 40 A		7.1	9.9	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		1700		pF
Output Capacitance	Coss	Vgs = 0 V		700		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		250		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 40 A		16		ns
Rise Time	tr	Vgs = 10 V		14		ns
Turn-off Delay Time	t <sub>d(off)</sub>	$R_G = 10 \Omega$		50		ns
Fall Time	<b>t</b> f			12		ns
Total Gate Charge	QG	V <sub>DD</sub> = 16 V		32		nC
Gate to Source Charge	Qgs	Vgs = 10 V		6.0		nC
Gate to Drain Charge	Q <sub>GD</sub>	ID = 65 A		8.3		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	IF = 65 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 65 A, VGS = 0 V		45		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		34		nC

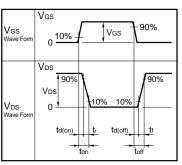
#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $V_{GS} = 20 \rightarrow 0 \text{ V}$

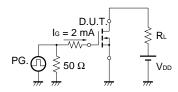


#### **TEST CIRCUIT 2 SWITCHING TIME**



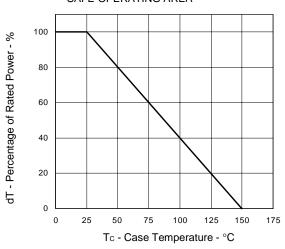


#### **TEST CIRCUIT 3 GATE CHARGE**

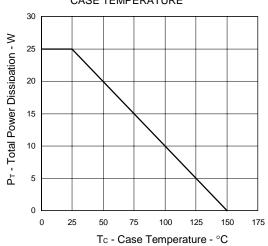


#### TYPICAL CHARACTERISTICS (TA = 25°C)

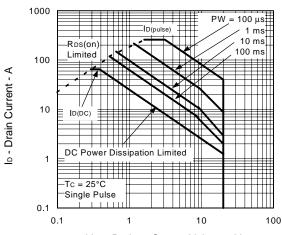
#### DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



#### TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

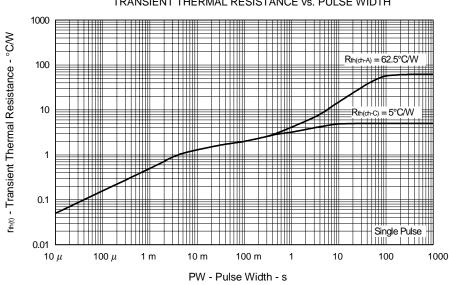


#### FORWARD BIAS SAFE OPERATING AREA

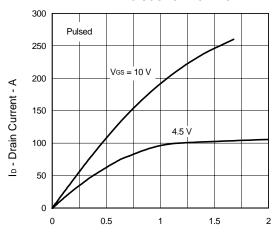


#### V<sub>DS</sub> - Drain to Source Voltage - V

#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

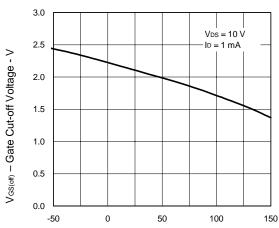


## DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



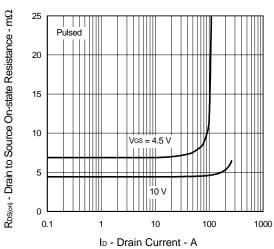
V<sub>DS</sub> - Drain to Source Voltage - V

# GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

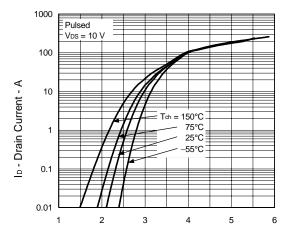


Tch - Channel Temperature - °C

# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

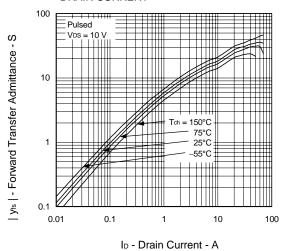


#### FORWARD TRANSFER CHARACTERISTICS

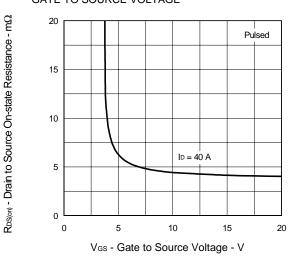


V<sub>GS</sub> - Gate to Source Voltage - V

# FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

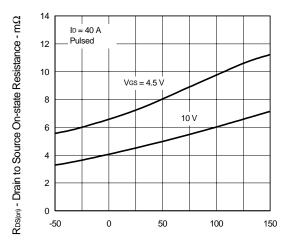


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



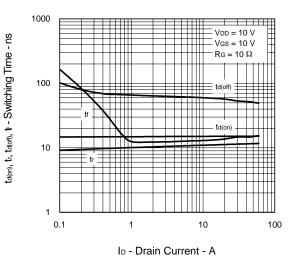
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## DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

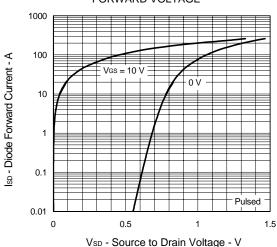


Tch - Channel Temperature - °C

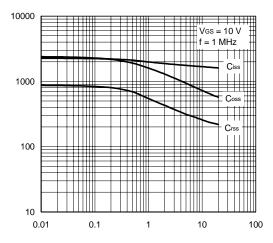
#### SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

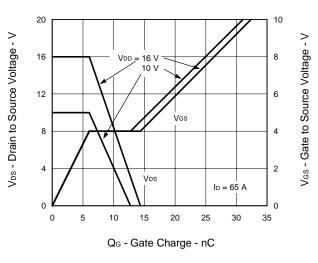


CAPACITANCE vs.
DRAIN TO SOURCE VOLTAGE

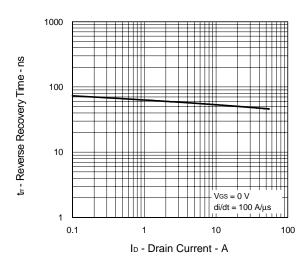


V<sub>DS</sub> - Drain to Source Voltage - V

#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS

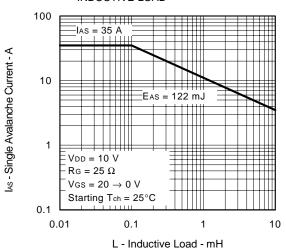


REVERSE RECOVERY TIME vs. DRAIN CURRENT

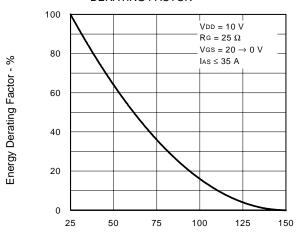


Ciss, Coss, Crss - Capacitance - pF

# SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



# SINGLE AVALANCHE ENERGY DERATING FACTOR

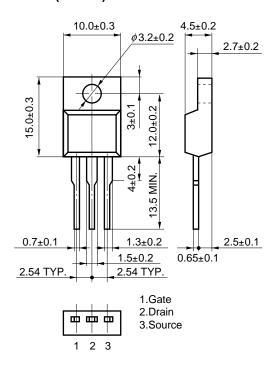


Starting Tch - Starting Channel Temperature - °C

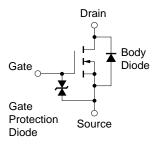


#### **PACKAGE DRAWING (Unit: mm)**

#### Isolated TO-220 (MP-45F)



#### **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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