

MOS FIELD EFFECT TRANSISTOR
2SK3640**SWITCHING**
N-CHANNEL POWER MOS FET**DESCRIPTION**

The 2SK3640 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

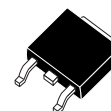
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3640-ZK	TO-252 (MP-3ZK)

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 21 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 9 \text{ A)}$
 $R_{DS(on)2} = 40 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 9 \text{ A)}$
- Low C_{iss} : $C_{iss} = 570 \text{ pF TYP.}$
- Built-in gate protection diode

(TO-252)

**ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)**

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 16	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 19	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 76	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	20	W
Total Power Dissipation	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current ^{Note2}	I_{AS}	10	A
Single Avalanche Energy ^{Note2}	E_{AS}	10	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 15 \text{ V}$, $R_G = 25 \Omega$, $L = 100 \mu\text{H}$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

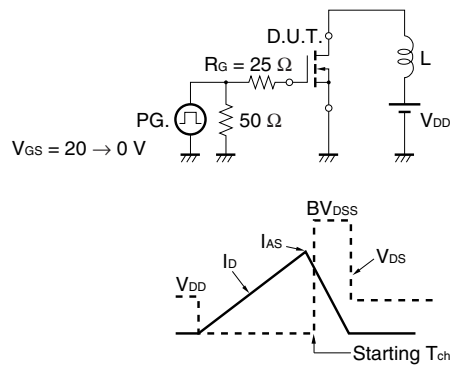
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

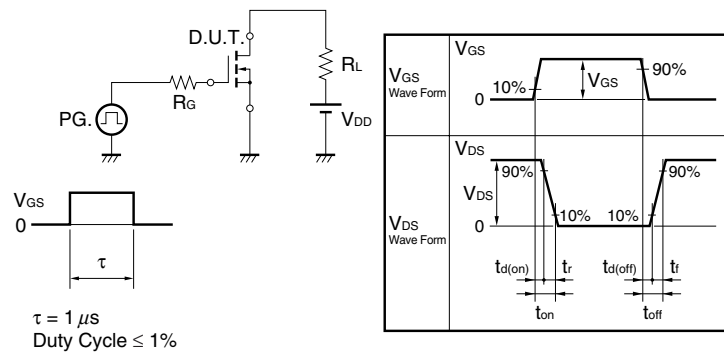
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 9 A	3.7	7.4		S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 9 A		15	21	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 9 A		24	40	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		570		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		160		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		100		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 9 A		7.7		ns
Rise Time	t _r	V _{GS} = 10 V		4.7		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		24		ns
Fall Time	t _f			7		ns
Total Gate Charge	Q _G	V _{DD} = 24 V		14		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		2.4		nC
Gate to Drain Charge	Q _{GD}	I _D = 19 A		4.3		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 19 A, V _{GS} = 0 V		0.95		V
Reverse Recovery Time	t _{rr}	I _F = 19 A, V _{GS} = 0 V		21		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		12		nC

Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

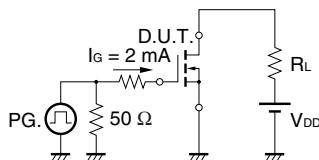
TEST CIRCUIT 1 AVALANCHE CAPABILITY



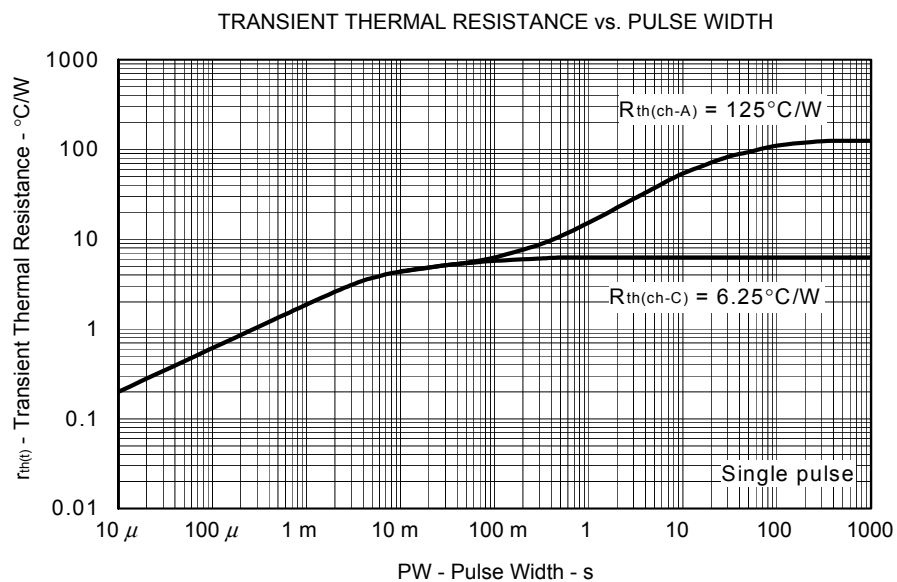
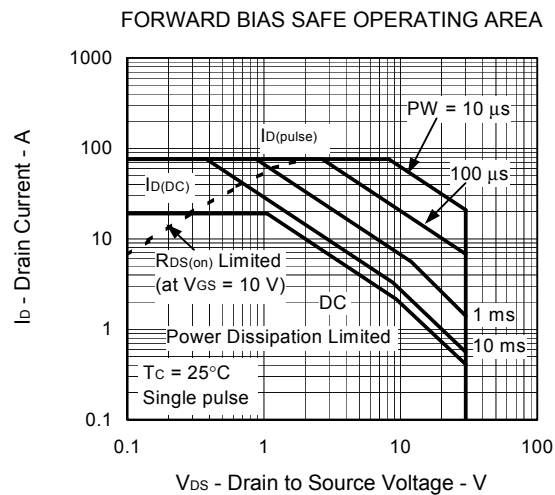
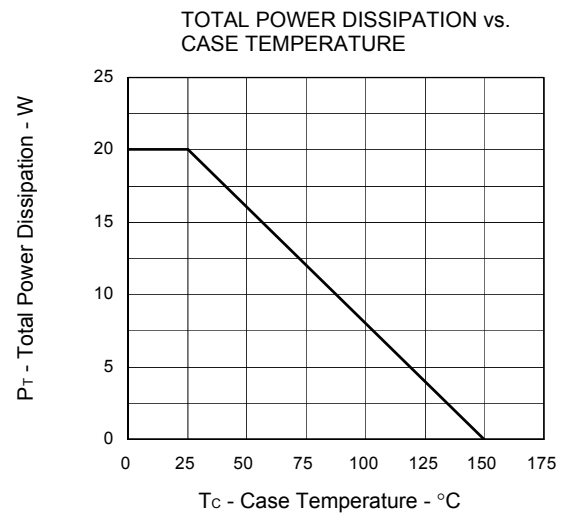
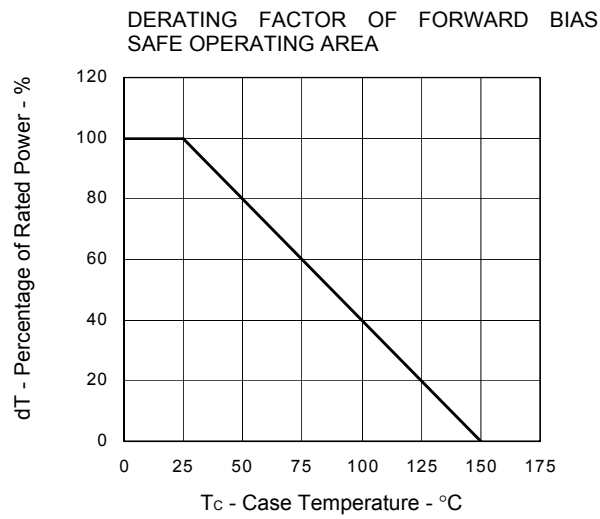
TEST CIRCUIT 2 SWITCHING TIME



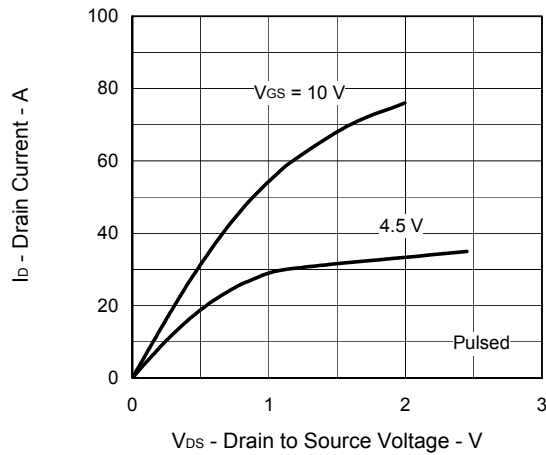
TEST CIRCUIT 3 GATE CHARGE



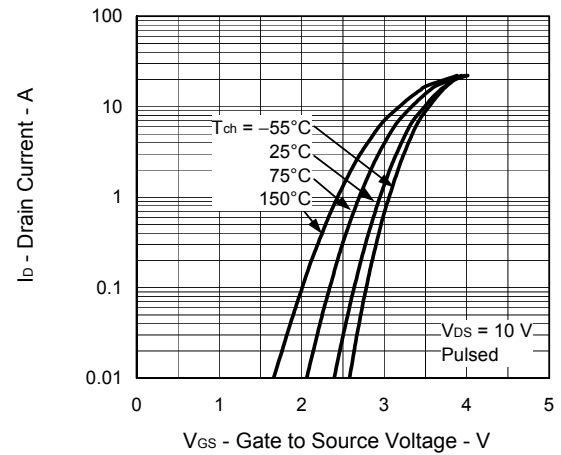
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



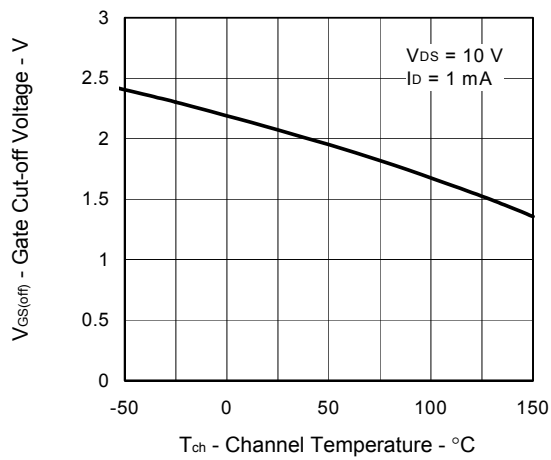
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



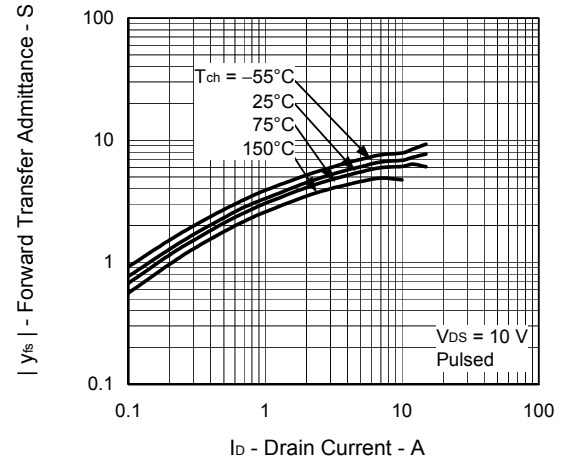
FORWARD TRANSFER CHARACTERISTICS



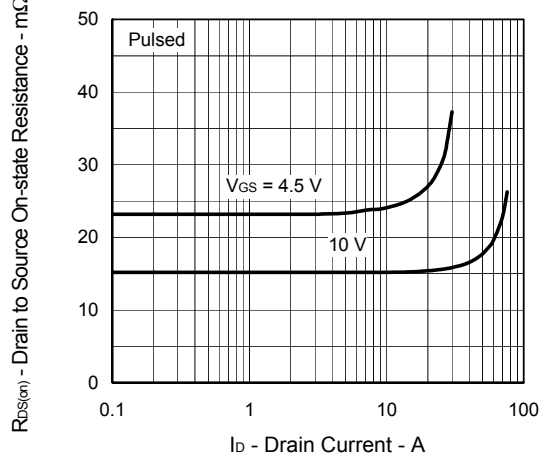
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



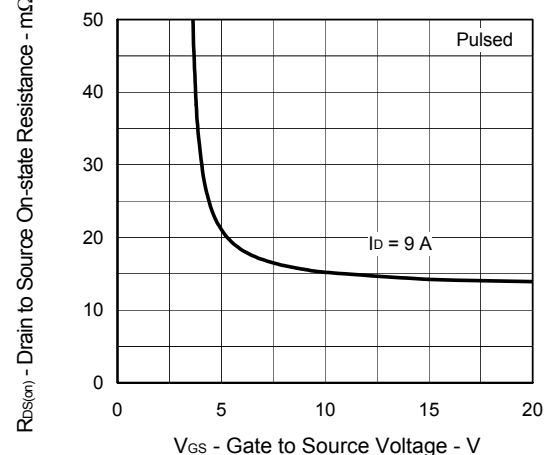
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



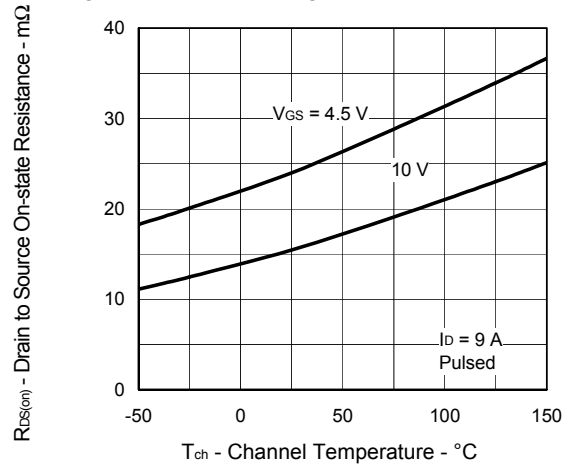
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



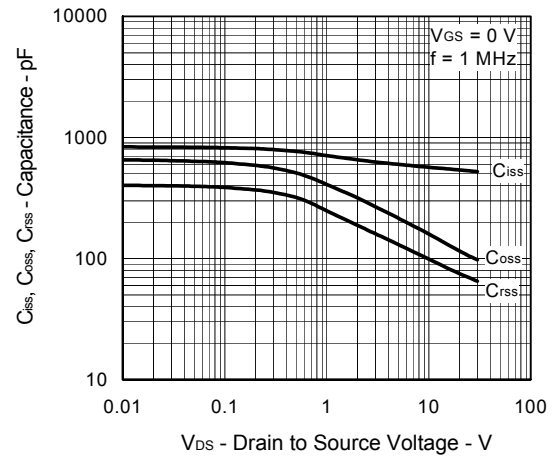
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



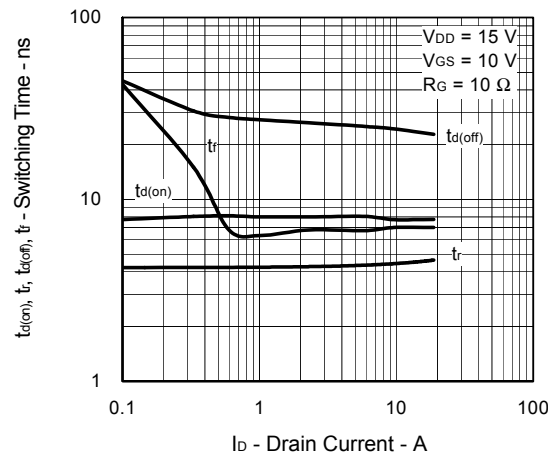
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



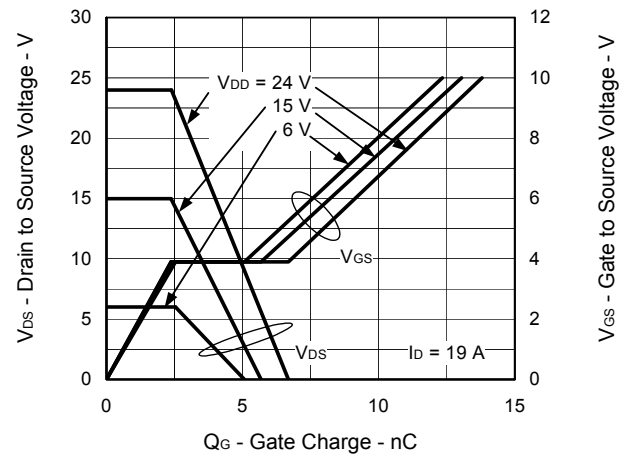
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



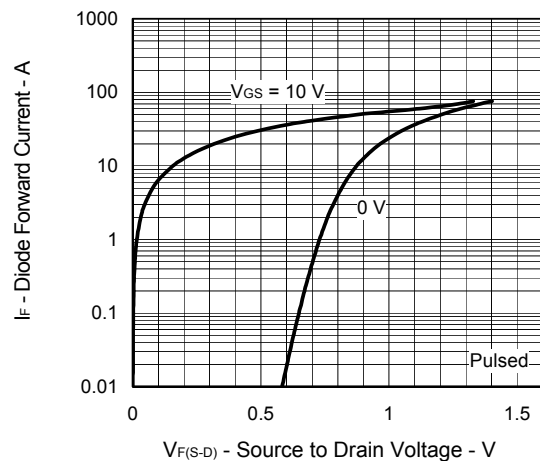
SWITCHING CHARACTERISTICS



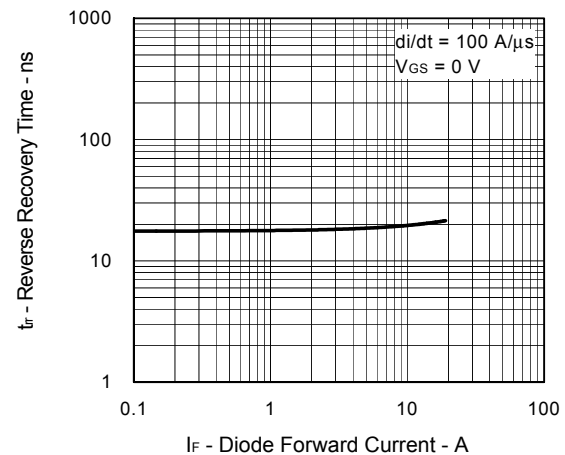
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

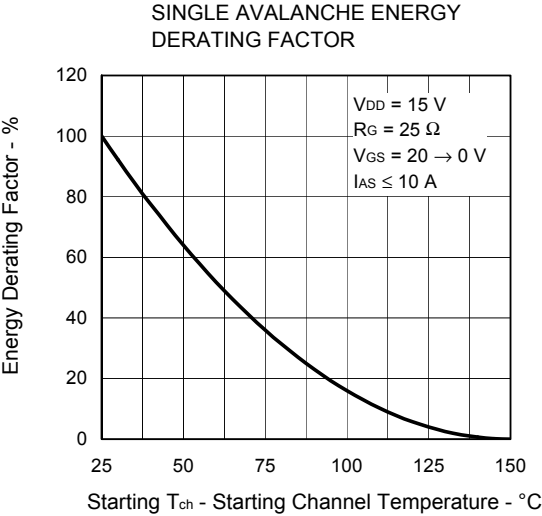
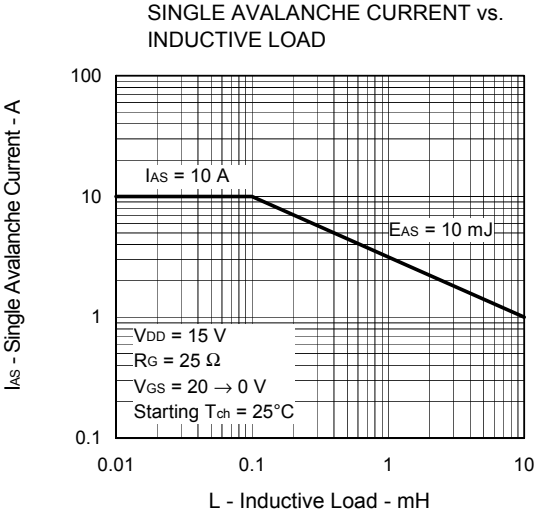


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



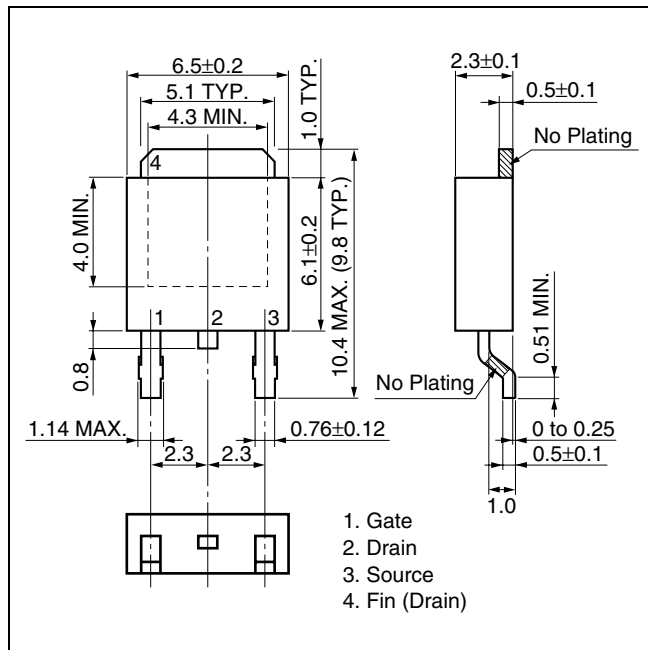
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



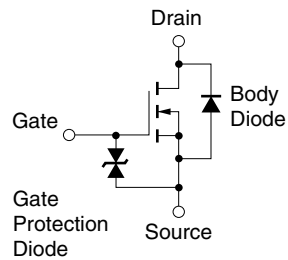


★ PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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