DATA SHEET

NEC

MOS FIELD EFFECT POWER TRANSISTOR
2SK1122

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK1122 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
  $R_{DS(on)} \leqq 50$ mΩ (V_{GS} = 10 V, I_D = 20 A)
  $R_{DS(on)} \leqq 70$ mΩ (V_{GS} = 4 V, I_D = 20 A)
- Low C_{iss} C_{iss} = 3 300 pF TYP.
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

Standard

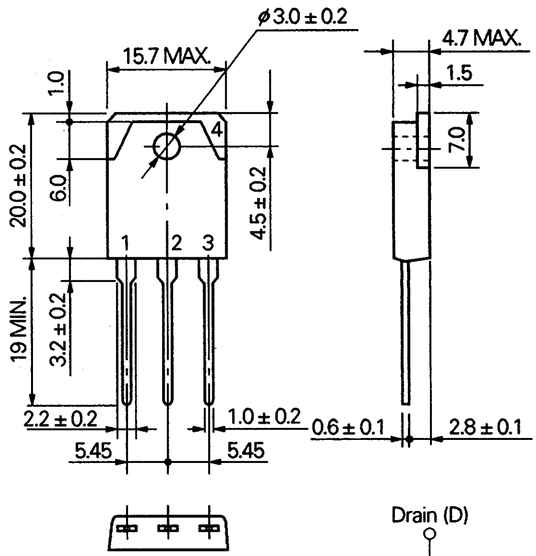
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

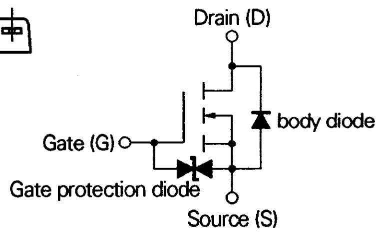
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	$V_{GSS(AC)}$	±20	V
Drain Current (DC)	$I_{D(DC)}$	±40	A
Drain Current (pulse)	$I_{D(pulse)}$*	±160	A
Total Power Dissipation (T_c = 25 °C)	P_{T1}	100	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	3.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

PACKAGE DIMENSIONS
(in millimeters)





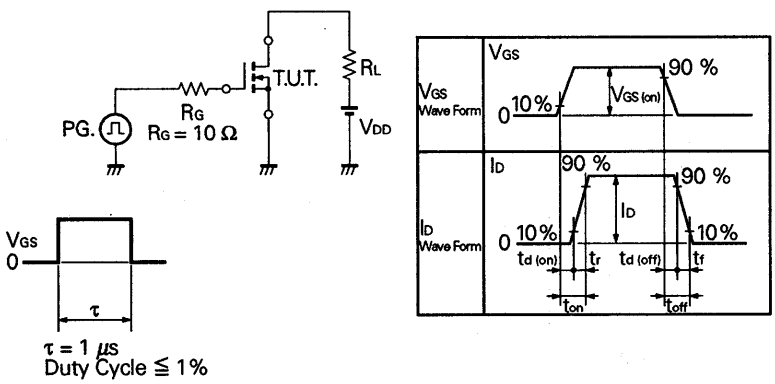
1. Gate
2. Drain
3. Source
4. Fin (Drain)

Document No. TC–2376
Date Published July 1993 M
Printed in Japan

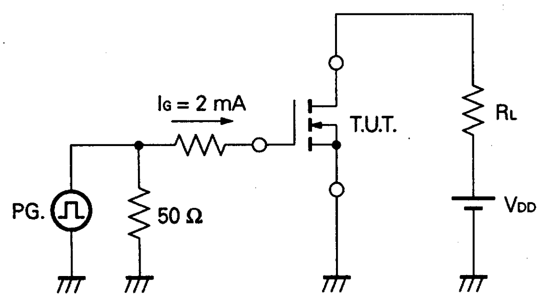
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		42	50	mΩ	V_{GS} = 10 V, I_D = 20 A
Drain to Source On-state Resistance	$R_{DS(on)}$		50	70	mΩ	V_{GS} = 4.0 V, I_D = 20 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	12			S	V_{DS} = 10 V, I_D = 20 A
Drain Leakage Current	I_{DSS}			10	μA	V_{DS} = 100 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±20 V, V_{DS} = 0
Input Capacitance	C_{iss}		3300		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		800		pF	
Reverse Transfer Capacitance	C_{rss}		200		pF	
Turn-On Delay Time	$t_{d(on)}$		40		ns	$V_{GS(on)}$ = 10 V V_{DD} = 50 V I_D = 20 A, R_G = 10 Ω R_L = 2.5 Ω
Rise Time	t_r		210		ns	
Turn-Off Delay Time	$t_{d(off)}$		210		ns	
Fall Time	t_f		155		ns	
Total Gate Charge	Q_G		80		nC	V_{GS} = 10 V I_D = 40 A V_{DD} = 80 V
Gate to Source Charge	Q_{GS}		10		nC	
Gate to Drain Charge	Q_{GD}		30		nC	
Diode Forward Voltage	V_{SD}		1.2		V	I_{SD} = 40 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		210		ns	I_F = 40 A, V_{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		600		nC	

Test Circuit 1: Switching Time

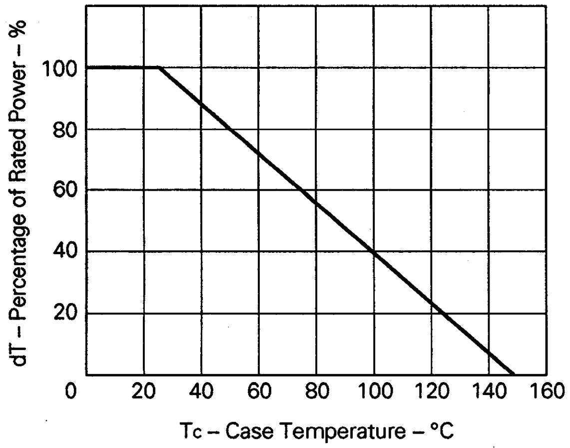


Test Circuit 2: Gate Charge

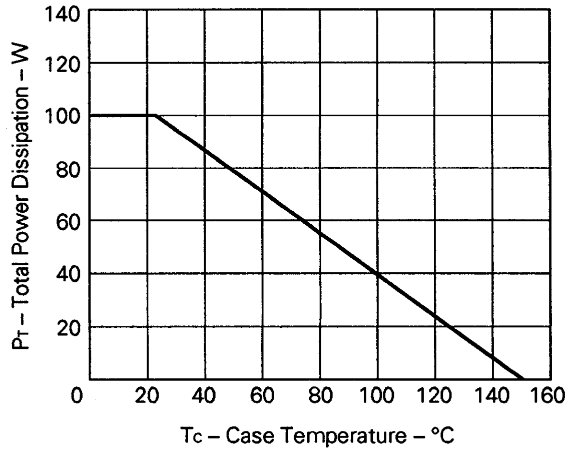


TYPICAL CHARACTERISTICS (T_a = 25 °C)

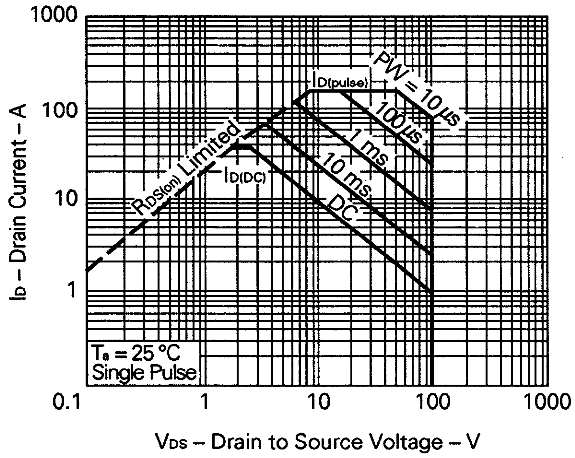
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



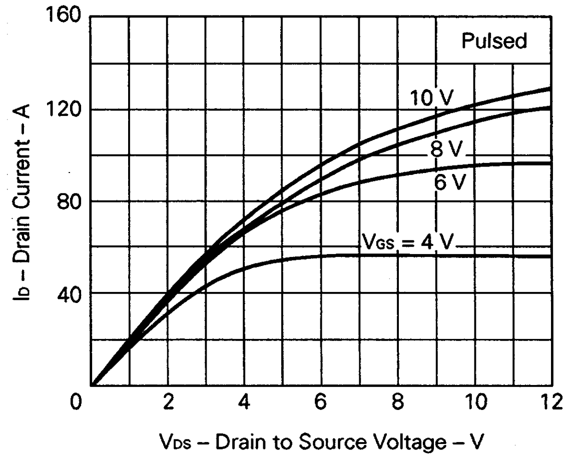
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



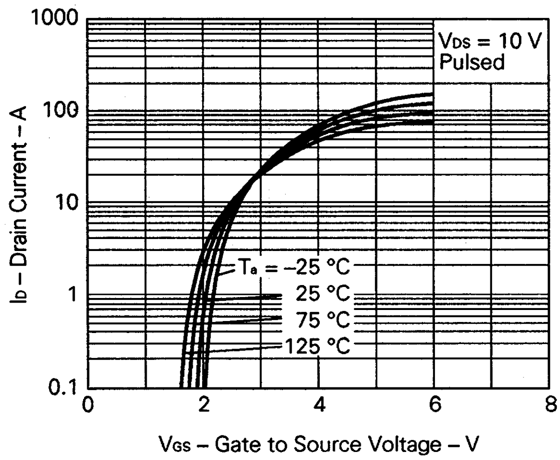
FORWARD BIAS SAFE OPERATING AREA



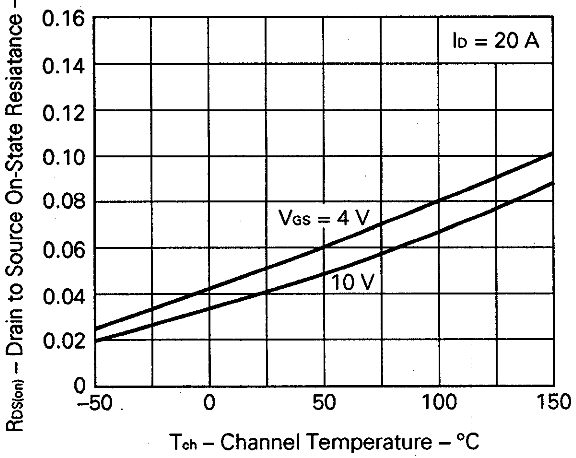
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



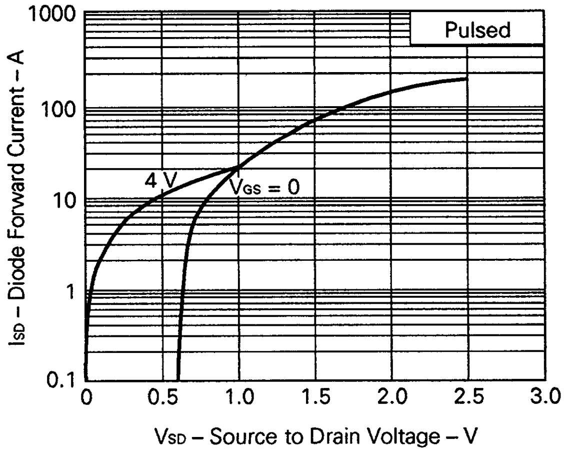
TRANSFER CHARACTERISTICS



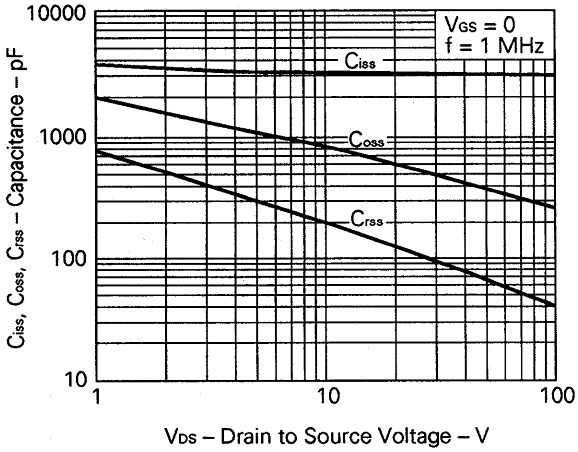
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



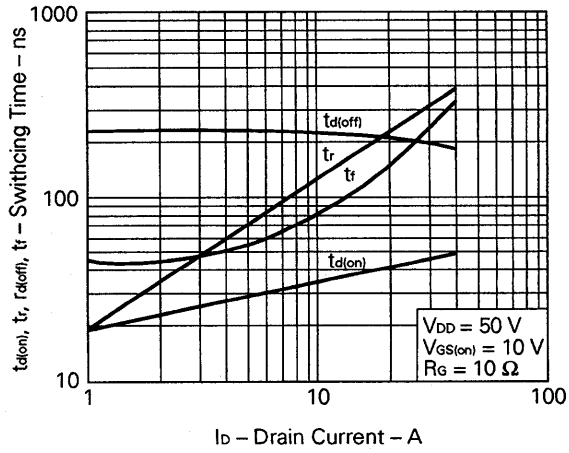
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



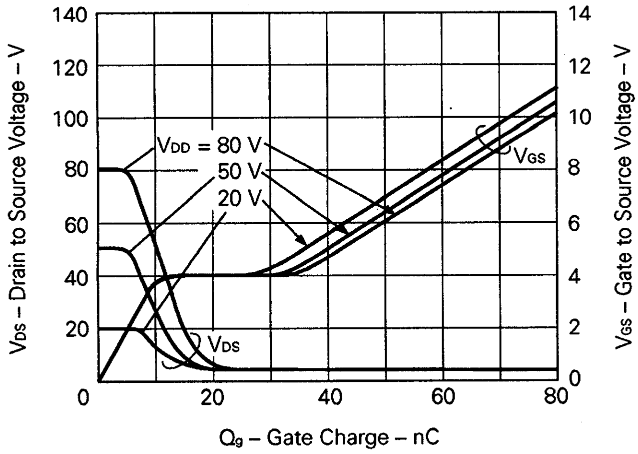
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



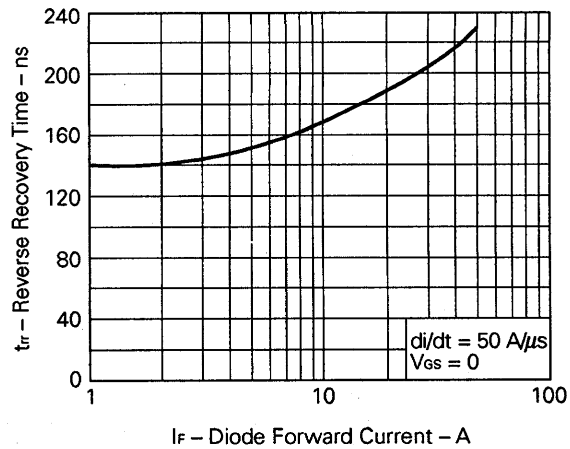
SWITCHING CHARACTERISTICS

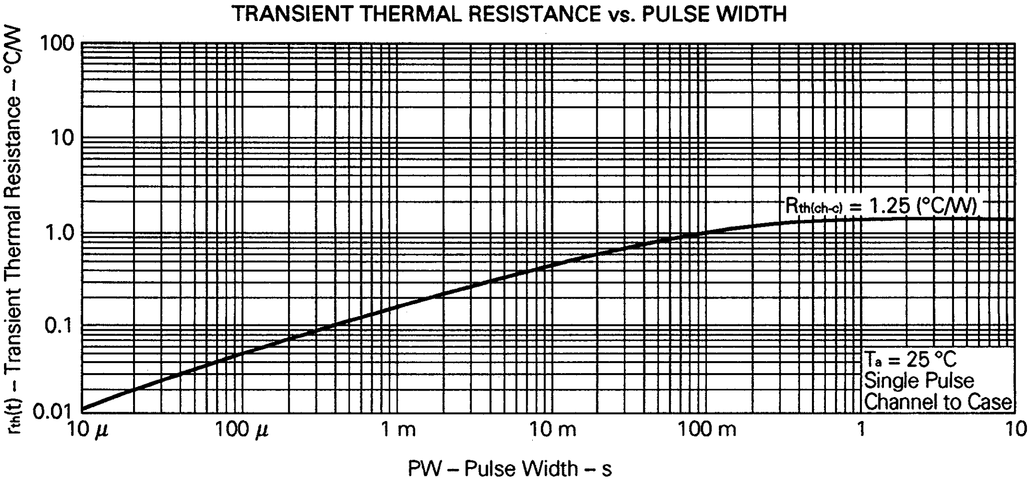


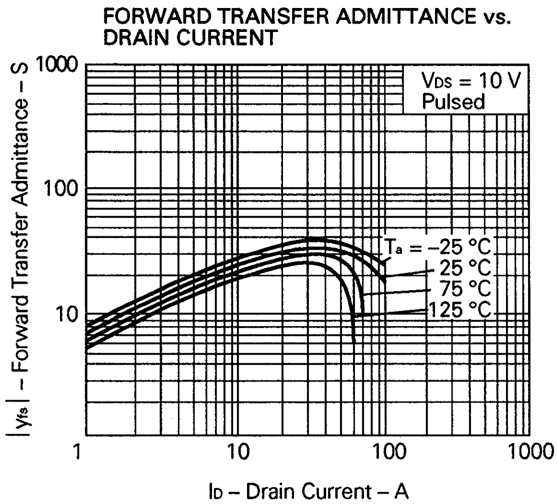
DYNAMIC INPUT CHARACTERISTICS

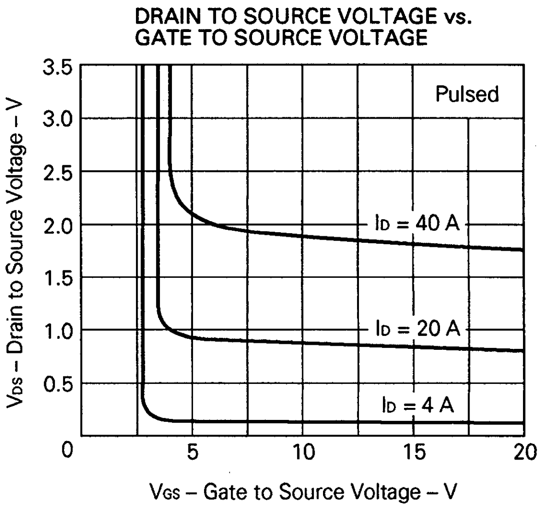


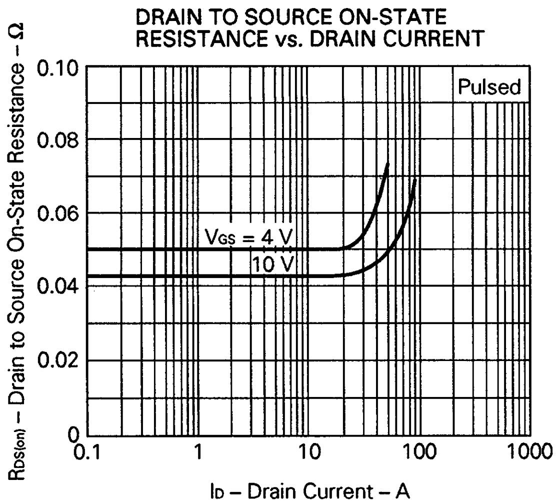
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

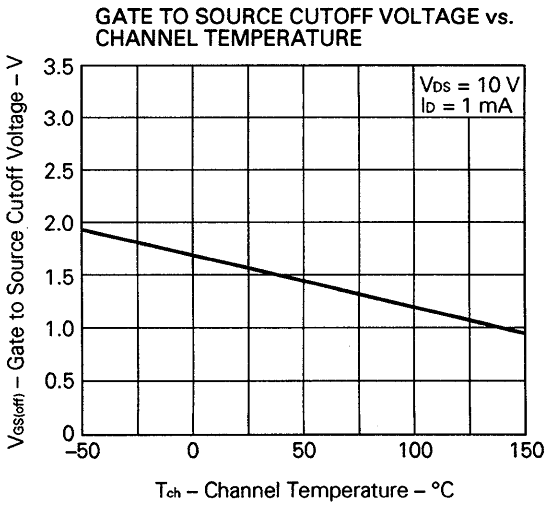



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH
rth(t) – Transient Thermal Resistance – °C/W
100
10
1.0
0.1
0.01
Rth(ch-c) = 1.25 (°C/W)
Ta = 25 °C
Single Pulse
Channel to Case
10 μ
100 μ
1 m
10 m
100 m
1
10
PW – Pulse Width – s


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT
|yfs| – Forward Transfer Admittance – S
1000
100
10
VDS = 10 V
Pulsed
Ta = –25 °C
25 °C
75 °C
125 °C
1
10
100
1000
ID – Drain Current – A


DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE
VDS – Drain to Source Voltage – V
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
Pulsed
ID = 40 A
ID = 20 A
ID = 4 A
5
10
15
20
VGS – Gate to Source Voltage – V


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT
RDS(on) – Drain to Source On-State Resistance – Ω
0.10
0.08
0.06
0.04
0.02
0
Pulsed
VGS = 4 V
10 V
0.1
1
10
100
1000
ID – Drain Current – A


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE
VGS(off) – Gate to Source Cutoff Voltage – V
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
VDS = 10 V
ID = 1 mA
–50
0
50
100
150
Tch – Channel Temperature – °C

REFERENCE

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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