

Silicon NPN Power Transistors

2SD388

DESCRIPTION

www.datasheet4u.com

- With TO-3 package
- High power dissipation

APPLICATIONS

- For use in power amplifier applications

PINNING

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector



Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings($T_a = \square$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	150	V
V_{CEO}	Collector-emitter voltage	Open base	140	V
V_{EBO}	Emitter-base voltage	Open collector	7	V
I_C	Collector current		8	A
P_C	Collector power dissipation	$T_C = 25 \square$	80	W
T_j	Junction temperature		150	$\square$
T_{stg}	Storage temperature		-55~150	$\square$

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CHARACTERISTICS

Tj=25°C unless otherwise specified

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CEO(SUS)}$	Collector-emitter sustaining voltage	$I_C=0.2A ; I_B=0$	140			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	$I_E=10mA ; I_C=0$	7			V
V_{CEsat}	Collector-emitter saturation voltage	$I_C=6A ; I_B=0.6A$			2.0	V
V_{BEsat}	Base-emitter saturation voltage	$I_C=6A ; I_B=0.6A$			2.5	V
I_{CBO}	Collector cut-off current	$V_{CB}=150V ; I_E=0$			0.1	mA
I_{EBO}	Emitter cut-off current	$V_{EB}=7V ; I_C=0$			0.1	mA
h_{FE-1}	DC current gain	$I_C=1A ; V_{CE}=5V$	50			
h_{FE-2}	DC current gain	$I_C=5A ; V_{CE}=5V$	20			
f_T	Transition frequency	$I_C=1A ; V_{CE}=10V$		9		MHz

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PACKAGE OUTLINE

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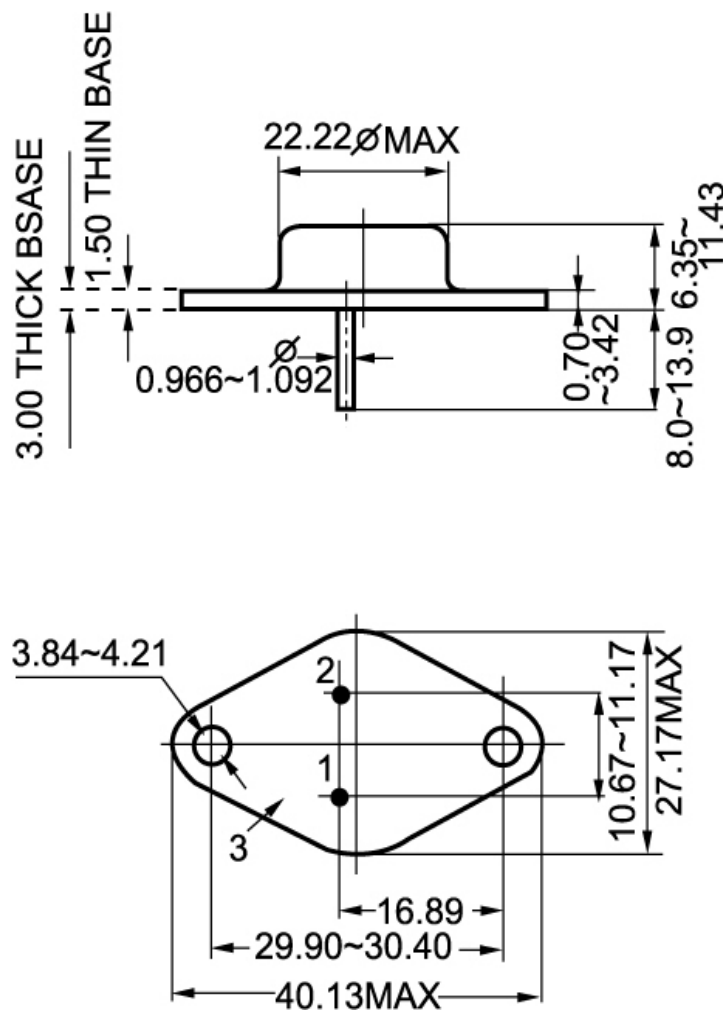


Fig.2 outline dimensions (unindicated tolerance:±0.1mm)