



SANYO Semiconductors

DATA SHEET

2SC6146

NPN Triple Diffused Planar Silicon Transistor

Switching Regulator Applications

Features

- High breakdown voltage.
- Ultrahigh-speed switching.
- Wide ASO.
- Adoption of MBIT process.

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	VCBO		800	V
Collector-to-Emitter Voltage	VCE		800	V
Collector-to-Emitter Voltage	VCEO		350	V
Emitter-to-Base Voltage	VEBO		8	V
Collector Current	IC		1	A
Collector Current (Pulse)	ICP	PW≤300μs, duty cycle≤10%	2	A
Base Current	IB		0.5	A
Collector Dissipation	PC		1	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		-55 to +150	°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	ICBO	VCB=400V, IE=0A			10	μA
Emitter Cutoff Current	IEBO	VEB=5V, IC=0A			10	μA
DC Current Gain	hFE1	VCE=5V, IC=0.1A	100		200	
	hFE2	VCE=5V, IC=0.5A	10			
	hFE3	VCE=5V, IC=1mA	20			

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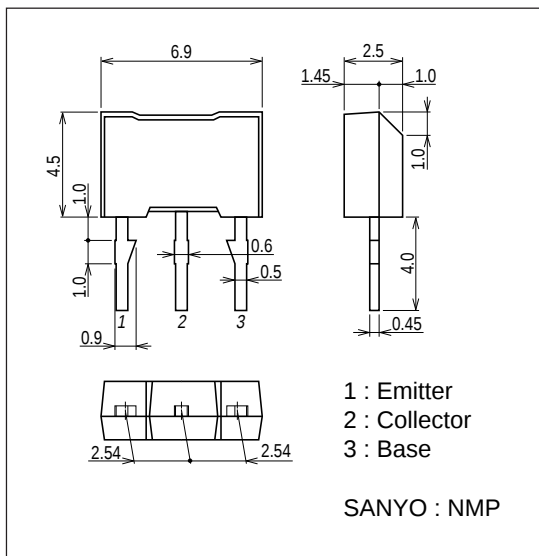
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Gain-Bandwidth Product	f_T	$V_{CE}=10V, I_C=0.1A$		20		MHz
Output Capacitance	C_{ob}	$V_{CB}=10V, f=1MHz$		10		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=0.5A, I_B=0.1A$			0.8	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C=0.5A, I_B=0.1A$			1.5	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=1mA, I_E=0A$	800			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CES}$	$I_C=100\mu A, R_{BE}=0\Omega$	800			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=5mA, R_{BE}=\infty$	350			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E=1mA, I_C=0A$	8			V
Turn-ON Time	t_{on}	$I_C=0.5A, I_{B1}=0.05A, I_{B2}=-0.5A, R_L=400\Omega, V_{CC}=200V$			1.0	μs
Storage Time	t_{stg}	$I_C=0.5A, I_{B1}=0.05A, I_{B2}=-0.5A, R_L=400\Omega, V_{CC}=200V$			1.0	μs
Fall Time	t_f	$I_C=0.5A, I_{B1}=0.05A, I_{B2}=-0.5A, R_L=400\Omega, V_{CC}=200V$			0.3	μs

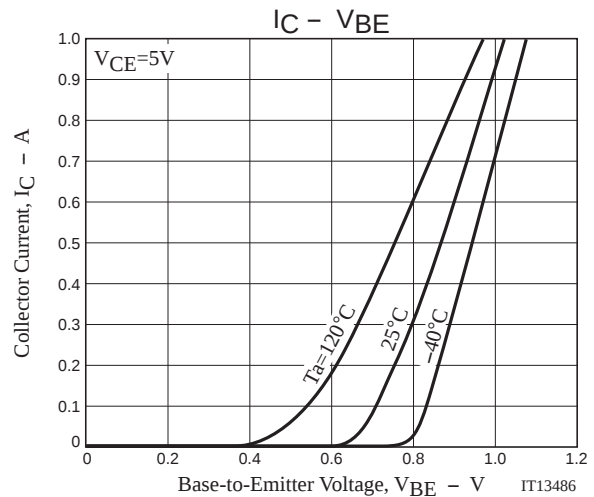
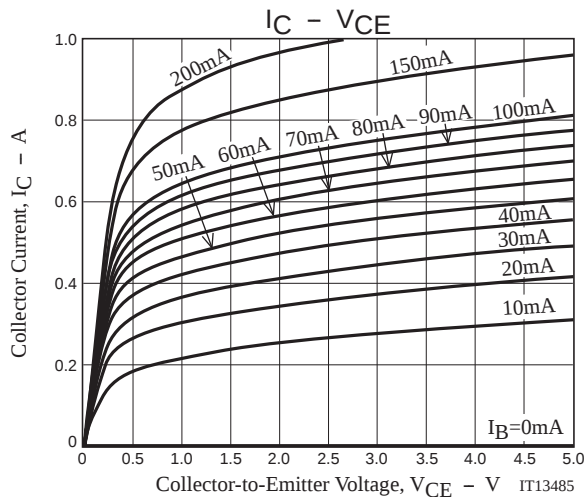
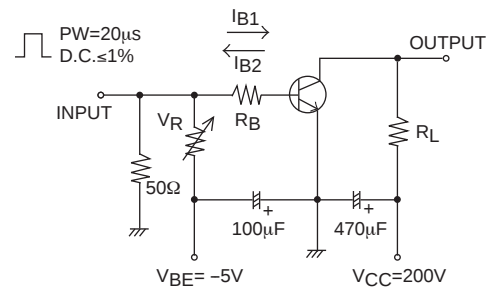
Package Dimensions

unit : mm (typ)

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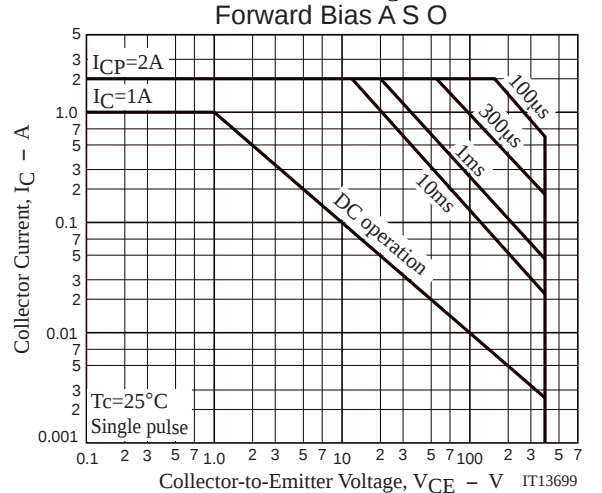
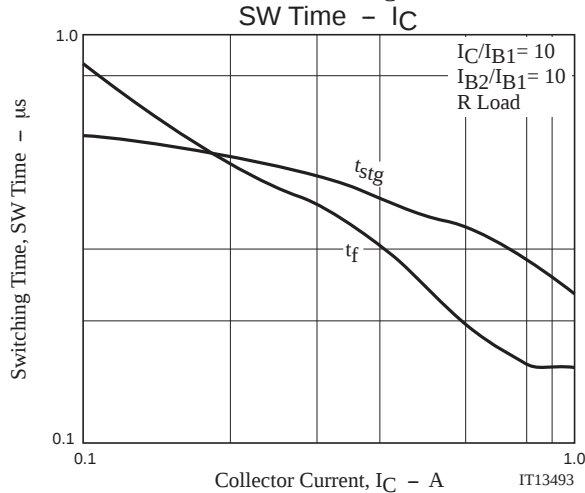
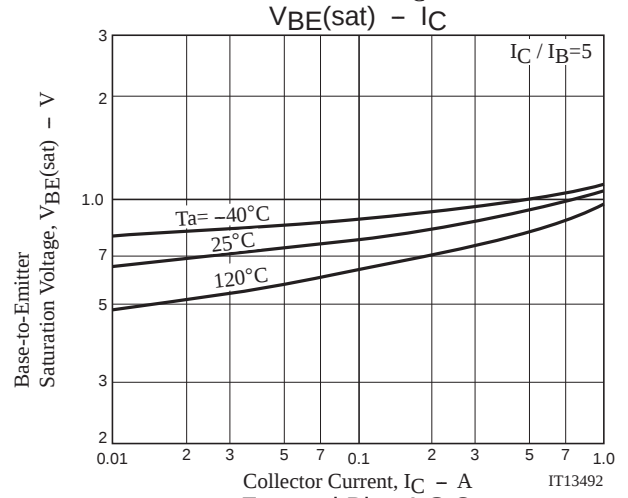
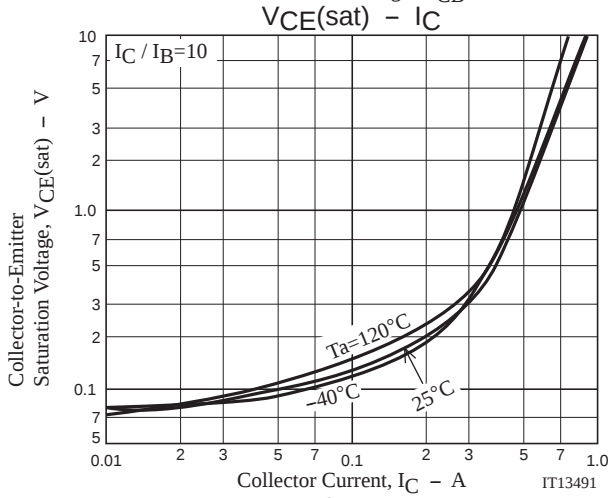
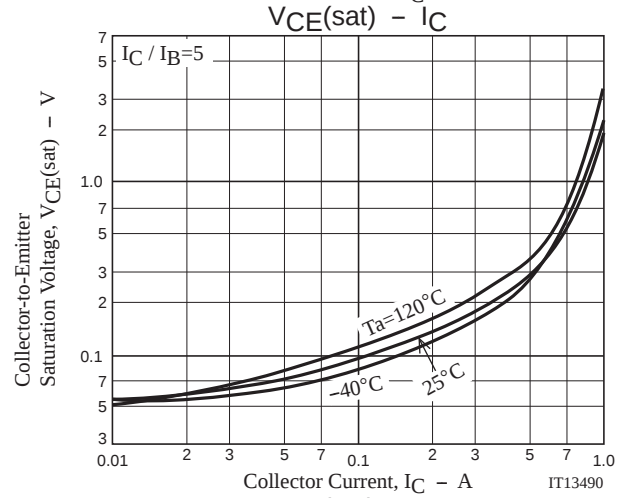
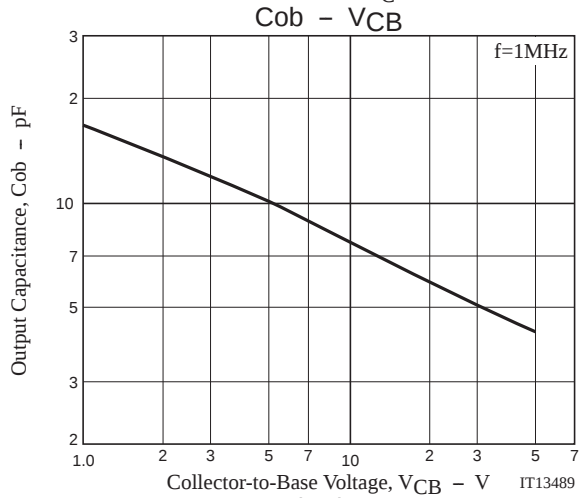
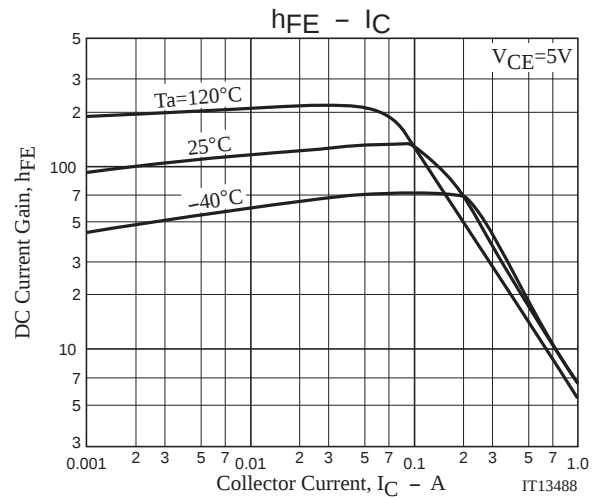
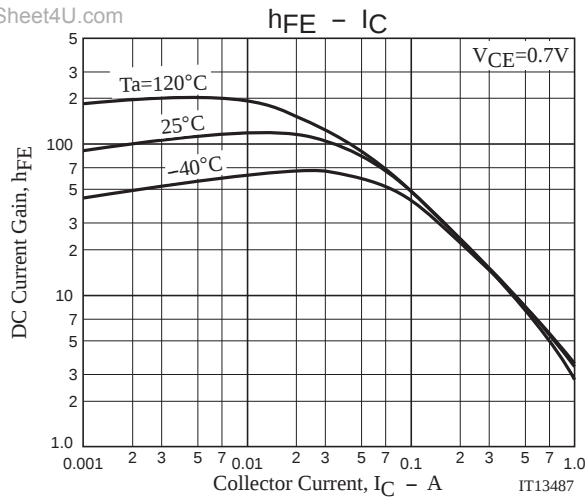


Switching Time Test Circuit

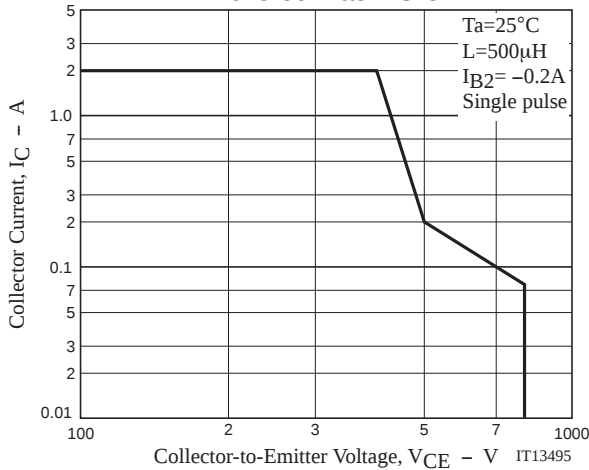
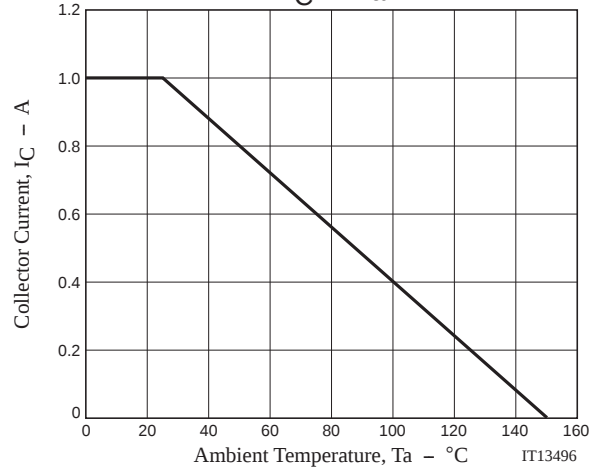


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Reverse Bias A S O

 $P_C - T_a$ 

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