MITSUBISHI RF POWER TRANSISTOR

2SC4526

NPN EPITAXIAL PLANAR TYPE

DISCRIPTION

2SC4526 is a silicon NPN epitaxial planar type transistor specifically designed for RF power amplifier applications in 1.65GHz.

FEATURES

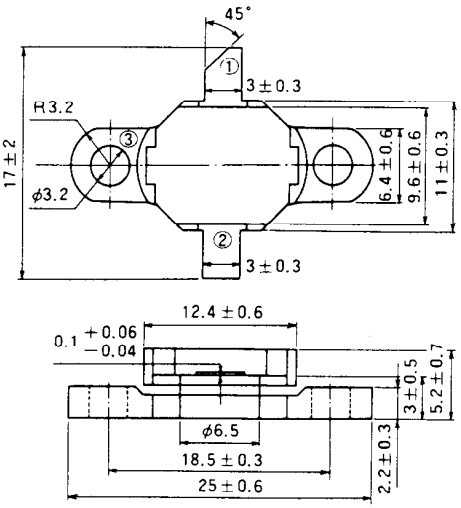
- High power gain: $G_{pb} \geqq 4.5$dB, P_O = 28W @V_{CC} = 28V, f = 1.65GHz.
- High ruggedness: Ability to withstand 16:1 load VSWR when operated at V_{CC} = 28V, f = 1.65 GHz, P_O = 28W.
- Emitter ballasted construction. Gold metalization die.

APPLICATION

For final stage (parallel or push-pull operation) of 50W, 1.6 — 1.65GHz, 28V, amplifier.

OUTLINE DRAWING

Dimensions in mm



PIN :
① COLLECTOR
② EMITTER
③ BASE (FLANGE)

X-139

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CBO}	Collector to base voltage		50	V
V_{EBO}	Emitter to base voltage		4	V
V_{CES}	Collector to emitter voltage	R_{BE} = 0	45	V
I_C	Collector current		7.5	A
P_C	Collector dissipation	T_C = 25°C	90	W
T_j	Junction temperature		175	°C
Tstg	Storage temperature		−55 to 175	°C
R_{th-c}	Thermal resistance	Junction to case	1.7	°C/W

Note. Above parameters are guaranteed independently.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{(BR)EBO}$	Emitter to base breakdown voltage	I_E = 10mA, I_C = 0	4.0			V
$V_{(BR)CBO}$	Collector to base breakdown voltage	I_C = 10mA, I_E = 0	50			V
$V_{(BR)CES}$	Collector to emitter breakdown voltage	I_C = 10mA, R_{EB} = 0	45			V
I_{CBO}	Collector cutoff current	V_{CB} = 25V, I_E = 0			3	mA
h_{FE}	DC forward current gain *	V_{CE} = 5V, I_C = 6A	10	50	180	—
P_O	Output power	V_{CC} = 28V, f = 1.65GHz, P_{in} = 10W	28	32		W
η_C	Collector efficiency		40	45		%

Note. *Pulse test, P_W = 150μs, duty = 5%.
Above parameters, ratings, limits and conditions are subject to change.

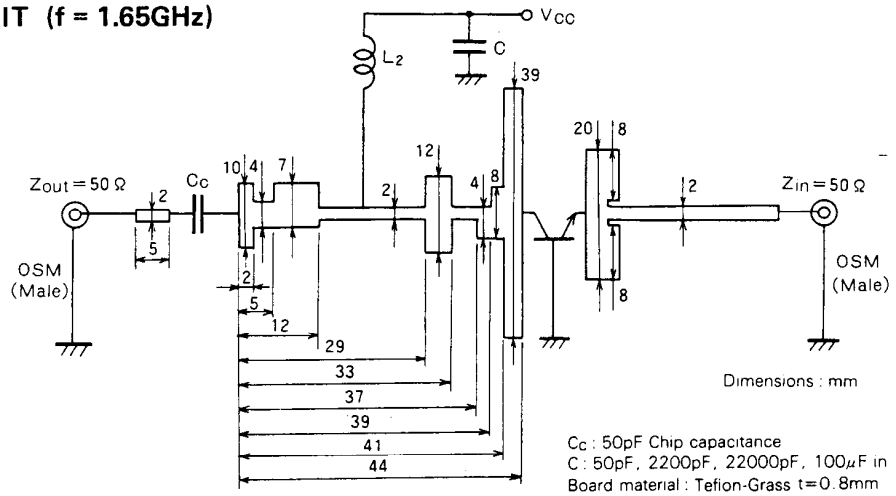
NOV. '97

MITSUBISHI ELECTRIC

2SC4526

NPN EPITAXIAL PLANAR TYPE

TEST CIRCUIT (f = 1.65GHz)

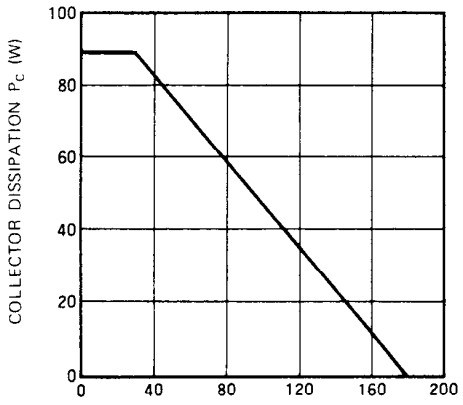


Dimensions : mm

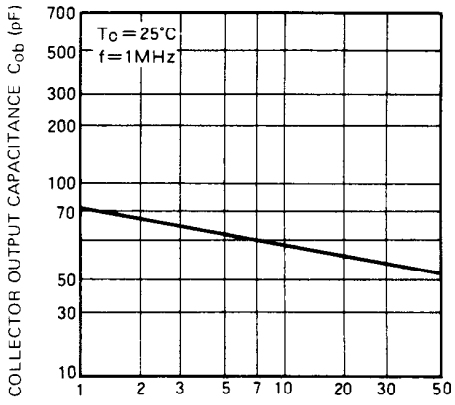
Cc : 50pF Chip capacitance
C : 50pF, 2200pF, 22000pF, 100μF in paralleled
Board material : Tefion-Grass t=0.8mm

TYPICAL PERFORMANCE DATE

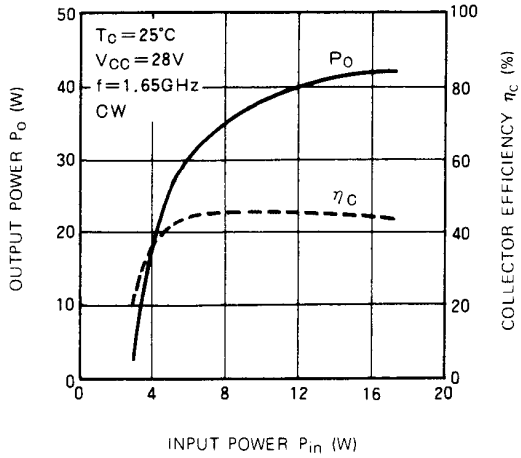
COLLECTOR DISSIPATION VS. CASE TEMPERATURE CHARACTERISTICS



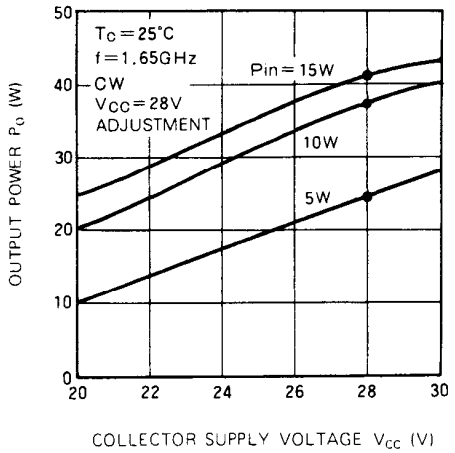
COLLECTOR OUTPUT CAPACITANCE VS. COLLECTOR TO BASE VOLTAGE CHARACTERISTICS



OUTPUT POWER, COLLECTOR EFFICIENCY VS. INPUT POWER CHARACTERISTICS



OUTPUT POWER VS. COLLECTOR SUPPLY VOLTAGE CHARACTERISTICS

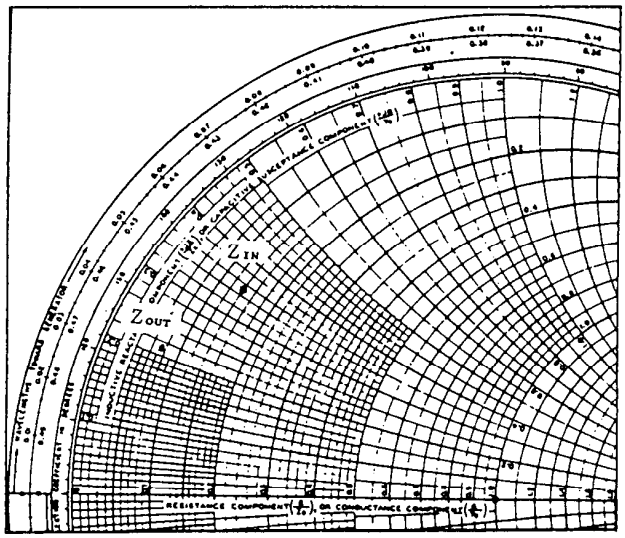


MITSUBISHI ELECTRIC

INPUT AND OUTPUT SERIES IMPEDANCE

f (GHz)	Zin (Ω)	Zout (Ω)
1.65	7.00+j17.5	3.69+j10.6
CONDITIONS : V_{CC}=28V, P_O=28W		

Z_O=50Ω



1. Special Instructions for Flange-Mounted Ceramic-Encapsulated High-Frequency High-Output Transistor Installation

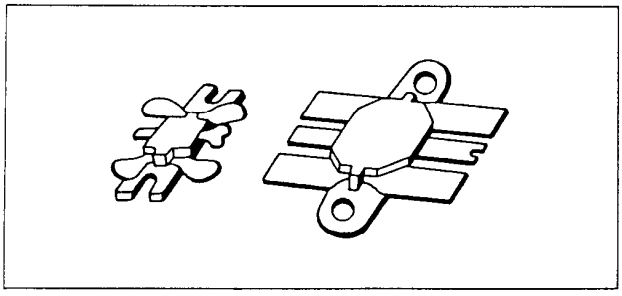


Fig. 1 Flange-Mounted Ceramic Encapsulated High-Frequency High-Output Transistor

When the flange-mounted ceramic-encapsulated transistor shown in Fig. 1 is mounted on a heat sink plate, be sure to follow the special instructions below, after referring to Fig. 2.

(1) Be sure to use M3 x 0.5 screws for mounting the transistor.

(2) Be sure that the fastening screws are tightened to a torque of 5 to 6kg.cm.

(3) Application of lubricants (grease): Apply lubricant (grease) to all heat-conducting components, including the bottom of the flange, the fastening screws, inside the flange holes, and the holes of the heat sink fins. Particular care is required in applying the lubricant compound. Be the more careful the greater the higher the operating level of the device concerned is.

(4) Be sure that the screw hole centers of the heat sink fins are spaced at a distance of 18.3 ± 0.2mm and that the holes have a diameter of 3.5mm.

(5) Take care to ensure that when the device is mounted on to the substrate, no tensile stress acting in the upward direction is applied to the leads. Mount so that the printed circuit board is positioned slightly lower than the bottom of the leads.

(6) After the device has been mounted, solder the leads so that the soldering temperature is below 250°C and that the time used for soldering one lead is within 8 seconds.

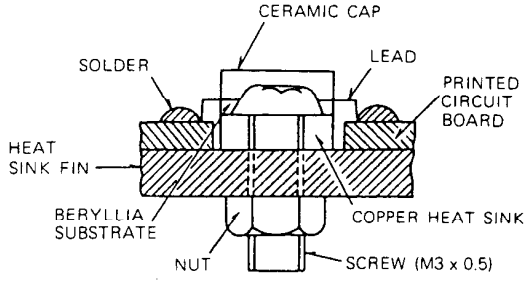


Fig. 2 Installation Procedure for Flange-Mounted Ceramic-Encapsulated Transistor with Printed Pattern on the Upper Surface

2. Precautions for Use of the Device

(1) Operating Junction Temperature (Tjop)

Be sure to design the circuit so that the operating junction temperature Tjop will not exceed 130°C at ambient temperature conditions within 60°C.

(2) Base-Emitter Externally Connected Resistor

If a bias resistor is inserted between the base and emitter for AB class amplifiers, be sure to design the bias circuit so that the resistance remains below 5 ohm. If this resistance value is excessively high, the exciting input will be increased, accordingly and a reverse bias current will be applied between the base and the emitter, thereby iving rise to the problem of a reduction in h_{FE} and a drop in the output power.

(3) Guaranteed Characteristics

All graphic characteristics illustrated in this catalog are typical examples. The characteristics for the individual devices are guaranteed under the specified conditions laid down with respect to the absolute maximum ratings and electrical characteristics.

3. Disposal of Defective or Discarded Products

All types of resin-encapsulated and ceramic-encapsulated high-frequency high-output transistors as well as some metal-encapsulated high-frequency high-output transistors use beryllia porcelain. The inhalation of beryllia dust and/or vapors can be extremely dangerous to the human body. It is therefore essential not to attempt to break, crush, cut, or dispose of these devices at high temperatures (above 800°C) in a moisture-containing atmosphere.