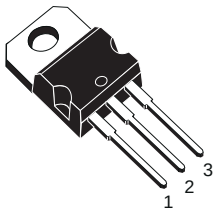
STP62NS04Z

N-CHANNEL CLAMPED 12mΩ - 40A TO-220
FULLY PROTECTED MESH OVERLAY™ MOSFET

ADVANCED DATA

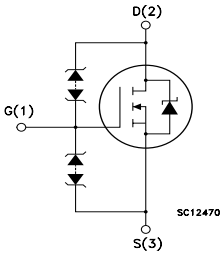
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP62NS04Z	CLAMPED	< 0.014 Ω	40 A (*)

- TYPICAL $R_{DS}(on)$ = 0.012 Ω
- 100% AVALANCHE TESTED
- LOW CAPACITANCE AND GATE CHARGE
- 175°C MAXIMUM JUNCTION TEMPERATURE



TO-220

INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

This fully clamped MOSFET is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment .Any other application requiring extra ruggedness is also recommended.

APPLICATIONS

- ABS,SOLENOID DRIVERS
- POWER TOOLS

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP62NS04Z	P62NS04Z	TO-220	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	CLAMPED	V
V_{DG}	Drain-gate Voltage	CLAMPED	V
V_{GS}	Gate- source Voltage	CLAMPED	V
I_D (*)	Drain Current (continuous) at T_C = 25°C	40	A
I_D (*)	Drain Current (continuous) at T_C = 100°C	40	A
I_{DG}	Drain Gate Current (continuous)	± 50	mA
I_{GS}	Gate Source Current (continuous)	± 50	mA
I_{DM} (•)	Drain Current (pulsed)	160	A
P_{TOT}	Total Dissipation at T_C = 25°C	110	W
	Derating Factor	0.74	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	5	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	500	mJ
V_{ESD}	ESD(HBM-C=100 pF, R=1.5 KΩ)	8	kV
T_{stg}	Storage Temperature	– 55 to 175	°C
T_j	Operating Junction Temperature		

(•)Pulse width limited by safe operating area
(*) Current Limited by Package
(1) I_{SD} ≤40A, di/dt ≤100A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.
(2) Starting T_j = 25 °C, I_D = 20A, V_{DD} = 20 V

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.36	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose (1.6mm from case, for 10sec)	300	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Clamped Voltage	I_D = 1 mA, V_{GS} = 0	33			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = 16 V			TBD	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±10 V			TBD	µA
V_{GSS}	Gate-Source Breakdown Voltage	I_{GS} = ±100 µA	18			V

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 20 A		12	14	mΩ

ELECTRICAL CHARACTERISTICS (CONTINUED)

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V ,I_D = 18 A		17.5		S
C_{iss}	Input Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		1330		pF
C_{oss}	Output Capacitance			420		pF
C_{rss}	Reverse Transfer Capacitance			135		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Q_g	Total Gate Charge	V_{DD} = 20 V, I_D = 40 A, V_{GS} = 10 V		34	47	nC
Q_{gs}	Gate-Source Charge			10		nC
Q_{gd}	Gate-Drain Charge			11.5		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off Voltage Rise Time	V_{CLAMP} = 30 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 10 V (see test circuit, Figure 5)		30		ns
t_f	Fall Time			54		ns
t_c	Cross-over Time			90		ns
t_d	Turn Off Delay Time			36		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				40	A
I_{SDM} (2)	Source-drain Current (pulsed)				160	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 40 A, V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 40 A, di/dt = 100 A/µs V_{DD} = 20 V, T_j = 150°C (see test circuit, Figure 5)		45		ns
Q_{rr}	Reverse Recovery Charge			65		nC
I_{RRM}	Reverse Recovery Current			2.9		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

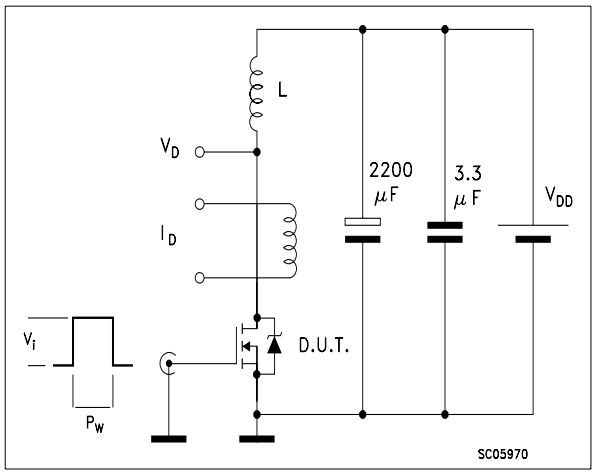


Fig. 2: Unclamped Inductive Waveform

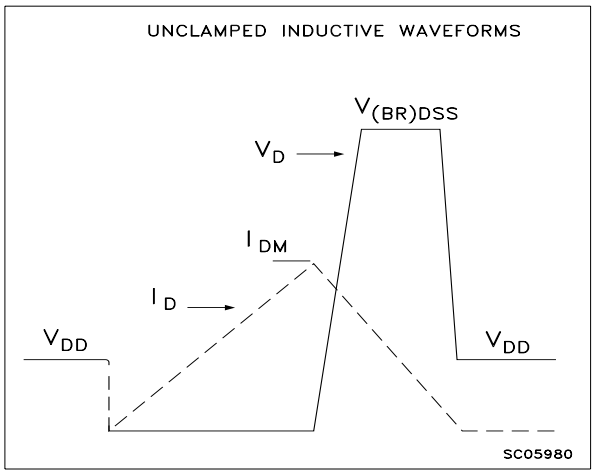


Fig. 3: Switching Times Test Circuit For Resistive Load

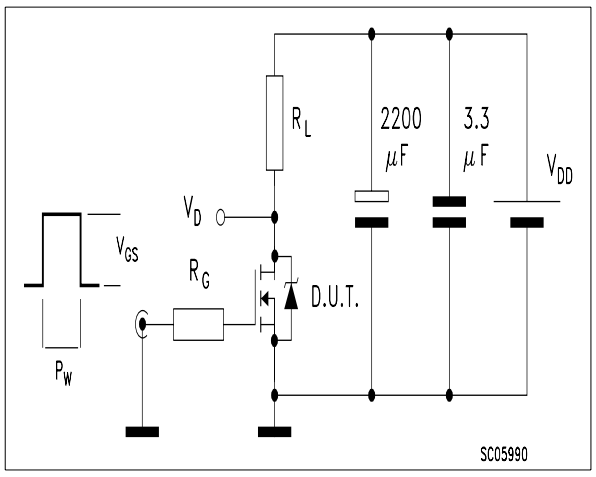


Fig. 4: Gate Charge test Circuit

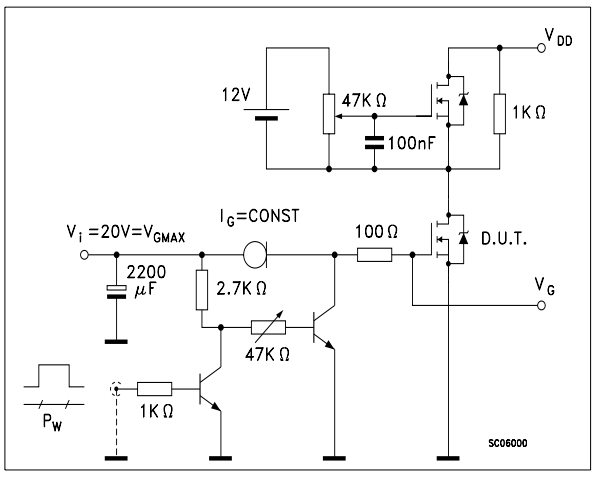
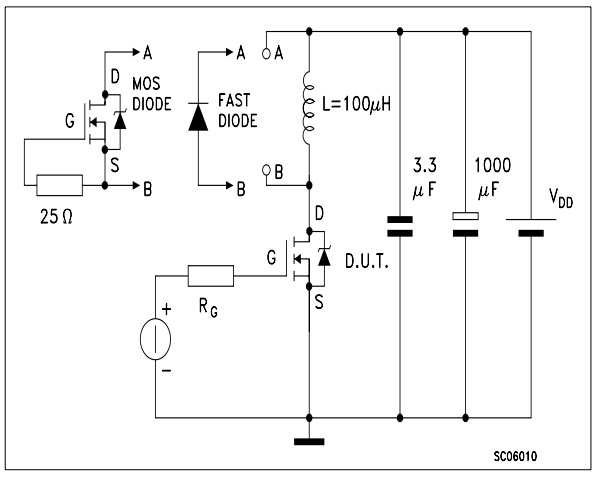


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116