2N7116 SERIES

Siliconix incorporated

N-Channel Lateral DMOS Quad FETs

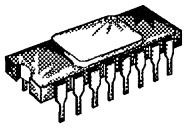
The Siliconix 2N7116 series is a monolithic array of single-pole, single-throw analog switches designed for high speed switching in audio, video and high frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the 2N7116 is rated for analog signals of ±10 V, while the 2N7117 and 2N7118 are rated for ±5 V and ±7.5 V respectively.

These bidirectional switches feature very low interelectrode capacitance and on-resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

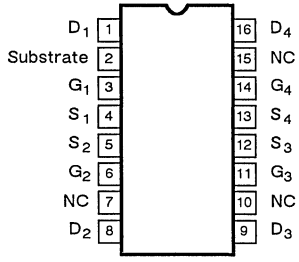
For additional design information please see performance curves DMCA-1B, which are located in Section 7.

PART NUMBER	$V_{(BR)DS}$ MIN (V)	$V_{GS(th)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	t_{ON} MAX (ns)
2N7116	20	2.0	70	2
2N7117	10	2.0	70	2
2N7118	15	2.0	70	2

16-PIN DIP
SIDE BRAZE QUAD



TOP VIEW



SIMILAR PRODUCTS

- SOT-143, See SST211 Series
- TO-18, See SD211DE Series
- SO-14, See SD5400 Series
- Chips, Order 2N711XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT 2N7116	LIMIT 2N7117	LIMIT 2N7118	UNITS
Gate-Source, Gate-Drain Voltage		V_{GS}, V_{GD}	25/–25	25/–15	30/–22.5	V
Drain-Substrate, Source-Substrate Voltage		V_{DB}, V_{SB}	25	15	22.5	V
Drain-Source, Source-Drain Voltage		V_{DS}, V_{SD}	20	10	15	V
Gate-Substrate Voltage [1]		V_{GB}	30/–0.3	25/–0.3	30/–0.3	V
Drain Current		I_D	50			mA
Power Dissipation	Package	P_D	640			mW
	Each Device		300			mW
Power Derating (Package)			5			mW/°C
Operating Junction Temperature		T_J	–55 to 125			°C
Storage Temperature		T_{stg}	–55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

[1]These devices feature an internal Zener procted gate.

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					2N7116		2N7117		2N7118		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Drain-Source Breakdown Voltage[3]	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10\,\mu A$		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage[3]	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_D = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage[3]	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA	Source OPEN	35	15		15		25		
Source-Substrate Breakdown Voltage[3]	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10\,\mu A$	Drain OPEN	35	15		15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4				10			nA
			$V_{DS} = 15$ V	0.7						10	
			$V_{DS} = 20$ V	0.9		10					
		$V_{GS} = V_{BS} = -5$ V, $T_A = 125°C$	$V_{DS} = 10$ V	0.4				5			µA
			$V_{DS} = 15$ V	0.7						5	
			$V_{DS} = 20$ V	0.9		5					
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5				10			nA
			$V_{SD} = 15$ V	0.7						10	
			$V_{SD} = 20$ V	1		10					
		$V_{GD} = V_{BD} = -5$ V, $T_A = 125°C$	$V_{SD} = 10$ V	0.5				5			µA
			$V_{SD} = 15$ V	0.7						5	
			$V_{SD} = 20$ V	1		5					
Gate Leakage	I_{GSS}	$V_{DS} = V_{SB} = 0$ V	$V_{GS} = 25$ V					1			
			$V_{GS} = 30$ V			1				1	
		$V_{DS} = V_{SB} = 0$ V, $T_A = 125°C$	$V_{GS} = 25$ V					10			
			$V_{GS} = 30$ V			10				10	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = V_{BS} = 0$ V				10					
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_D = 1\,\mu A$, $V_{SB} = 0$ V		0.7	0.1	2	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{GS} = 5$ V, $I_D = 1$ mA, $V_{BS} = 0$ V		58		70		70		70	Ω
DYNAMIC											
Forward Transconductance[3]	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, f = 1 kHz		11							mS
Output Conductance[3]	g_{os}			0.9							
Gate Node Capacitance	C_{iss}	$V_{DS} = 10$ V, f = 1 MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5		3.5	pF
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5		0.5	
SWITCHING											
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\,\Omega$, $V_{IN} = 5$ V, $R_G = 50\,\Omega$		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-OFF Time [3]	$t_{d(OFF)}$			2							
	t_f			6							

NOTES: 1. $T_A = 25°C$ unless otherwise noted.
2. For design aid only, not subject to production testing.
3. This parameter not registered with JEDEC.

5