

**2N65-TC****Power MOSFET****2A, 650V N-CHANNEL  
POWER MOSFET****■ DESCRIPTION**

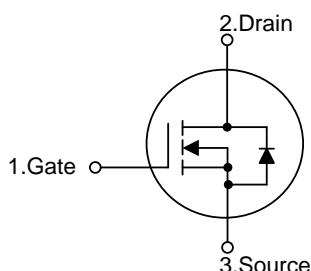
The UTC 2N65-TC is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC 2N65-TC is generally applied in high efficiency switch mode power supplies.

**■ FEATURES**

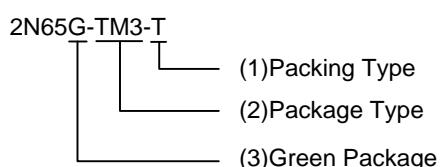
\*  $R_{DS(ON)} \leq 4.8 \Omega$  @  $V_{GS}=10V$ ,  $I_D=1.0A$

\* High Switching Speed

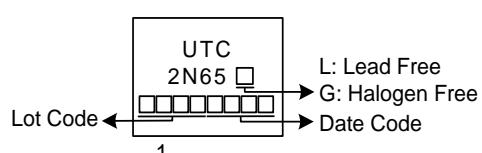
**■ SYMBOL****■ ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2N65L-TM3-T	2N65G-TM3-T	TO-251	G	D	S	Tube
2N65L-TMS4-T	2N65G-TMS4-T	TO-251S4	G	D	S	Tube
2N65L-TN3-R	2N65G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source



(1) T: Tube, R: Tape Reel  
 (2) TM3: TO-251, TMS4: TO-251S4, TN3: TO-252  
 (3) G: Halogen Free and Lead Free, L: Lead Free

**■ MARKING**

**■ ABSOLUTE MAXIMUM RATINGS** ( $T_C = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	650	V
Gate-Source Voltage		$V_{GSS}$	$\pm 30$	V
Drain Current	Continuous	$I_D$	2	A
	Pulsed (Note 2)	$I_{DM}$	4	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	101	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.8	V/ns
Power Dissipation		$P_D$	44	W
Junction Temperature		$T_J$	+150	$^\circ\text{C}$
Storage Temperature		$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L = 30\text{mH}$ ,  $I_{AS} = 2.6\text{A}$ ,  $V_{DD} = 90\text{V}$ ,  $R_G = 25 \Omega$  Starting  $T_J = 25^\circ\text{C}$

4.  $I_{SD} \leq 2.0\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$

**■ THERMAL DATA**

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	$\theta_{JA}$	110	$^\circ\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	2.87	$^\circ\text{C}/\text{W}$

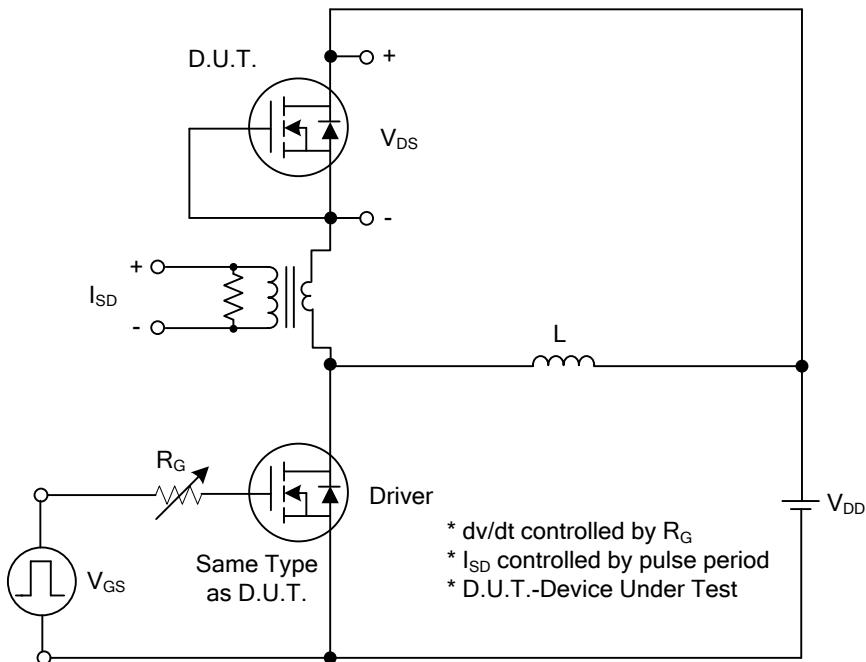
**■ ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$	650			V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=650\text{V}$ , $V_{GS}=0\text{V}$			10	$\mu\text{A}$
Gate-Source Leakage Current	Forward	$I_{GSS}$	$V_{GS}=30\text{V}$ , $V_{DS}=0\text{V}$		100	nA
	Reverse		$V_{GS}=-30\text{V}$ , $V_{DS}=0\text{V}$		-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=1.0\text{A}$			4.8	$\Omega$
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	$C_{ISS}$	$V_{GS}=0\text{V}$ , $V_{DS}=25\text{V}$ , $f=1.0\text{ MHz}$		301		pF
Output Capacitance	$C_{OSS}$			38		pF
Reverse Transfer Capacitance	$C_{RSS}$			2.5		pF
<b>SWITCHING CHARACTERISTICS</b>						
Total Gate Charge (Note 1)	$Q_G$	$V_{DS}=520\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=2\text{A}$ $I_G=1\text{mA}$ (Note 1, 2)		7.5		nC
Gate-source Charge	$Q_{GS}$			3		nC
Gate-Drain Charge	$Q_{GD}$			1		nC
Turn-on Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=100\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=2\text{A}$ , $R_G=25\Omega$ (Note 1, 2)		6		ns
Rise Time	$t_R$			16		ns
Turn-off Delay Time	$t_{D(OFF)}$			22		ns
Fall-Time	$t_F$			24		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$				2	A
Maximum Body-Diode Pulsed Current	$I_{SM}$				4	A
Drain-Source Diode Forward Voltage (Note 1)	$V_{SD}$	$V_{GS}=0\text{V}$ , $I_S=2.0\text{A}$			1.4	V
Reverse Recovery Time (Note 1)	$t_{rr}$	$V_{GS}=0\text{V}$ , $I_S=2.0\text{A}$ , $dl_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		205		ns
Reverse Recovery Charge	$Q_{rr}$			2.3		$\mu\text{C}$

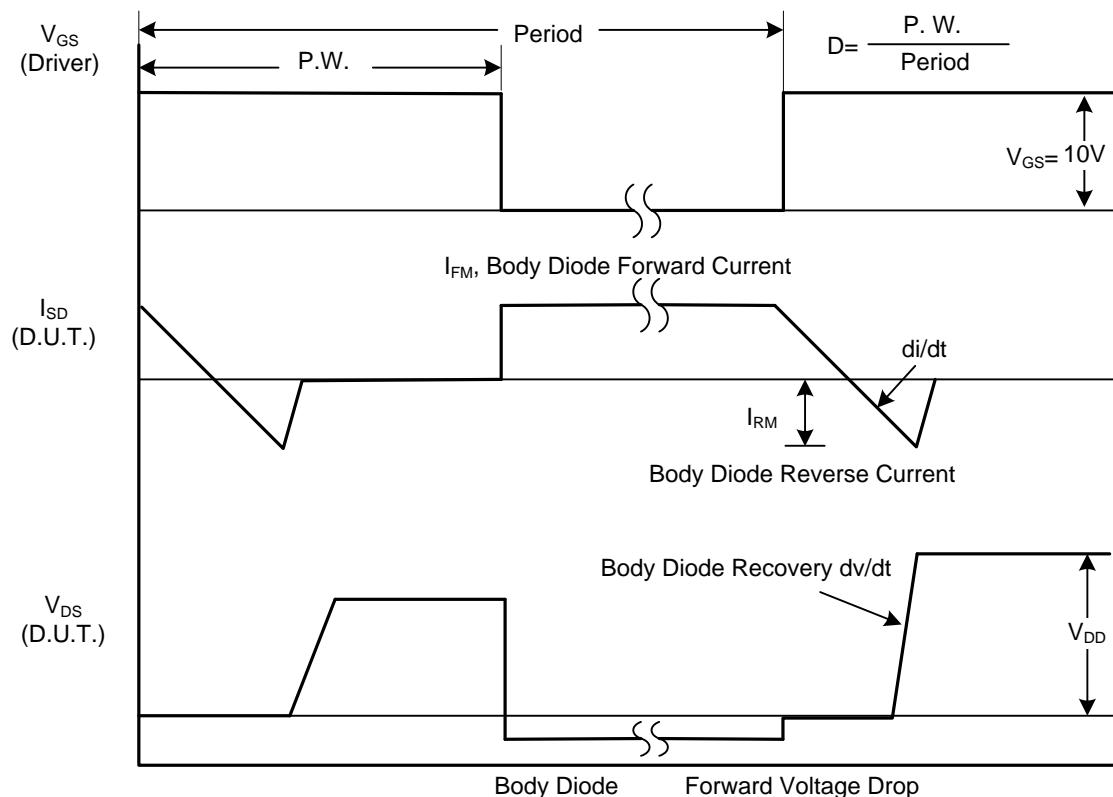
Notes: 1. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating temperature.

## ■ TEST CIRCUITS AND WAVEFORMS

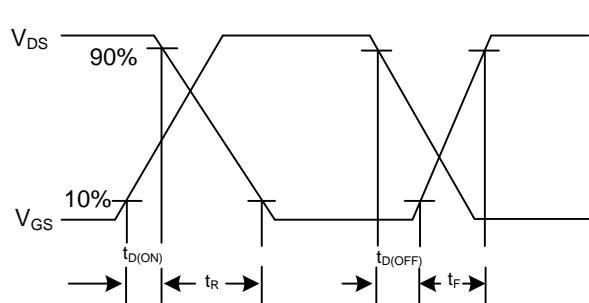
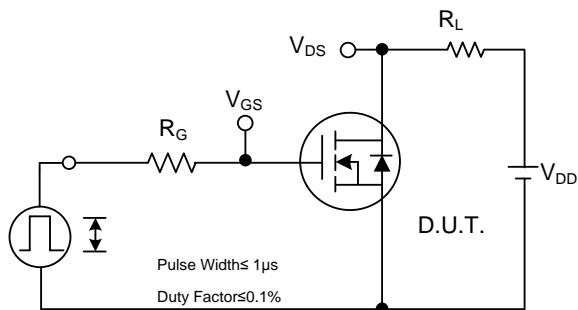


Peak Diode Recovery dv/dt Test Circuit



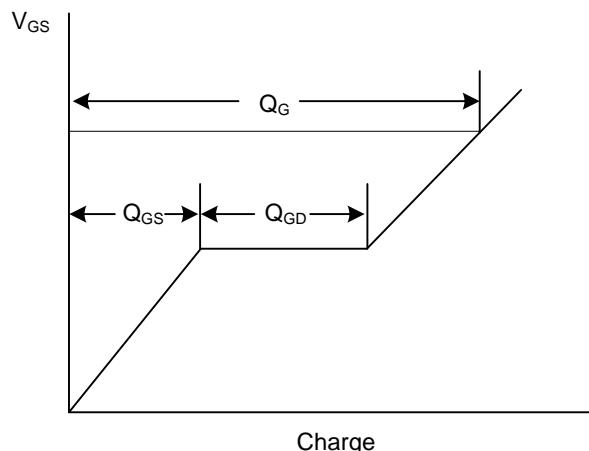
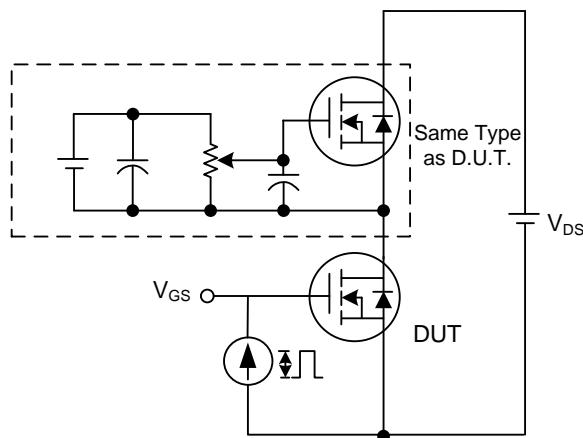
Peak Diode Recovery dv/dt Waveforms

### ■ TEST CIRCUITS AND WAVEFORMS



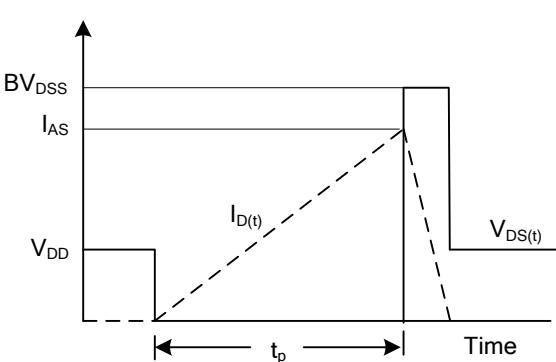
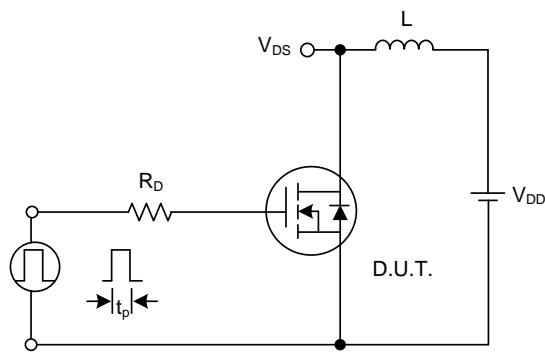
**Switching Test Circuit**

**Switching Waveforms**



**Gate Charge Test Circuit**

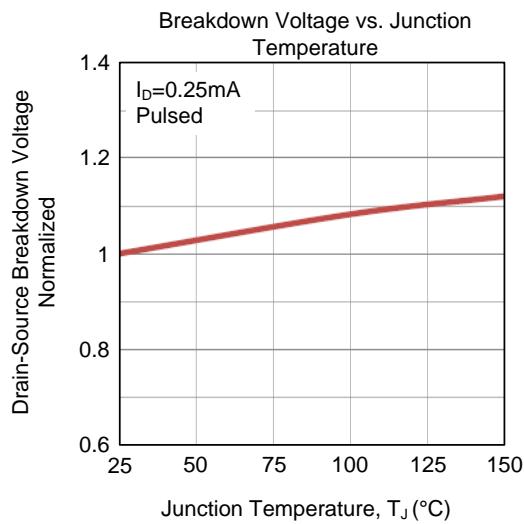
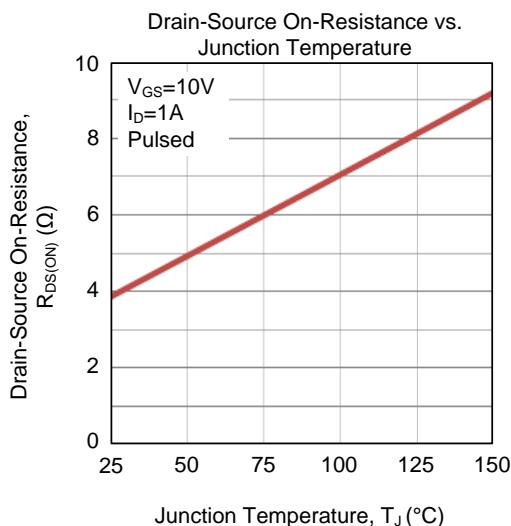
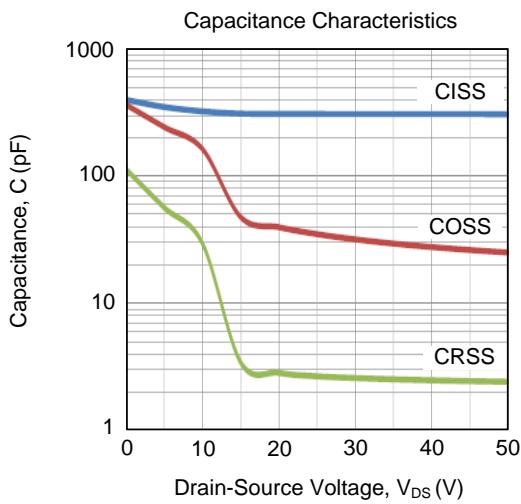
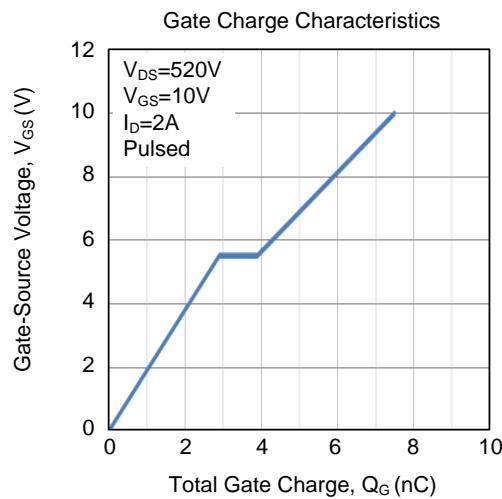
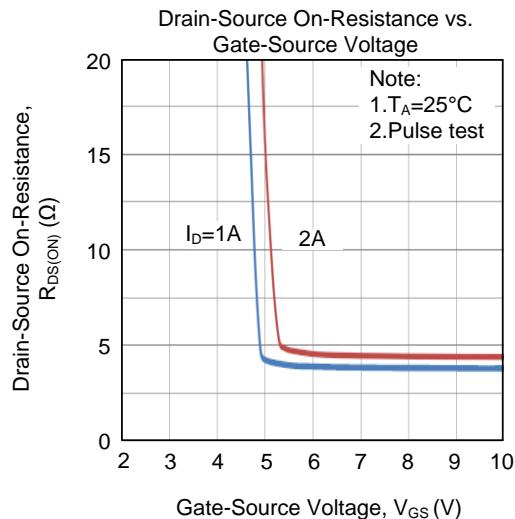
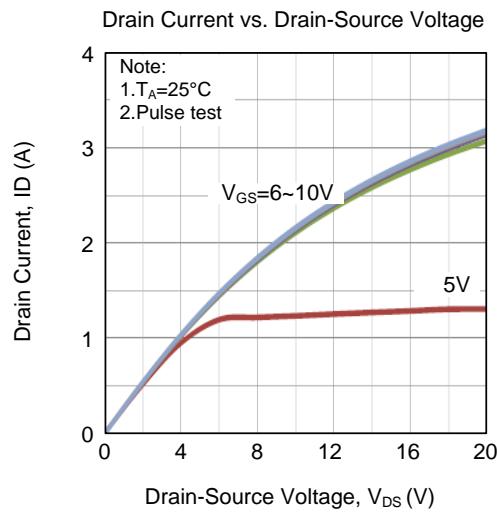
**Gate Charge Waveform**



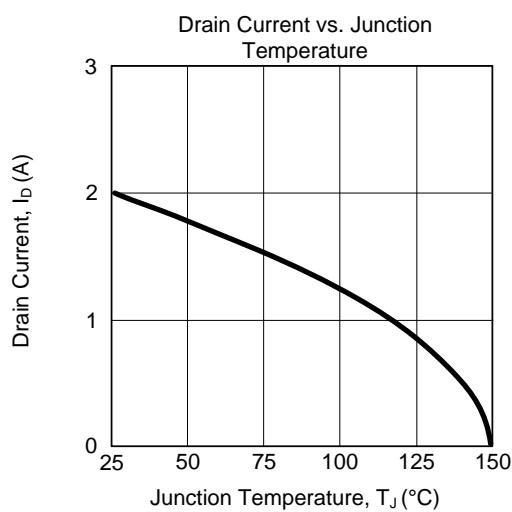
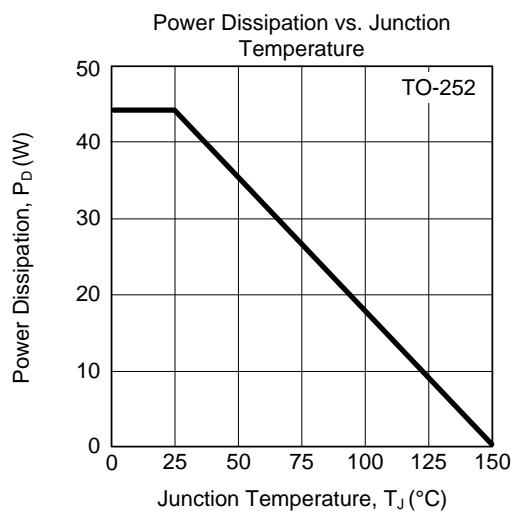
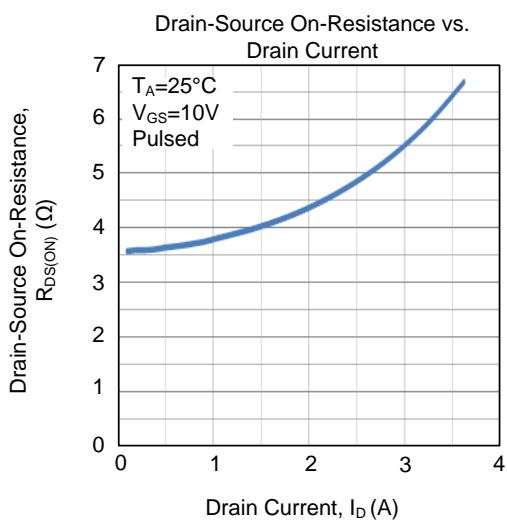
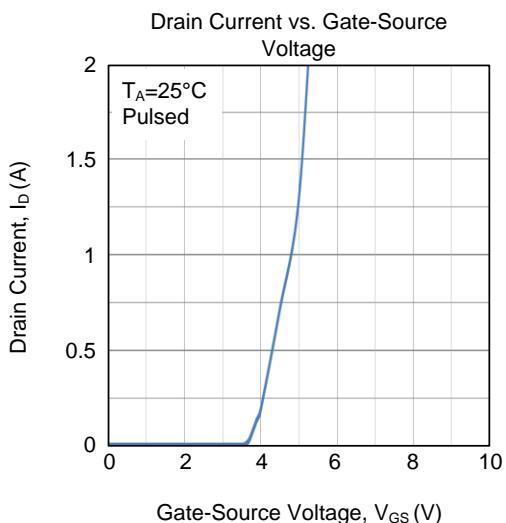
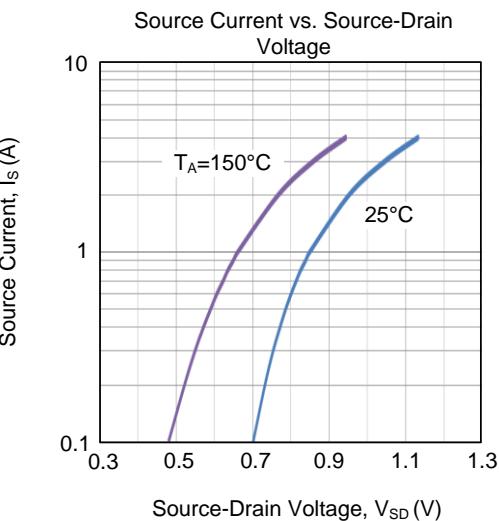
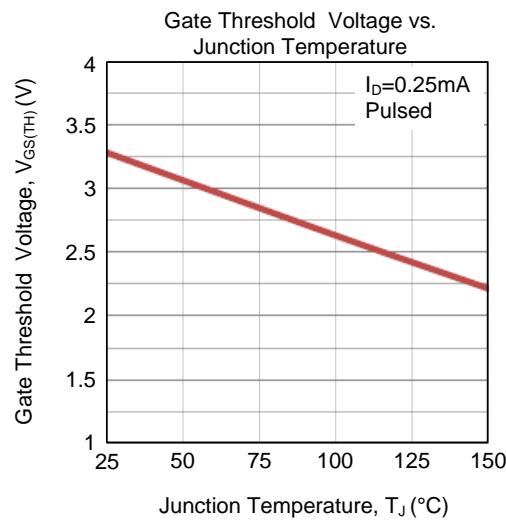
**Unclamped Inductive Switching Test Circuit**

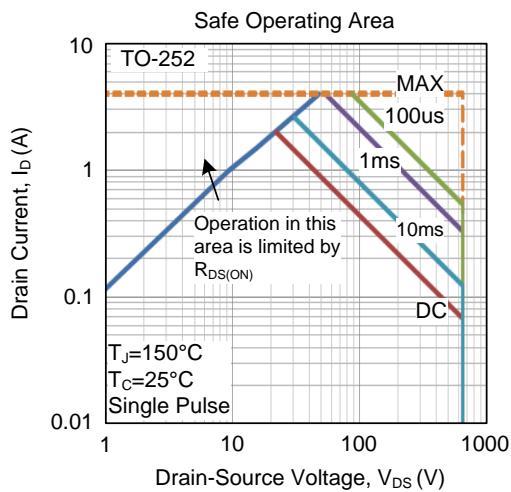
**Unclamped Inductive Switching Waveforms**

## ■ TYPICAL CHARACTERISTICS



### ■ TYPICAL CHARACTERISTICS (Cont.)



**■ TYPICAL CHARACTERISTICS (Cont.)**

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