

2N6441 (SILICON)

thru

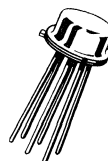
2N6448

MULTIPLE SILICON ANNULAR MONOLITHIC TRANSISTORS

... designed for use as differential amplifiers, dual general-purpose amplifiers, front end detectors and temperature compensation applications.

- Excellent Temperature Tracking — 2N6445 thru 2N6448
 $\Delta|V_{BE1} - V_{BE2}| = 0.8 \text{ mVdc (Max) @ } -55 \text{ to } +25^{\circ}\text{C}$
 $= 1.0 \text{ mVdc (Max) @ } +25 \text{ to } +125^{\circ}\text{C}$
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 0.1 \text{ Vdc (Typ) @ } I_C = 1.0 \text{ mAdc}$
- DC Current Gain Specified — $10 \mu\text{Adc to } 1.0 \text{ mAdc}$
- High Current-Gain-Bandwidth Product—
 $f_T = 500 \text{ MHz (Typ) @ } I_C = 0.5 \text{ mAdc}$

NPN SILICON MONOLITHIC MULTIPLE TRANSISTORS



*MAXIMUM RATING

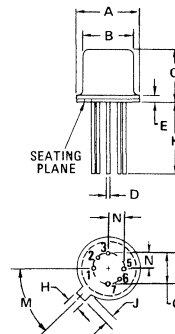
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	45	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	10	mAdc
Total Power Dissipation @ $T_A = 25^{\circ}\text{C}$ Derate above 25°C	$P_D(1)$	550 3.14	mW mW/ $^{\circ}\text{C}$
Total Power Dissipation @ $T_C = 25^{\circ}\text{C}$ Derate above 25°C	$P_D(1)$	1.4 8.0	Watts mW/ $^{\circ}\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^{\circ}\text{C}$

(1) One die or both die with equal power

THERMAL CHARACTERISTICS

Characteristic	Junction to Case	Junction to Ambient	Unit
Thermal Resistance Each Die Effective, 2 Die	125	319	$^{\circ}\text{C/W}$
Coupling Factors	100	100	%

*Indicates JEDEC Registered Data



STYLE 1:
 PIN 1. COLLECTOR 5. EMITTER
 2. BASE 6. BASE
 3. EMITTER 7. COLLECTOR
 4. OMITTED 8. OMITTED

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.70	0.150	0.185
D	0.41	0.53	0.016	0.021
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	—	0.500	—
M	45 $^{\circ}$ BSC		45 $^{\circ}$ BSC	
N	2.54 BSC		0.100 BSC	

CASE 654-07

THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

$$(1) \Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2}$$

Where ΔT_{J1} is the change in junction temperature of die 1
 $R_{\theta 1}$ and $R_{\theta 2}$ is the thermal resistance of die 1 and die 2
 P_{D1} and P_{D2} is the power dissipated in die 1 and die 2
 $K_{\theta 2}$ is the thermal coupling between die 1 and die 2.

An effective package thermal resistance can be defined as follows:

$$(2) R_{\theta(EFF)} = \Delta T_{J1} / P_{DT}$$

Where P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to:

$$(3) \Delta T_{J1} = R_{\theta 1} (P_{D1} + K_{\theta 2} P_{D2})$$

For the conditions where $P_{D1} = P_{D2}$, $P_{DT} = 2 P_D$, equation (3) can be further simplified and by substituting into equation (2) results in:

$$(4) R_{\theta(EFF)} = R_{\theta 1} (1 + K_{\theta 2}) / 2$$

Values for the coupling factors when either the case or the ambient is used as a reference are given in the table on page 1.

***ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 10 \text{ mA}$, $I_B = 0$)	BV_{CEO}	45	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 10 \text{ }\mu\text{A}$, $I_E = 0$)	BV_{CBO}	60	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \text{ }\mu\text{A}$, $I_C = 0$)	BV_{EBO}	6.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 45 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	5.0	nAdc
Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	5.0	nAdc
Collector Cutoff Current ($V_{CE} = 5.0 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	5.0	nAdc
Collector-Collector Leakage Current ($V_{C1-C2} = 100 \text{ Vdc}$)	I_{C1-C2}	—	5.0	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 10 \text{ }\mu\text{A}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 100 \text{ }\mu\text{A}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 100 \text{ }\mu\text{A}$, $V_{CE} = 5.0 \text{ Vdc}$, $T_A = -55^\circ\text{C}$) ($I_C = 1.0 \text{ mA}$, $V_{CE} = 5.0 \text{ Vdc}$)	h_{FE}	60 120 100 200 30 60 125 250	240 600 — — — — — —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0 \text{ mA}$, $I_B = 0.1 \text{ mA}$)	$V_{CE(sat)}$	—	0.3	Vdc
Base-Emitter On Voltage ($I_C = 100 \text{ }\mu\text{A}$, $V_{CE} = 5.0 \text{ Vdc}$)	$V_{BE(on)}$	—	0.7	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (2) ($I_C = 0.5 \text{ mA}$, $V_{CE} = 5.0 \text{ Vdc}$, $f = 20 \text{ MHz}$)	f_T	160	—	MHz
Collector-Base Capacitance ($V_{CB} = 5.0 \text{ Vdc}$, $I_E = 0$, $f = 140 \text{ kHz}$)	C_{cb}	—	1.5	pF
Collector-Collector Capacitance ($V_{C1-C2} = 0$)	C_{C1-C2}	—	1.5	pF
Emitter-Base Capacitance ($V_{BE} = 0.5 \text{ Vdc}$, $I_C = 0$, $f = 140 \text{ kHz}$)	C_{eb}	—	2.0	pF
Noise Figure ($I_C = 10 \text{ }\mu\text{A}$, $V_{CE} = 5.0 \text{ Vdc}$, $R_S = 10 \text{ k ohms}$, $BW = 15.7 \text{ kHz}$) ($I_C = 10 \text{ }\mu\text{A}$, $V_{CE} = 5.0 \text{ Vdc}$, $R_S = 10 \text{ k ohms}$, $f = 10 \text{ kHz}$, $BW = 20 \text{ Hz}$)	NF	— —	4.0 3.0	dB

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Max	Unit
*MATCHING CHARACTERISTICS				
DC Current Gain Ratio (3) ($I_C = 100 \mu\text{Adc}$, $V_{CE} = 5.0 \text{ Vdc}$)	h_{FE1}/h_{FE2}	0.6 0.8 0.9 0.95	1.0 1.0 1.0 1.0	—
Base-Emitter Voltage Differential ($I_C = 10 \mu\text{Adc}$, $V_{CE} = 5.0 \text{ Vdc}$)	$ V_{BE1} - V_{BE2} $	— — —	10 5.0 3.0	mVdc
($I_C = 100 \mu\text{Adc}$, $V_{CE} = 5.0 \text{ Vdc}$)		— — —	10 5.0 3.0	
Base-Emitter Voltage Differential Change Due to Temperature ($I_C = 100 \mu\text{Adc}$, $V_{CE} = 5.0 \text{ Vdc}$, $T_A = -55$ to $+25^\circ\text{C}$)	$\Delta V_{BE1} - V_{BE2} $	— — —	3.2 1.6 0.8	mVdc
($I_C = 100 \mu\text{Adc}$, $V_{CE} = 5.0 \text{ Vdc}$, $T_A = +25$ to $+125^\circ\text{C}$)		— — —	4.0 2.0 1.0	

*Indicates JEDEC Registered Data

(3) The lowest h_{FE} reading is taken as h_{FE1} for this ratio.

NOISE FIGURE
($V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$)

FIGURE 1 – FREQUENCY EFFECTS

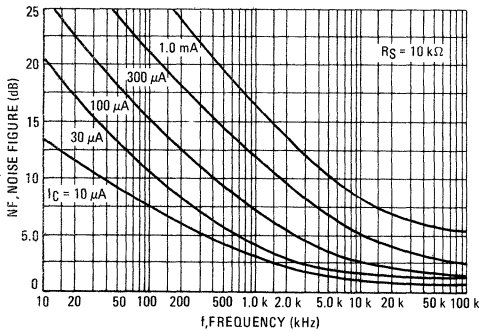


FIGURE 2 – SOURCE RESISTANCE EFFECTS

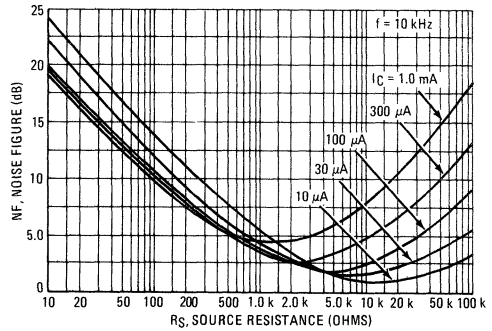


FIGURE 3 – DC CURRENT GAIN

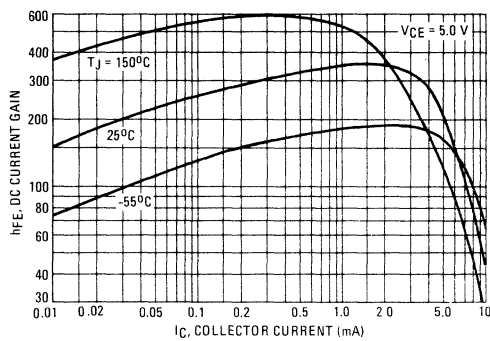


FIGURE 4 – "ON" VOLTAGES

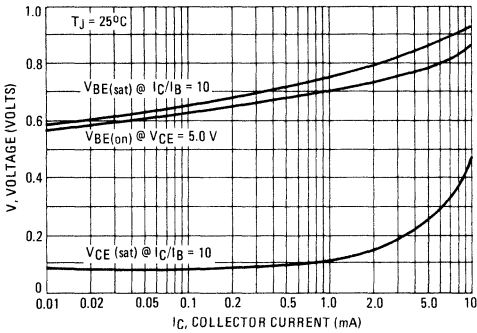


FIGURE 6 – CURRENT-GAIN-BANDWIDTH PRODUCT

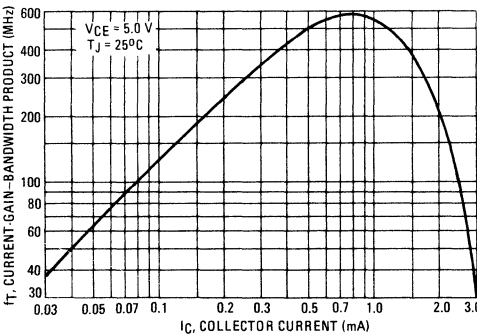


FIGURE 5 – TEMPERATURE COEFFICIENTS

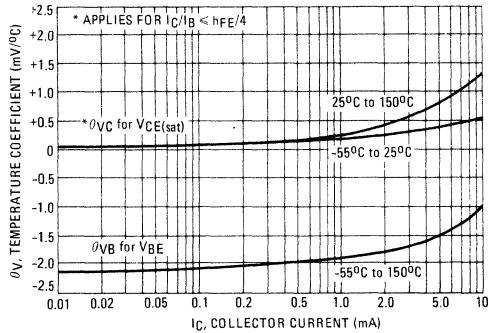


FIGURE 7 – CAPACITANCE

