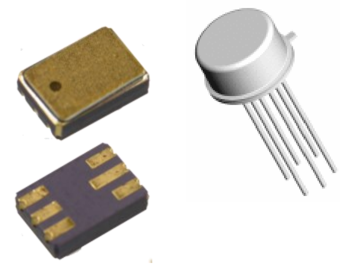
2N5795, 2N5795A, 2N5796
2N5796A, 2N5796AU, 2N5796U

PNP Dual Silicon Transistors

Rev. V3

Features

- Available in JAN, JANTX, JANTXV, JANS and JANSR per MIL-PRF-19500/496
- TO-78 and U package types
- Radiation Tolerant Levels M, D, P, L, and R



Electrical Characteristics (+25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Off Characteristics					
Collector - Emitter Breakdown Voltage	I_C = 10 mA dc	$V_{(BR)CEO}$	V dc	60	—
Collector - Base Cutoff Current	V_{CB} = 60 V dc V_{CB} = 50 V dc	I_{CBO1} I_{CBO2}	μA dc nA dc	—	10 10
Emitter - Base Cutoff Current	V_{EB} = 5.0 V dc V_{EB} = 3.0 V dc	I_{EBO1} I_{EBO2}	μA dc nA dc	—	10 100
On Characteristics[1]					
Forward Current Transfer Ratio	2N5795, 2N5795A V_{CE} = 10 V dc; I_C = 0.1 mA dc V_{CE} = 10 V dc; I_C = 1.0 mA dc V_{CE} = 10 V dc; I_C = 10 mA dc V_{CE} = 10 V dc; I_C = 150 mA dc V_{CE} = 10 V dc; I_C = 300 mA dc V_{CE} = 1.0 V dc; I_C = 150 mA dc	 h_{FE1} h_{FE2} h_{FE3} h_{FE4} h_{FE5} h_{FE6}	h_{FE}	 40 40 40 40 20 20	 150
	2N5796, 2N5796U 2N5796A V_{CE} = 10 V dc; I_C = 0.1 mA dc V_{CE} = 10 V dc; I_C = 1.0 mA dc V_{CE} = 10 V dc; I_C = 10 mA dc V_{CE} = 10 V dc; I_C = 150 mA dc V_{CE} = 10 V dc; I_C = 300 mA dc V_{CE} = 1.0 V dc; I_C = 150 mA dc	 h_{FE1} h_{FE2} h_{FE3} h_{FE4} h_{FE5} h_{FE6}		 75 100 100 100 50 50	 300
Collector - Emitter Saturation Voltage	I_C = 150 mA dc; I_B = 15 mA dc I_C = 500 mA dc; I_B = 50 mA dc	$V_{CE(SAT)1}$ $V_{CE(SAT)2}$	Vdc	—	0.4 1.6
Base - Emitter Saturation Voltage	I_C = 150 mA dc; I_B = 15 mA dc	$V_{BE(SAT)1}$	Vdc	—	1.3
Base - Emitter Saturation Voltage	I_C = 500 mA dc; I_B = 50 mA dc	$V_{BE(SAT)2}$	Vdc	—	2.6
Forward-Current Transfer Ratio (Gain Ratio) (2N5795A, 2N5796A)	V_{CE} = 10 V dc; I_C = 10 mA dc	$\frac{h_{FE2-1}}{h_{FE2-2}}$		0.9	1.1

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2.0%.

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info@vptcomponents.com

Electrical Characteristics (+25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.
Forward-Current Transfer Ratio (Gain Ratio) (2N5795A, 2N5796A)	V_{CE} = 10 V dc; I_C = 10 mA dc	$\frac{h_{FE3-1}}{h_{FE3-2}}$		0.9	1.1
Absolute Value of Base Emitter-Voltage Differential (2N5795A, 2N5796A)	V_{CE} = 10 V dc; I_C = 1 mA dc	$\lvert V_{BE1}-V_{BE2}\rvert$	mV dc	—	10
Collector-Base Cutoff Current	T_A = +150°C V_{CB} = 50 V dc	I_{CBO3}	µA	—	10
Forward Current Transfer Ratio	T_A = -55°C 2N5795, 2N5795A 2N5796, 2N5796U, 2N5796UC 2N5796, 2N5796AUC	h_{FE7}		 16 40 40	
Collector One to Collector Two Leakage Current	$V_{(1C-2C)}$ = $\pm$50 V dc	$1_{(1C-2C)}$	nA dc		$\pm$1
Dynamic Characteristics					
Magnitude of Common Small-Signal Short-Circuit Forward Current Transfer Ratio	I_C = 20 mA dc, V_{CE} = 20 V dc, f = 100 MHz	$\lvert h_{FE} \rvert$	-	2.0	10
Open Circuit Output Capacitance	V_{CB} = 10 V dc, I_E = 0 mA , 100 kHz ≤ f ≤ 1 MHz	C_{obo}	pF	—	8.0
Input Capacitance (Output Open-Circuited)	V_{EB} = 2.0 V dc; I_C = 0 mA; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}	pF	—	30
Switching Characteristics					
Turn-On Time (saturated)	V_{CC} = 30 V dc; I_C = 150 mA dc; I_{B1} = 15 mA dc	t_{on}	ns	—	50
Turn-Off Time (saturated)	V_{CC} = 30 Vdc; I_C = 150 mA dc; I_{B1} = I_{B2} = 15 mA dc	t_{off}	ns	—	140

Absolute Maximum Ratings

Ratings	Symbol	Value
Collector - Emitter Voltage	V_{CEO}	60 V dc
Collector - Base Voltage	V_{CBO}	60 V dc
Emitter - Base Voltage	V_{EBO}	5.0 V dc
Collector Current	I_C	-600 mA dc
Total Power Dissipation @ T_A = +25°C One Section Total Device	P_T (1) (2)	 0.5 W 0.6 W
Operating & Storage Temperature Range	T_J, T_{STG}	-65°C to +175°C

Thermal Characteristics

Types	$R_{\theta JA}$ One Section	$R_{\theta JA}$ Both Sections	$R_{\theta JSP}$ One Section	$R_{\theta JSP}$ Both Sections	$R_{\theta JPCB}$ One Section	$R_{\theta JPCB}$ Both Sections
	°C/W (2) (3)	°C/W (2) (3)	°C/W (2) (3)	°C/W (2) (3)	°C/W (2) (3)	°C/W (2) (3)
2N5795, 2N5796	350	290				
2N5795A, 2N5796A	350	290				
2N5796U			110	90	350	290
2N5796AU			110	90	350	290

(1) For $T_A \geq 25^oC$, derate linearly 2.86 mW/°C one section, 3.43 mW/°C total.
(2) For 2N5795, 2N5795A, 2N5796, 2N5796A, 2N5796U devices.
(3) For thermal impedance curves see figures 4, 5 and 6 of MIL-PRF-19500/496

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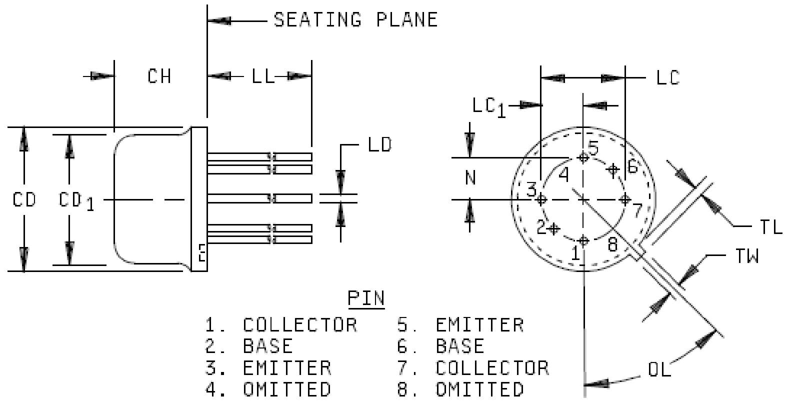
Outline Drawing

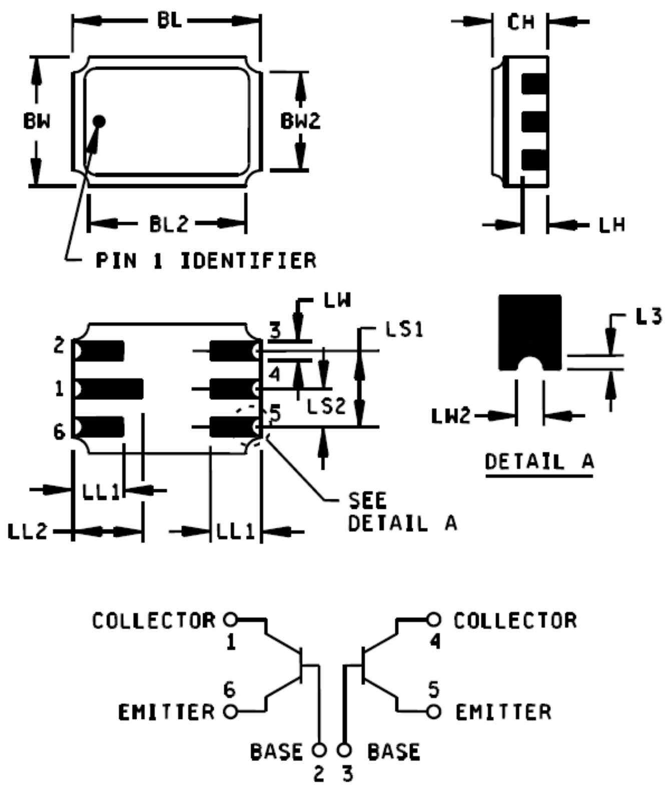


Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.335	.370	8.51	9.40	
CD_1	.305	.335	7.75	8.51	
CH	.150	.185	3.81	4.70	
LD	.016	.021	0.41	0.53	
LC	.200 BSC		5.08 BSC		4
LC_1	.100 BSC		2.54 BSC		4
LL	.500		12.70		
TW	.028	.034	0.71	0.86	
TL	.029	.045	0.74	1.14	3
OL	45° BSC		45° BSC		6
N	.100 BSC		2.54 BSC		

NOTES:
1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Measured from maximum diameter of the product.
4. Leads having maximum diameter .019 inch (0.483 mm) measured in gaging plan .054 inch (1.37 mm) + .001 inch (0.025 mm) - .000 inch (0.000 mm) below the seating plane of the product shall be within .007 inch (.178 mm) of their true position relative to a maximum width tab.
5. The product may be measured by direct methods or by gauge.
6. Tab centerline.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions for 2N5795 and 2N5796 (TO-78).

Outline Drawing



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.240	.250	6.10	6.35
BL_2		.250		6.35
BW	.165	.175	4.19	4.45
BW_2		.175		4.45
CH	.058	.100	1.47	2.54
L_3	.003	.007	0.08	0.18
LH	.026	.039	0.66	0.99

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
LL_1	.060	.070	1.52	1.78
LL_2	.082	.098	2.08	2.49
LS_1	.095	.105	2.41	2.67
LS_2	.045	.055	1.14	1.40
LW	.022	.028	0.56	0.71
LW_2	.006	.022	0.15	0.56

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension "CH" controls the overall package thickness.
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option from that shown on the drawing.
5. Dimensions "LW_2" minimum and "L_3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "LW_2" maximum and "L_3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions, 2N5796U.