

2N4352

CASE 20-03, STYLE 2
TO-72 (TO-206AF)

MOS FET
SWITCHING

P-CHANNEL — ENHANCEMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage	V_{GS}	± 30	Vdc
Gate Current	I_G	30	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 1.7	mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	800 4.56	mW mW/ $^\circ\text{C}$
Junction Temperature Range	T_J	175	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +175	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($I_D = -10\ \mu\text{A}$, $V_{GS} = 0$)	$V_{(BR)DSX}$	-25	—	Vdc
Zero-Gate-Voltage Drain Current ($V_{DS} = -10\ \text{V}$, $V_{GS} = 0$) $T_A = 25^\circ\text{C}$ $T_A = 150^\circ\text{C}$	I_{DSS}	— —	-10 -10	nAdc μAdc
Gate Reverse Current ($V_{GS} = \pm 30\ \text{V}$, $V_{DS} = 0$)	I_{GSS}	—	± 10	pAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = -10\ \text{V}$, $I_D = -10\ \mu\text{A}$)	$V_{GS(Th)}$	-1.0	-5.0	Vdc
Drain-Source On-Voltage ($I_D = -2.0\ \text{mA}$, $V_{GS} = -10\ \text{V}$)	$V_{DS(on)}$	—	-1.0	V
On-State Drain Current ($V_{GS} = -10\ \text{V}$, $V_{DS} = -10\ \text{V}$)	$I_{D(on)}$	-3.0	—	mA

SMALL-SIGNAL CHARACTERISTICS

Drain-Source Resistance ($V_{GS} = -10\ \text{V}$, $I_D = 0$, $f = 1.0\ \text{kHz}$)	$r_{ds(on)}$	—	600	ohms
Forward Transfer Admittance ($V_{DS} = -10\ \text{V}$, $I_D = 2.0\ \text{mA}$, $f = 1.0\ \text{kHz}$)	$ y_{fs} $	1000	—	μmho
Input Capacitance ($V_{DS} = -10\ \text{V}$, $V_{GS} = 0$, $f = 140\ \text{kHz}$)	C_{iss}	—	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 0$, $V_{GS} = 0$, $f = 140\ \text{kHz}$)	C_{rss}	—	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)} = -10\ \text{V}$, $f = 140\ \text{kHz}$)	$C_{d(sub)}$	—	4.0	pF

SWITCHING CHARACTERISTICS

Turn-On Delay (Figures 5)	$I_D = -2.0\ \text{mAdc}$, $V_{DS} = -10\ \text{Vdc}$, $V_{GS} = -10\ \text{V}$ (See Figure 9, Times Circuit Determined)	t_{d1}	—	45	ns
Rise Time (Figures 6)		t_r	—	65	ns
Turn-Off Delay (Figures 7)		t_{d2}	—	60	ns
Fall Time (Figures 8)		t_f	—	100	ns

FIGURE 1 — FOWARD TRANSFER ADMITTANCE

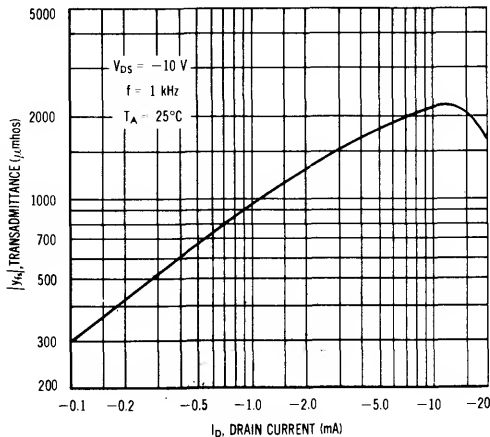


FIGURE 2 — TRANSFER CHARACTERISTICS

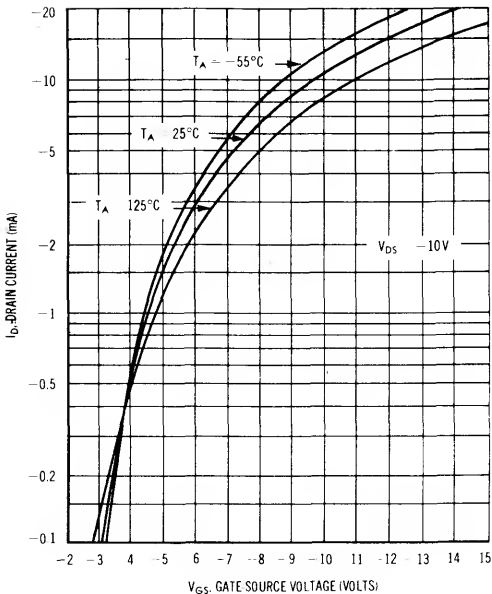


FIGURE 3 — DRAIN-SOURCE "ON" RESISTANCE

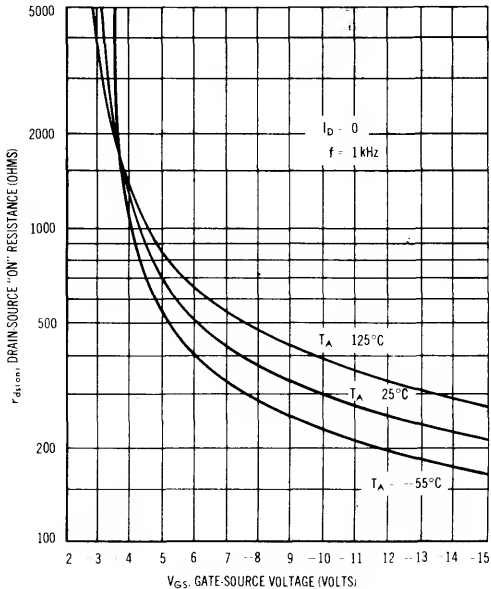
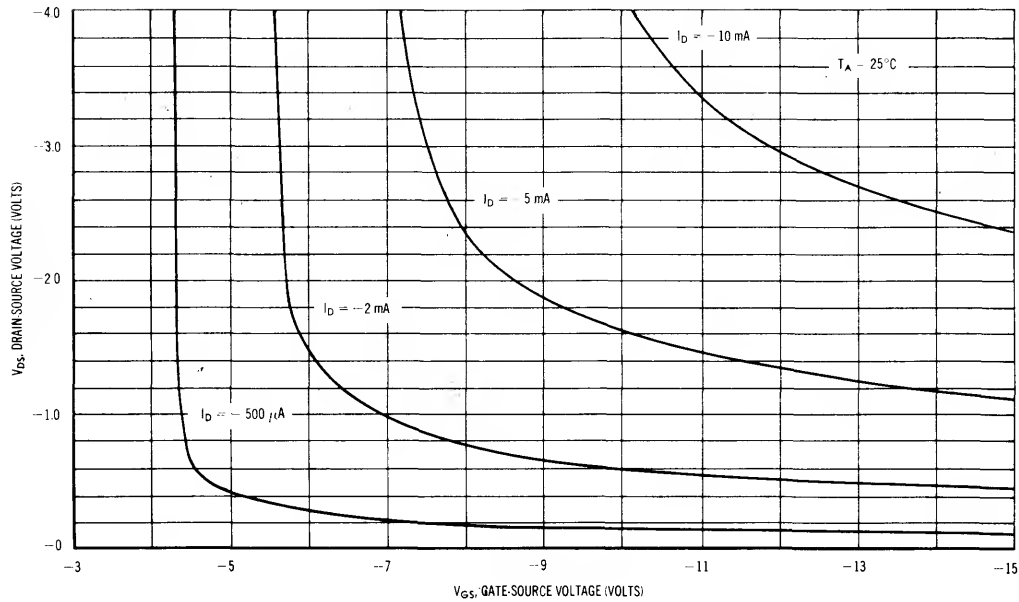


FIGURE 4 — "ON" DRAIN-SOURCE VOLTAGE



SWITCHING CHARACTERISTICS
($T_A = 25^\circ\text{C}$)

FIGURE 5 — TURN-ON DELAY TIME

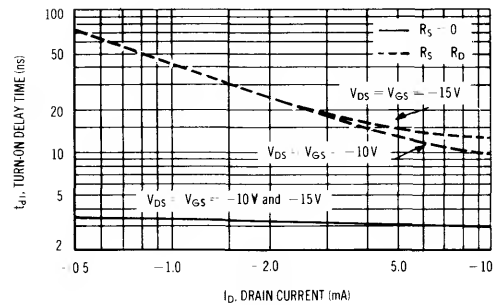


FIGURE 6 — RISE TIME

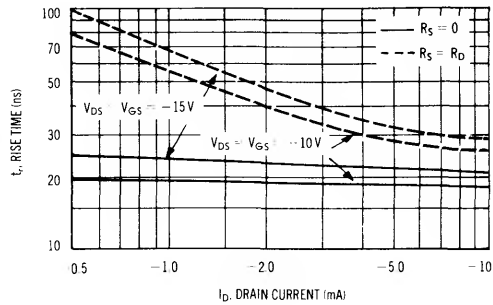


FIGURE 7 — TURN-OFF DELAY TIME

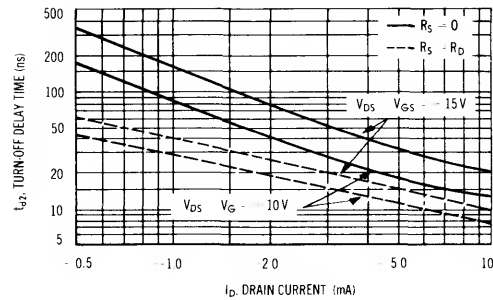


FIGURE 8 — FALL TIME

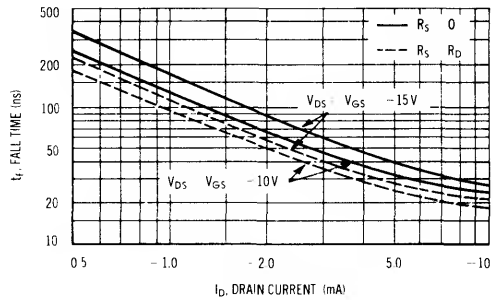
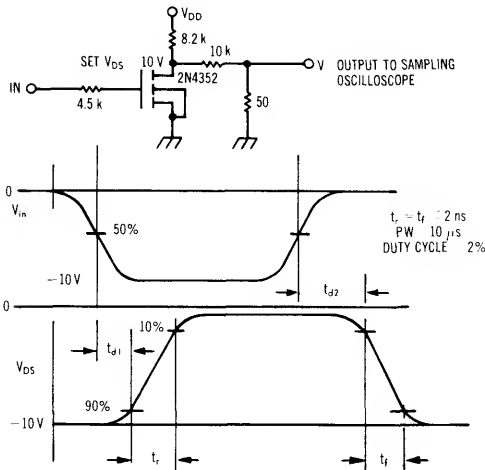


FIGURE 9 — SWITCHING CIRCUIT and WAVEFORMS



The switching characteristics shown above were measured in a test circuit similar to Figure 10. At the beginning of the switching interval, the gate voltage is at ground and the gate-source capacitance ($C_{gs} = C_{iss} - C_{rss}$) has no charge. The drain voltage is at V_{DD} , and thus the feedback capacitance (C_{rss}) is charged to V_{DD} . Similarly, the drain-substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

During the turn-on interval, C_{gs} is charged to V_{GS} (the input voltage) through R_S (generator impedance) (Figure 11). C_{rss} must be discharged to $V_{DS} - V_{GS}$ through R_D and the parallel combination of the load resistor (R_L) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(sat)}$) through R_L in parallel with r_{ds} . During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate-source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 4) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds} , turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_L) will be low compared to R_L during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where $R_S = 0$ and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with $R_S = R_L$ simulate the switching behavior of cascade J stages where the driving source impedance is normally the same as the load impedance. The set of curves with $R_S = 0$ simulates a low source impedance drive such as might occur in complementary logic circuits.

FIGURE 10 — SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL

