24C32
24C64

Bookly Micro

64K-bit/32K-bit
2-WIRE SERIAL CMOS EEPROM

JANUARY 2007

FEATURES

- Two-Wire Serial Interface, I²C™ Compatible
  - –Bi-directional data transfer protocol
- Wide Voltage Operation
  - –Vcc = 1.8V to 5.5V
- 400 KHz (2.5V) and 1MHz (5.0V) Compatible
- Low Power CMOS Technology
  - –Standby Current less than 6 µA (5.0V)
  - –Read Current less than 2 mA (5.0V)
  - –Write Current less than 3 mA (5.0V)
- Hardware Data Protection
  - –24C32/64: WP protects entire array
- Sequential Read Feature
- Filtered Inputs for Noise Suppression
- Self time write cycle with auto clear
  - 5 ms max.@ 2.5V
- Organization:
  - –24C32: 4Kx8 (128 pages of 32 bytes)
  - –24C64: 8Kx8 (256 pages of 32 bytes)
- 32 Byte Page Write Buffer
- High Reliability
  - –Endurance: 1,000,000 Cycles
  - –Data Retention: 100 Years
- Full pin-to-pin with ATMEL and MICROCHIP
- 8-pin PDIP, 8-pin SOIC, 8-pin TSSOP, 8-pad DFN, and 8-pin MSOP packages
- Designed with Samsung technology

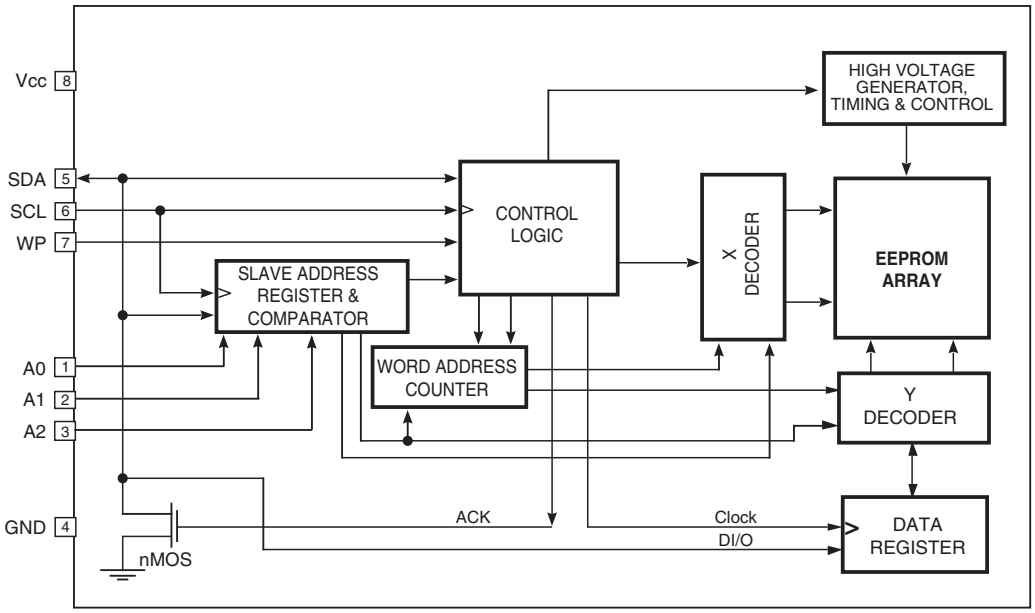
DESCRIPTION

The 24C32 and 24C64 are electrically erasable PROM devices that use the standard 2-wire interface for communications. The 24C32 and 24C64 contain a memory array of 32K-bits (4K x 8) and 64K-bits (8K x 8), respectively. Each device is organized into 32 byte pages for page write mode.

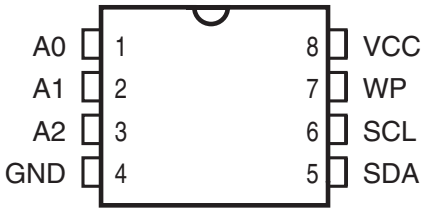
This EEPROM operates in a wide voltage range of 1.8V to 5.5V to be compatible with most application voltages. designed this device family to be a practical, low-power 2-wire EEPROM solution. The devices are available in 8-pin PDIP, 8-pin SOIC, 8-pin TSSOP, 8-pad DFN, and 8-pin MSOP packages.

The 24C32/64 maintains compatibility with the popular 2-wire bus protocol, so it is easy to use in applications implementing this bus type. The simple bus consists of the Serial Clock wire (SCL) and the Serial Data wire (SDA). Using the bus, a Master device such as a microcontroller is usually connected to one or more Slave devices such as this device. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The 24CXX has a Write Protect pin (WP) to allow blocking of any write instruction transmitted over the bus.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
8-Pin DIP, SOIC, TSSOP, and MSOP



PIN DESCRIPTIONS

A0-A2	Address Inputs
SDA	Serial Address/Data I/O
SCL	Serial Clock Input
WP	Write Protect Input
Vcc	Power Supply
GND	Ground

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

SDA

The SDA is a Bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wire-Ored with other open drain or open collector outputs. The SDA bus *requires* a pullup resistor to Vcc.

A0, A1, A2

The A0, A1 and A2 are the device address inputs that are hardwired or left not connected for hardware compatibility with the 24C16. When pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system. When the pins are not hardwired, the default values of A0, A1, and A2 are zero.

WP

WP is the Write Protect pin. The input level determines if all, partial, or none of the array is protected from modifications.

DEVICE OPERATION

24CXX features serial communication and supports a bi-directional 2-wire bus transmission protocol called I²C™.

2-WIRE BUS

The two-wire bus is defined as a Serial Data line (SDA), and a Serial Clock line (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by a Master device that generates the SCL, controls the bus access, and generates the Stop and Start conditions. The 24CXX is the Slave device on the bus.

The Bus Protocol:

– Data transfer may be initiated only when the bus is not busy

– During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated with a Stop condition.

Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

Acknowledge (ACK)

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

Reset

The 24CXX contains a reset function in case the 2-wire bus transmission is accidentally interrupted (eg. a power loss), or needs to be terminated mid-stream. The reset is caused when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

Standby Mode

Power consumption is reduced in standby mode. The 24CXX will enter standby mode: a) At Power-up, and remain in it until SCL or SDA toggles; b) Following the Stop signal if a no write operation is initiated; or c) Following any internal write operation.

DEVICE ADDRESSING

The Master begins a transmission by sending a Start condition. The Master then sends the address of the particular Slave devices it is requesting. The Slave device (Fig. 5) address is 8 bits.

The four most significant bits of the Slave address are fixed as 1010 for the 24CXX.

The next three bits of the Slave address are A0, A1, and A2, and are used in comparison with the hard-wired input values on the A0, A1, and A2 pins. Up to eight 24CXX units may share the 2-wire bus.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master transmits the Start condition and Slave address byte (Fig. 5), the appropriate 2-wire Slave (eg.24C64) will respond with ACK on the SDA line. The Slave will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data. The selected EEPROM then prepares for a Read or Write operation by monitoring the bus.

WRITE OPERATION

Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/$\overline{W}$ set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the two byte address that is to be written into the address pointer of the 24CXX. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The 24CXX acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The 24CXX is capable of 32-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 31 more bytes. After the receipt of each data word, the EEPROM responds immediately with an ACK on SDA line, and the five lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 32 bytes prior to issuing the Stop condition, the address counter will "roll over," and the previously written data will be overwritten. Once all 32 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the 24CXX in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the 24CXX initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the 24CXX has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

READ OPERATION

Read operations are initiated in the same manner as Write operations, except that the (R/$\overline{W}$) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read and sequential read.

Current Address Read

The 24CXX contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the EEPROM receives the Slave Addressing Byte with a Read operation (R/$\overline{W}$ bit set to “1”), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the 24CXX discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the 24CXX acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/$\overline{W}$ bit set to one. The EEPROM then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 9. Random Address Read Diagram.)

Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the 24CXX sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the 24CXX. The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition.

The data output is sequential, with the data from address n followed by the data from address n+1, n+2 ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of 8191 for 24C64 or 4095 for 24C32 (depending on the device) is reached, the address counter “rolls over” to address 0, and the device continues to output data. (Refer to Figure 10. Sequential Read Diagram).

Figure 1. Typical System Bus Configuration

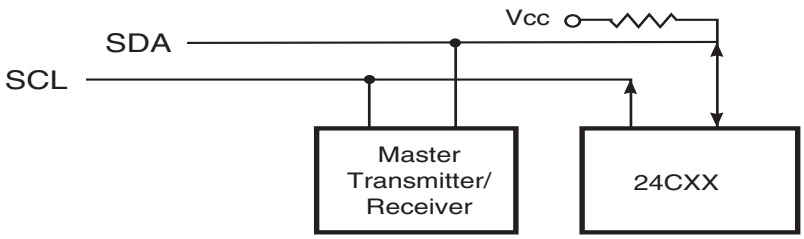


Figure 2. Output Acknowledge

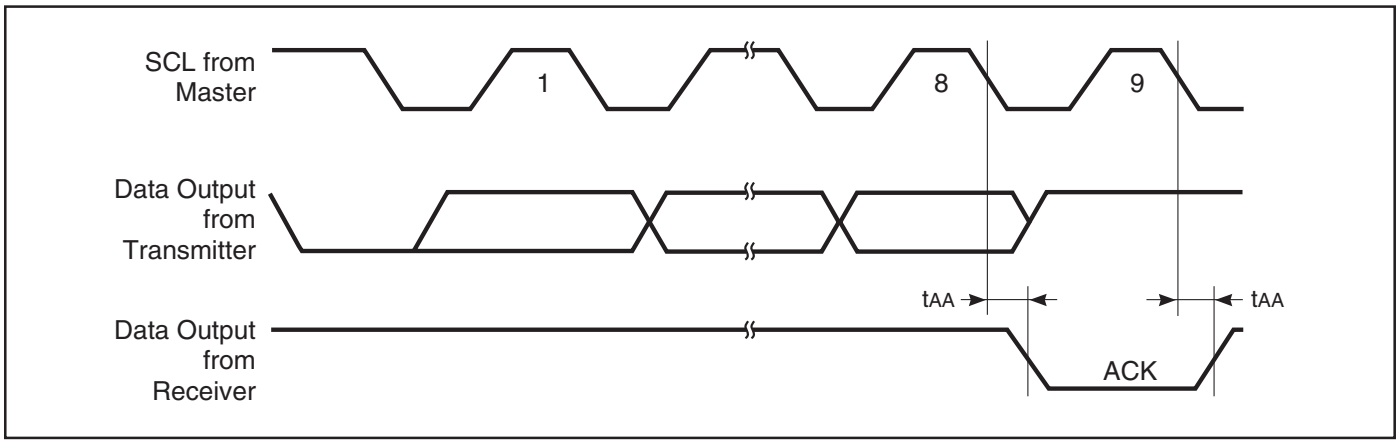


Figure 3. START and STOP Conditions

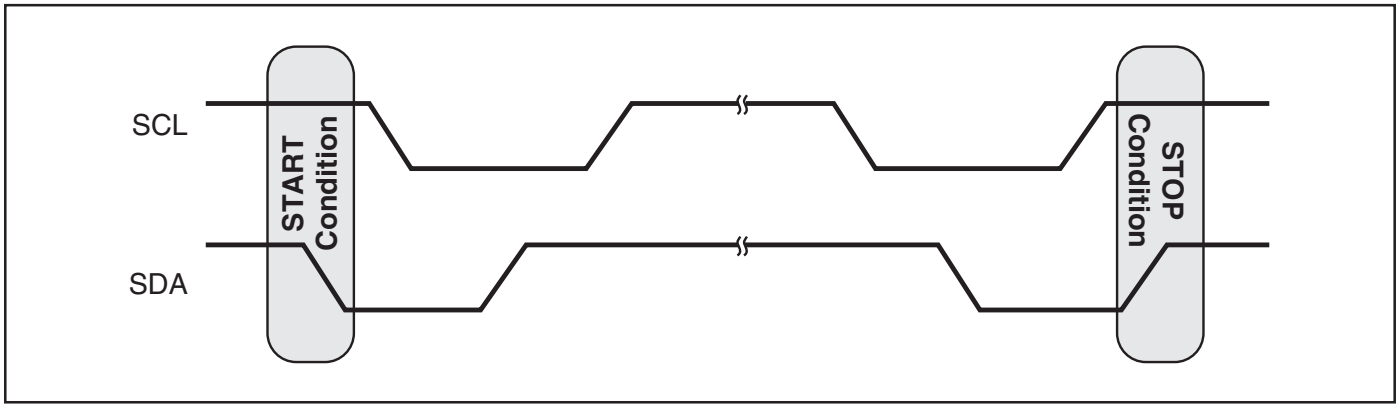


Figure 4. Data Validity Protocol

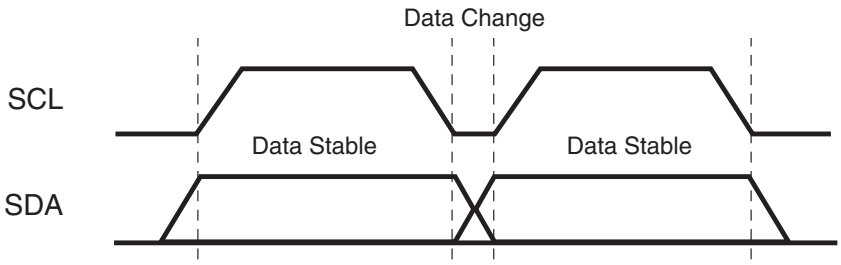


Figure 5. Slave Address

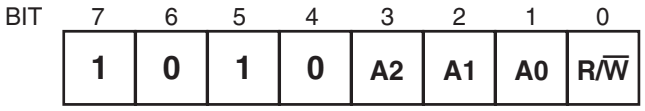


Figure 6. Byte Write

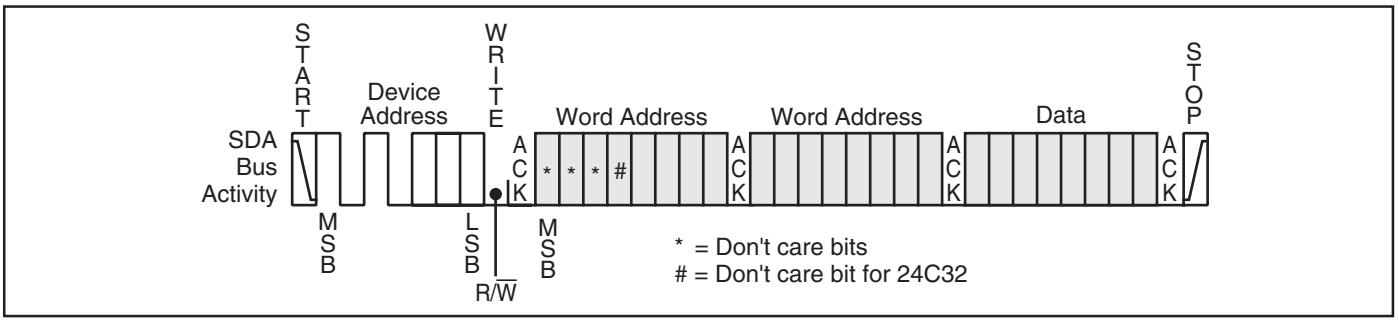


Figure 7. Page Write

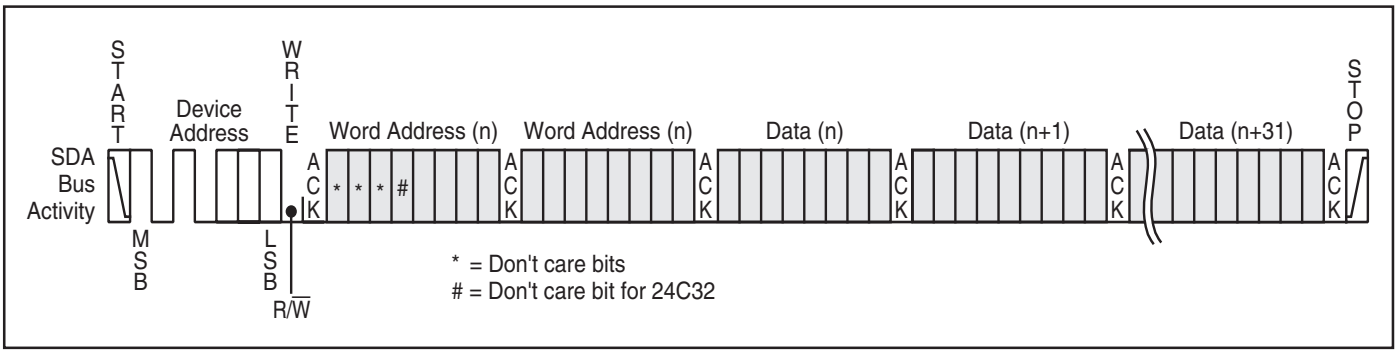


Figure 8. Current Address Read

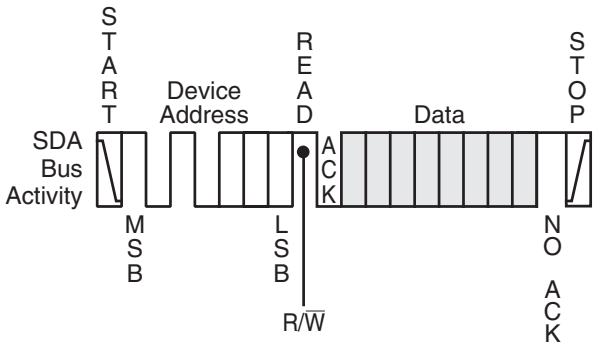


Figure 9. Random Address Read

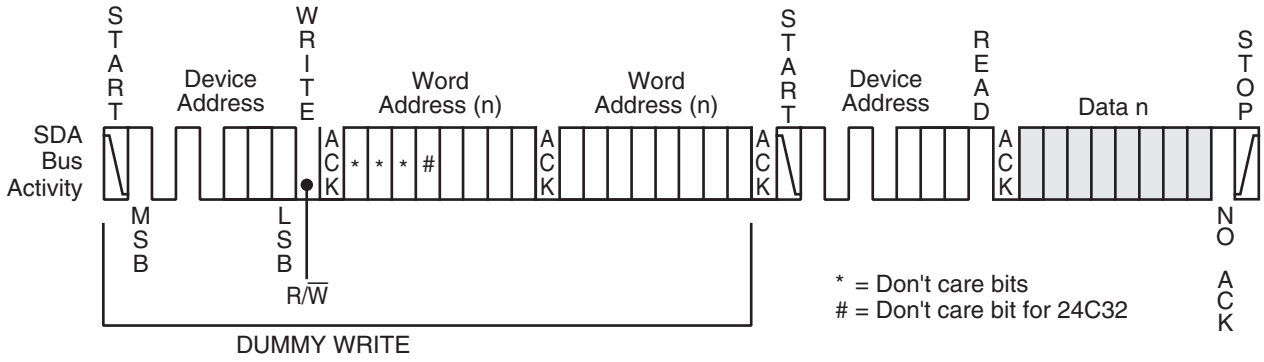
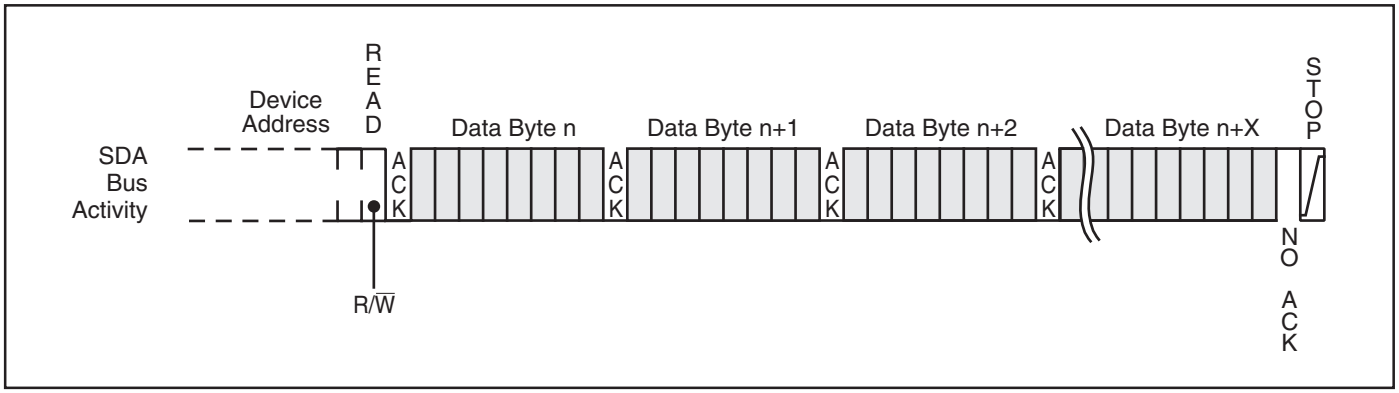


Figure 10. Sequential Read



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	–0.5 to +6.5	V
V_P	Voltage on Any Pin	–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (24C64 and 24C32)

Range	Ambient Temperature	Vcc
Industrial	–40°C to +85°C	1.8V to 5.5V

Note: offers Industrial grade for Commerical applications (-5°C to +75°C).

OPERATING RANGE (24C64 and 24C32)

Range	Ambient Temperature	Vcc
Automotive	–40°C to +125°C	2.5V to 5.5V

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.